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Preliminary PART B

Location	Machine Instruction	Assembly Language Equivalent
0x00	0x20020005	addi $v0, $zero, 5
0x04	0x2003000C	addi $v1, $zero, 12
0x08	0x2067FFF7	addi $a3, $v1, 65527
0x0C	0x00E22025	or $a0, $a3, $v0
0x10	0x00642824	and $a1, $v1, $a0
0x14	0x00A42820	add $a1, $a1, $a0
0x18	0x10A7000A	beq $a1, $a3, 40
0x1C	0x0064202A	slt $a0, $v1, $a0
0x20	0x10800001	beq $a0, $zero, 4
0x24	0x20050000	addi $a1, $zero, 0
0x28	0x00E2202A	slt $a0, $a3, $v0
0x2C	0x00853820	add $a3, $a0, $a1
0x30	0x00E23822	sub $a3, $a3, $v0
0x34	0xAC670044	sw $a3, 44($v1)
0x38	0x8C020050	lw $v0, 50($zero)
0x3C	0x08000011	j 44
0x40	0x20020001	addi $v0, $zero, 1
0x44	0xAC020054	sw $v0, 54($zero)
0x48	0x08000012	J 48

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Preliminary Part C : RTL expressions for new instruction

bge:

IM[PC]

if(R[rs] >= R[rt])

PC <- PC + 4 + BranchAddr

else

PC <- PC + 4

sw+:

IM[PC]

M[R[rs] + SignExtImm] <- R[rt]

R[rs] <- R[rs] + 4

PC <- PC + 4

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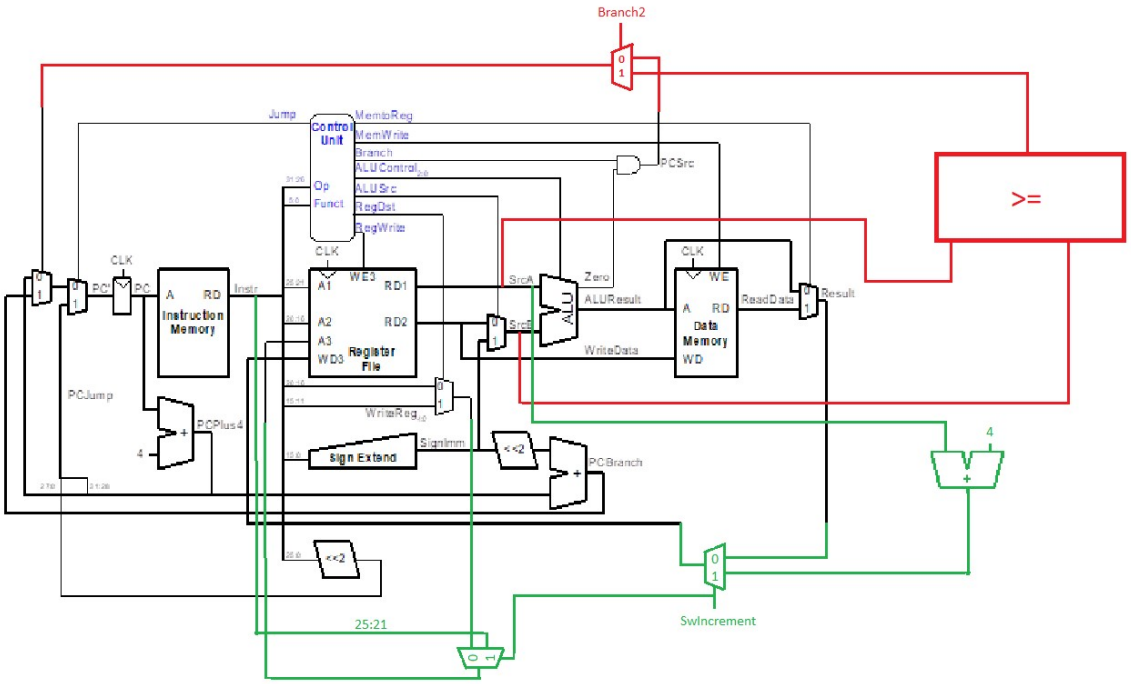
Preliminary Part D : Datapath



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Preliminary Part E : Control Table

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp	Jump	Branch2	SwIncrement
R-type	000000	1	1	0	0	0	0	10	0	0	0
lw	100011	1	0	1	0	0	1	00	0	0	0
sw	101011	0	x	1	0	1	x	00	0	0	0
beq	000100	0	x	0	1	0	x	01	0	0	0
addi	001000	1	0	1	0	0	0	00	0	0	0
j	000010	0	x	x	x	0	x	xx	1	0	0
bge	111110	1	x	0	x	0	0	xx	0	1	0
sw+	000001	1	x	x	x	1	0	xx	0	0	1

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Preliminary Part F : Test Program

```
0x00: addi $v0, $zero, 5
0x04: or   $a0, $a3, $v0
0x08: and  $a1, $v1, $a0
0x0C: beq  $a1, $a3, 8        # jump 2 instructions
0x10: or   $a0, $a3, $v0
0x14: and  $a1, $v1, $a0
0x18: slt  $a0, $v1, $a0
0x1C: sub  $a3, $a3, $v0
0x20: sw   $a3, 44($v1)
0x24: lw   $v1, 50($zero)
0x28: sw+  $a3, 44($v1)       # new instruction
0x2C: j    30
0x30: and $v0, $zero, $zero
0x34: addi $v1, $zero, 5
0x38: bge  $v1, $v0, 30       # new instruction
0x3C: sw   $a3, 44($v1)       # this will not be reached
```

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COMPUTER SCIENCE

CS 224 : COMPUTER ORGANIZATION

PRELIMINARY DESIGN REPORT

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28.11.2019