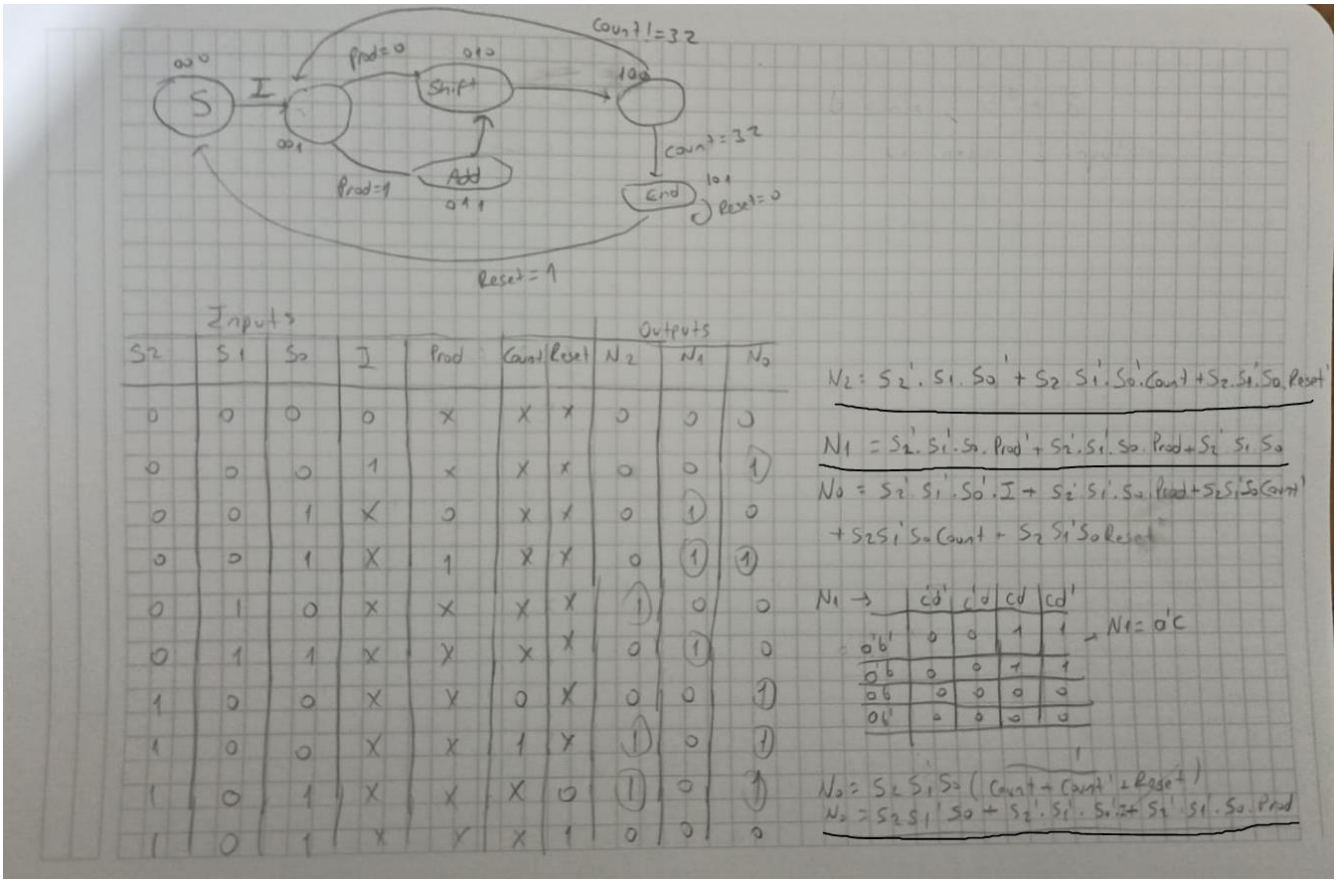
Question1)

Adder.v has been designed.And fsm designed for Control.v but can not designed Multiplier.v and Control.v.



N2 = S2’S1S0’+S2S1’S0’Count+S2S1’S0Reset’

N1 = S2’S1’S0Prod’+S2’S1’S0Prod+S2’S1S0

N0 = S2S1’S0+S2’S1’S0’I+S2’S1’S0Prod

Question 2)

1)Designed 32 bit adder and test.

```
ModelSim> vsim -voptargs=+acc work.adder_test
# vsim -voptargs=+acc work.adder_test
# Loading work.adder_test
# Loading work.adder_32bit
# Loading work.full_adder
VSIM 7> run
# Input1=00000000000000000000000000000001=           1
# Input2=00000000000000000000000000000111 =           7
# Sum=00000000000000000000000000001000 =          8
#
```

2)Designed 32 bit and with test.

```
# Top level modules:
#       xor_test
VSIM 12> vsim -voptargs=+acc work.xor_test
# vsim -voptargs=+acc work.xor_test
# Loading work.xor_test
# Loading work.xor_32bit
VSIM 13> run
# Input1=00000100010010000000000010000001=   71827585
# Input2=00000001010000000100000010000111 =   20988039
# Sum=00000101000010000100000000000000 =  84426752
#
```

3)Designed 32 bit nor and test

```
ModelSim> vsim -voptargs=+acc work.nor_test
# vsim -voptargs=+acc work.nor_test
# Loading work.nor_test
# Loading work.nor_32bit
VSIM 5> step
VSIM 6> run
# Input1=00000001100010010000100010000001=   25757825
# Input2=00000001010000010100010010000111 =   21054599
# Sum=11111110001101101011001101111000 =4264997752
#
```

4)Designed 32 bit or and test.

```
# Top level modules:
#       or_test
VSIM 9> vsim -voptargs=+acc work.or_test
# vsim -voptargs=+acc work.or_test
# Loading work.or_test
# Loading work.or_32bit
VSIM 10> run
# Input1=00000000000010000000000010000001=     524417
# Input2=00000000000000000100000010000111 =      16519
# Sum=00000000000010000100000010000111 =    540807
#
```

5)Designed 32 bit slt and test.

```
# Top level modules:
#       slt_test
ModelSim> vsim -voptargs=+acc work.slt_test
# vsim -voptargs=+acc work.slt_test
# Loading work.slt_test
# Loading work.slt_32bit
VSIM 5> run
# Input1=00000100010010000000000010000001=   71827585
# Input2=00000001010000000100000010000111 =   20988039
# Sum=11111010111101111011111111111001 =4210540537
#
```

6)Designed 32bit substractor with adder and test.

```
# Top level modules:
#       substractor_test
VSIM 8> vsim -voptargs=+acc work.substractor_test
# vsim -voptargs=+acc work.substractor_test
# Loading work.substractor_test
# Loading work.substractor_32bit
# Loading work.full_adder
VSIM 9> run
# Input1=00000000000000000000000000001111=         15
# Input2=00000000000000000000000000000111 =          7
# Substract=00000000000000000000000000001000 =         8
#
```

7)Designed 32 bit xor and test.

```
# Top level modules:
#       xor_test
VSIM 12> vsim -voptargs=+acc work.xor_test
# vsim -voptargs=+acc work.xor_test
# Loading work.xor_test
# Loading work.xor_32bit
VSIM 13> run
# Input1=00000100010010000000000010000001=   71827585
# Input2=00000001010000000100000010000111 =   20988039
# Sum=00000101000010000100000000000000 =  84426752
#
```