C sclect → 0 for R-Type (ADD, ADC, ADZ, ADL, ~~ADI~~, NDU, NDC)

① A1_sclect → 0 → ADD
ADC
ADZ
ADL
ADI.
NDU
NDC
NDZ.

Not Defined
LHI.

(1)

1 → LW.
SW

② A2_sclect → 0 → ADD
ADC
ADZ
ADL
NDU
NDC
NDZ

ND (Not Defined)
ADI
LHI
LW

1 → SW

③ Reg_write_enable_to ALU

olp from ID Decoder. Goes to ALU controller and gets redefined based on conditional instructions.

1 for all instn writing to Register

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g- Write-enable-out-from-ALU.

Redefined RegWrite Enable based on conditional Instrn.

(5) Zero-write-en, Carry-write-en } Defined from ALU-controller

(6) ALU-control (2)

00 → Add
01 → NAND
10 → Nop

(7) ALU-SRC-B-select

00 → RF-D2
01 → Imm 6
10 → Imm 6 sll 1 (ADL)

(8) MemRead
MemWrite

(9) .Reg Data Select
Select Signal for value to be written to Register

00 → ALU_OUT
01 → M[ALUOUT]
10 → (IR(8:0) → LS7) (for LHI).

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(3).

(10) - Reg_Dst_Select

Selects the Destination based on Instr^{n}.

00 → IR(5:3)	01 IR(8:6)	10. IR(11:9)
ADD.	ADI.	LHI.
ADC.		LW. (11:9)
ADZ.		
ADL.		
NDU		
NDC		Undefined
NDZ.		SW.

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