Course Outline: Introduction to VLSI Design

Instructor: Jun Albert Pardillo  
Credit Units: 3  
Target Students: 2nd Year Electronic Engineering Students  
Total Hours: 54  
Class Hours per Week: 3  
  
Course Description:  
This course is designed to introduce 2nd year Electronic Engineering students to the fundamentals of Very Large Scale Integration (VLSI) design. The course will cover the basics of digital design, including combinational and sequential logic, and will then delve into the specifics of VLSI design, including transistor-level design, layout, and verification.  
  
Students will learn how to use industry-standard design tools, such as Cadence and Synopsys, to design and simulate digital circuits. They will also gain hands-on experience with the design and layout of basic digital circuits, such as adders, multipliers, and flip-flops.  
  
Throughout the course, students will be exposed to the latest trends and challenges in VLSI design, including low-power design, design for manufacturability, and design for testability. They will also learn about the impact of technology scaling on VLSI design, and how to design for different process technologies.  
  
By the end of the course, students will have a solid understanding of the principles of VLSI design, and will be able to design and simulate basic digital circuits using industry-standard design tools. They will also be prepared to take on more advanced courses in VLSI design, and to pursue careers in the semiconductor industry.

# Topic: Introduction to Digital Design and VLSI

Hours: 10

- Overview of VLSI design process  
 - Introduction to digital circuits and logic design  
 - Basics of combinational and sequential logic  
 - Introduction to simulation tools

# Topic: Transistor-Level Design and Layout

Hours: 12

- MOS transistor theory  
 - CMOS logic gates design  
 - Basic layout concepts and techniques  
 - Introduction to layout design tools

# Topic: Advanced Digital Circuit Design

Hours: 12

- Design and simulation of adders, multipliers, and flip-flops  
 - Timing analysis and optimization  
 - Power dissipation and low-power design techniques

# Topic: Design for Manufacturability and Testability

Hours: 10

- Challenges in VLSI design for manufacturability  
 - Yield enhancement techniques  
 - Introduction to design for testability concepts  
 - Fault modeling and testing strategies

# Topic: Trends in VLSI Design

Hours: 10

- Impact of technology scaling  
 - Design for different process technologies  
 - Current trends and future directions in VLSI design