```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   18:59:36 09/22/2024
8   // Design Name:   barrel
9   // Module Name:   C:/Xilinx/14.7/rtr/tbfsh.v
10  // Project Name:  rtr
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: barrel
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24
25  module tbfsh;
26
27     // Inputs
28     reg [7:0] a;
29     reg [2:0] b;
30     reg dir;
31
32     // Outputs
33     wire [7:0] y;
34
35     // Instantiate the Unit Under Test (UUT)
36     barrel uut (
37        .a(a),
38        .b(b),
39        .dir(dir),
40        .y(y)
41     );
42
43     initial begin
44        // Initialize Inputs
45        a = 8'b10101010;b = 3'b001;dir = 0;#100;
46        a = 8'b10101010;b = 3'b010;dir = 0;#100;
47        a = 8'b10101010;b = 3'b011;dir = 0;#100;
48        a = 8'b10101010;b = 3'b001;dir = 1;#100;
49        a = 8'b10101010;b = 3'b010;dir = 1;#100;
50        a = 8'b10101010;b = 3'b011;dir = 1;#100;
51
52        // Add stimulus here
53
54     end
55
56  endmodule
57
```