FPGA to LCD HBR Board

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| --- | --- | --- | --- | --- |
| LCD Pins | Function | FPGA GPIO 1 Block | FPGA GPIO | Quartus |
| 1 | GND | 12 |  |  |
| 2 | Vdd  Logic Power | 11 |  |  |
| 3 | Contrast |  |  |  |
| 4 | RS | 14 | 19 | R11 |
| 5 | R/W | 13 | 18 | T10 |
| 6 | E | 15 | 110 | P11 |
| 7 | DB0 | 2 | 10 | F13 |
| 8 | DB1 | 4 | 11 | T15 |
| 9 | DB2 | 5 | 12 | T14 |
| 10 | DB3 | 6 | 13 | T13 |
| 11 | DB4 | 7 | 14 | R13 |
| 12 | DB5 | 8 | 15 | T12 |
| 13 | DB6 | 9 | 16 | R12 |
| 14 | DB7 | 10 | 17 | T11 |
| 15 | A Backlight |  |  |  |
| 16 | K Backlight |  |  |  |

Standard LCD Layout single row with Pin 1 is nearest to the edge

See Nano manual for GPIO layouts and Pin assignments