BLE113

DATA SHEET

Wednesday, 25 March 2015

Version 1.46

bluegiga

VERSION HISTORY

Version	Comment
1.0	Preliminary datasheet -> production datasheet. No changes
1.1	Pull-up resistors added to P1_0 and P1_1 in the example schematic
1.2	5 mm restriction removed from the FCC statement
1.3	Product code for 256k variant added. Peripheral mapping table: analog comparator added. Added note that pins configured as peripheral I/O signals do not have pull-up / -down capability. RF Characteristics added.
1.4	Product numbering updated
1.41	CE info
1.42	Updated FCC ID in one incorrect location
1.43	PIO current drive capability figures added
1.44	Current consumption profile added
1.45	SPI slave mode removed
1.46	Example layouts added

TABLE OF CONTENTS

BLE113 *Bluetooth*® Smart Module

DESCRIPTION

BLE113 is a *Bluetooth* Smart module targeted for small and low power sensors and accessories. It integrates all features required for a *Bluetooth* Smart application: *Bluetooth* radio, software stack and GATT based profiles.

BLE113 *Bluetooth* Smart module can also host end user applications, which means no external micro controller is required in size or price constrained devices.

BLE113 module has flexible hardware interfaces to connect to different peripherals and sensors. BLE113 can be powered directly from a standard 3V coin cell battery or pair of AAA batteries.

In lowest power sleep mode it consumes only 500nA and will wake up in few hundred microseconds.

APPLICATIONS:

- Health and fitness sensors
- Medical sensors
- iPhone and iPad accessories
- Security and proximity tags
- Key fobs
- Smart home sensors and collectors
- Wireless keys
- HID keyboards and mice

KEY FEATURES:

- *Bluetooth* v. 4.0, single mode compliant
  - Supports master and slave modes
  - Up to eight connections
- Integrated *Bluetooth* Smart stack
  - GAP, GATT, L2CAP and SMP
  - Bluetooth Smart profiles
- Radio performance
  - TX power : 0 dBm to -23 dBm
  - Receiver sensitivity: -93 dBm
- Ultra low current consumption
  - Transmit: 18.2 mA (0dBm)
  - Transmit: 14.3 mA (0dBm + DC/DC)
  - Receive: 14.3 mA
  - Sleep mode 3: 0.4 uA
- Flexible peripheral interfaces
  - UART and SPI
  - I2C, PWM and GPIO
  - 12-bit ADC
- Host interfaces:
  - UART
- Programmable 8051 processor for stand-alone operation
- Dimensions: 9.15 x 15.75 x 2.1 mm
- *Bluetooth*, CE, FCC, IC, South Korea and Japan qualified

1 BLE113 Product numbering

Product code	Description
BLE113-A	BLE113 with integrated chip antenna, 128k flash memory
BLE113-A-M256K	BLE113 with integrated chip antenna, 256k flash memory

2 Pinout and Terminal Description

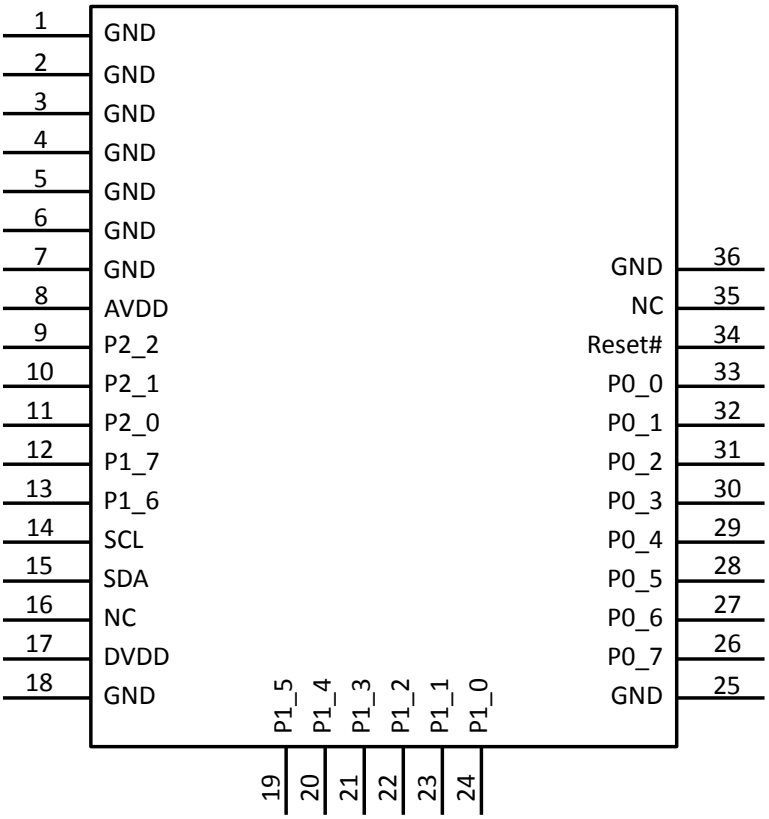

Figure 1: BLE113

RESET	34		Active low reset. Internal pull-up.
GND	1 - 7, 18, 25, 36	GND	GND
DVDD	17	Supply voltage	Supply voltage 2V - 3.6V
AVDD	8	Supply voltage	Supply voltage 2V - 3.6V

Table 1: Supply and RF Terminal Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	DESCRIPTION
9	P2_2	Digital I/O	Configurable I/O port, See table 3
10	P2_1		
11	P2_0		
12	P1_7		
13	P1_6		
19	P1_5		
20	P1_4		
21	P1_3		
22	P1_2		
26	P0_7		
27	P0_6		
28	P0_5		
29	P0_4		
30	P0_3		
31	P0_2		
32	P0_1		
33	P0_0		
23	P1_1	Digital I/O	Configurable I/O port with 20mA driving capability, See table 3
24	P1_0		
14	SCL	I^2C clock or digital I/O	Can be used as I^2C clock pin or digital I/O. Leave floating if not used. If grounded disable pull up.
15	SDA	I^2C data or digital I/O	Can be used as I^2C data pin or digital I/O. Leave floating if not used. If grounded disable pull up.

Table 2: Terminal Descriptions

PERIPHERAL / FUNCTION		P0								P1								P2			HARDWARE.XML Example (*
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	2	1	0	
Analog Comparator				+	-																(***
ADC		A7	A6	A5	A4	A3	A2	A1	A0												(***
USART 0 SPI (**	Alt.1			C	SS	MO	MI														<usart channel="0" mode="spi_master" alternate="1" ...
	Alt.2											MO	MI	C	SS						<usart channel="0" mode="spi_master" alternate="2" ...
USART 0 UART	Alt.1			RT	CT	TX	RX														<usart channel="0" mode="uart" alternate="1" ...
	Alt.2											TX	RX	RT	CT						<usart channel="0" mode="uart" alternate="2" ...
USART 1 SPI (**	Alt.1			MI	MO	C	SS														<usart channel="1" mode="spi_master" alternate="1" ...
	Alt.2									MI	MO	C	SS								<usart channel="1" mode="spi_master" alternate="2" ...
USART 1 UART	Alt.1			RX	TX	RT	CT														<usart channel="1" mode="uart" alternate="1" ...
	Alt.2									RX	TX	RT	CT								<usart channel="1" mode="uart" alternate="2" ...
TIMER 1	Alt.1		4	3	2	1	0														<timer index="1" alternate="1" ...
	Alt.2	3	4												0	1	2				<timer index="1" alternate="2" ...
TIMER 3	Alt.1												1	0							<timer index="3" alternate="1" ...
	Alt.2									1	0										<timer index="3" alternate="2" ...
TIMER 4	Alt.1															1	0				<timer index="4" alternate="1" ...
	Alt.2																			0	<timer index="4" alternate="2" ...
DEBUG																		DC	DD		
OBSSEL												5	4	3	2	1	0				

*) Refer to Profile Toolkit Developer Guide for detailed settings

**) SS is the slave select signal when BLE113 is set as SPI slave. When set as SPI master, any available I/O can be used as chip select signal of BLE113

***) The analog comparator and the ADC will be turned on automatically when taken in use and the configuration is done using API (Application Programming Interface). Refer to Bluetooth Smart Software API Reference

NOTE: Pins configured as peripheral I/O signals do not have pull-up / -down capability

Table 3:Peripheral I/O Pin Mapping

2.1 I/O Ports

Each I/O port can be configured as an input or output. When configured as input, each I/O port, except pins P1_0 and P1_1, can also be configured with internal pull-up, pull-down or tri-state. Pull-down or pull-up can only be configured to whole port, not individual pins. Unused I/O pins should have defined level and not be floating. See the Profile Toolkit developer guide for more information about the configuration.

During reset the I/O pins are configured as inputs with pull-ups. P1_0 and P1_1 are inputs but do not have pull-up or pull-down.

NOTE: Pins configured as peripheral I/O signals do not have pull-up / -down capability

2.2 UART

UART baud rate can be configured up 2 Mbps. See the Profile Toolkit developer guide for more information. Following table lists commonly used baud rates for BLE113

Baud rate (bps)	Error (%)
2400	0.14
4800	0.14
9600	0.14
14 400	0.03
19 200	0.14
28 800	0.03
38 400	0.14
57 600	0.03
76 800	0.14
115 200	0.03
230 400	0.03

Table 4: Commonly used baud rates for BLE113

2.3 Electrical Characteristics

2.4 Absolute Maximum Ratings

Note: These are absolute maximum ratings beyond which the module can be permanently damaged. These are not maximum operating conditions. The maximum recommended operating conditions are in the table 6.

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
AVDD, DVDD	-0.3	3.9	V
Other Terminal Volatages	VSS-0.4	VDD+0.4	V

*)All supply nets must have the same voltage

Table 5: Absolute Maximum Ratings

2.5 Recommended Operating Conditions

Rating	Min	Max	Unit
Operationg Temperature Range	-40	+85	°C
AVDD, DVDD (*	2.0	3.6	V

*) Supply voltage noise should be less than 10mVpp. Excessive noise at the supply voltage will reduce the RF performance.

Table 6: Recommended Operating Conditions

2.6 DC Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage	DVDD =3V0	2.5			V
Logic-0 input current	Input equals 0V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
I/O pin pull-up and pull-down resistors			20		kΩ
Logic-0 output voltage, 4 mA pins	Output load 4 mA			0.5(*	V
Logic-1 output voltage, 4 mA pins	Output load 4 mA	2.4(*			V

***) See Figure 2 and Figure 3**

Table 7: DC Characteristics @ VDD=3.0V

For detailed I/O terminal characteristic and timings refer to the CC2541 datasheet available in (http://www.ti.com/lit/ds/symlink/cc2541.pdf)

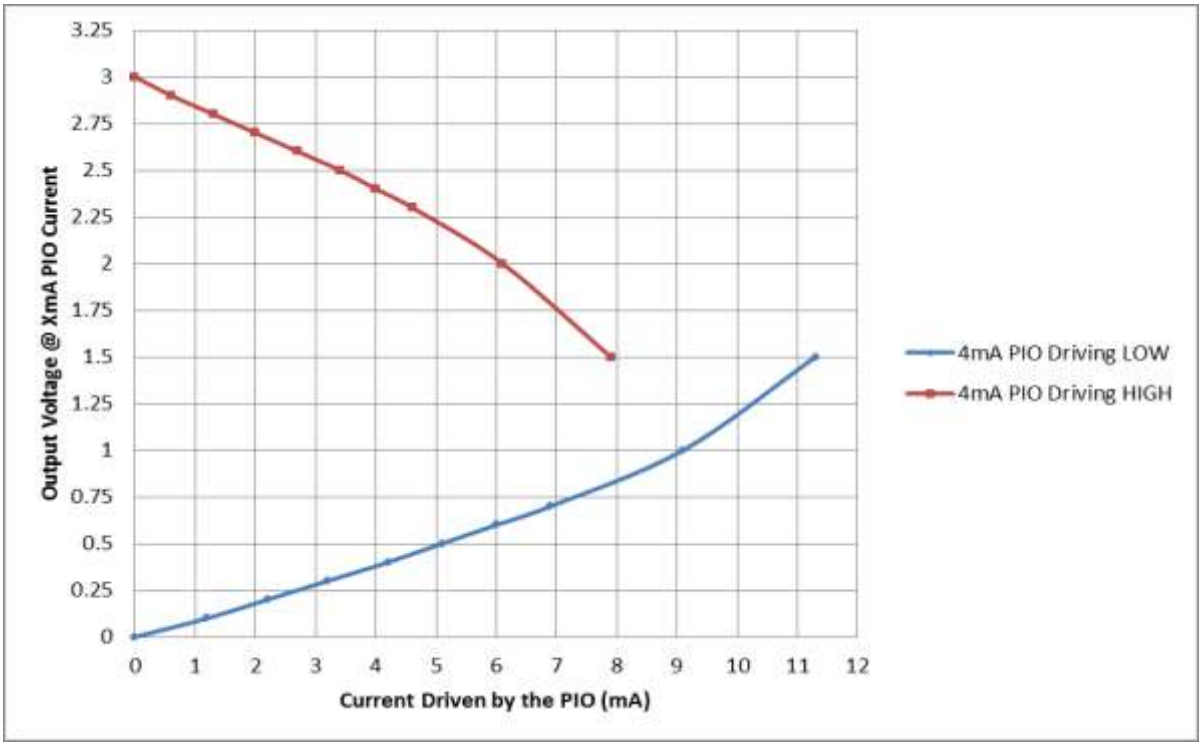

Figure 2: 4mA PIO Current Drive Capability @ VDD=3.0V

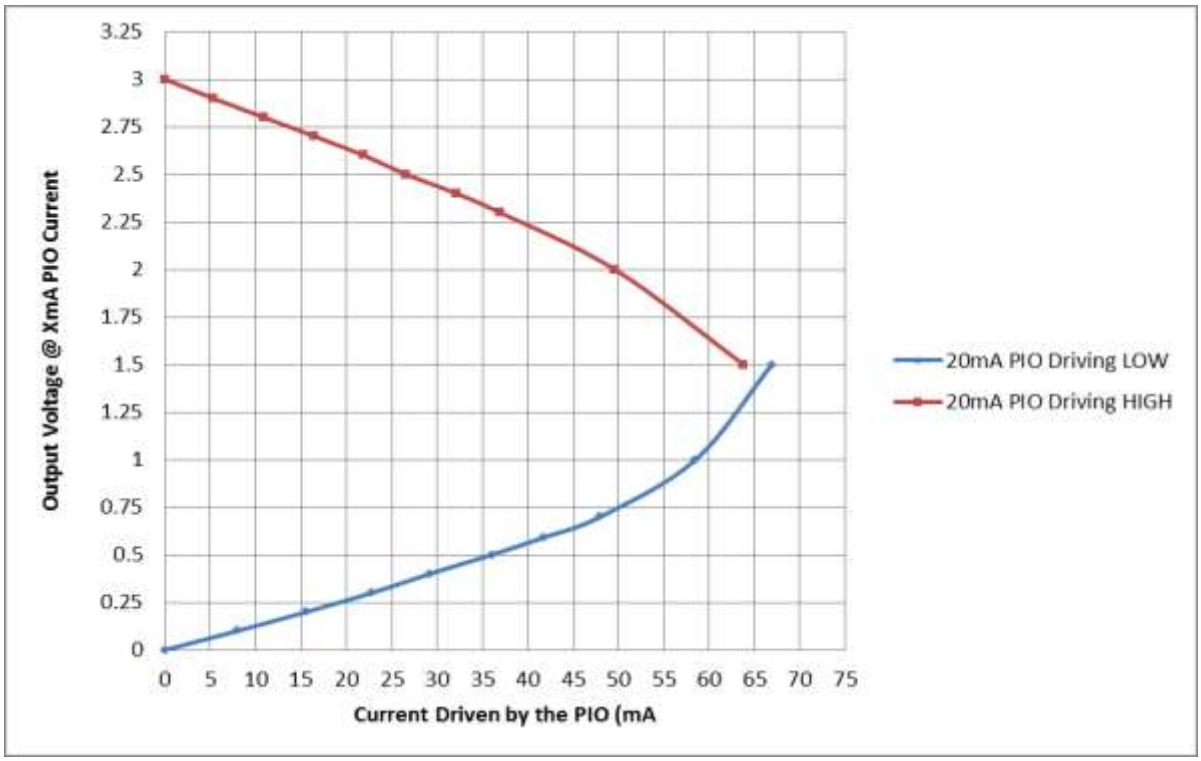

Figure 3: 20mA PIO (P1_0 and P1_1) Current Drive Capability @ VDD=3.0V

2.7 Current Consumption

Power mode	hardware.xml	Min	Typ	Max	Unit
Transmit	<txpower power = "1"/> <slow clock enable = ”true”>		18.2		mA
	<txpower power = "7"/> <slow clock enable = ”true”>		18.3		mA
	<txpower power = "15"/> <slow clock enable = ”true”>		20.7		mA
	<txpower power = "1"/> <slow clock enable = ”false”>		23.6		mA
	<txpower power = "7"/> <slow clock enable = ”false”>		23.6		mA
	<txpower power = "15"/> <slow clock enable = ”false”>		26.1		mA
Receive	<slow clock enable = ”true”>		21.9		mA
	<slow clock enable = ”false”>		27.0		mA
Power mode 1			270		µA
Power mode 2			1		µA
Power mode 3			0.5		µA

Table 8: Current consumption of BLE113

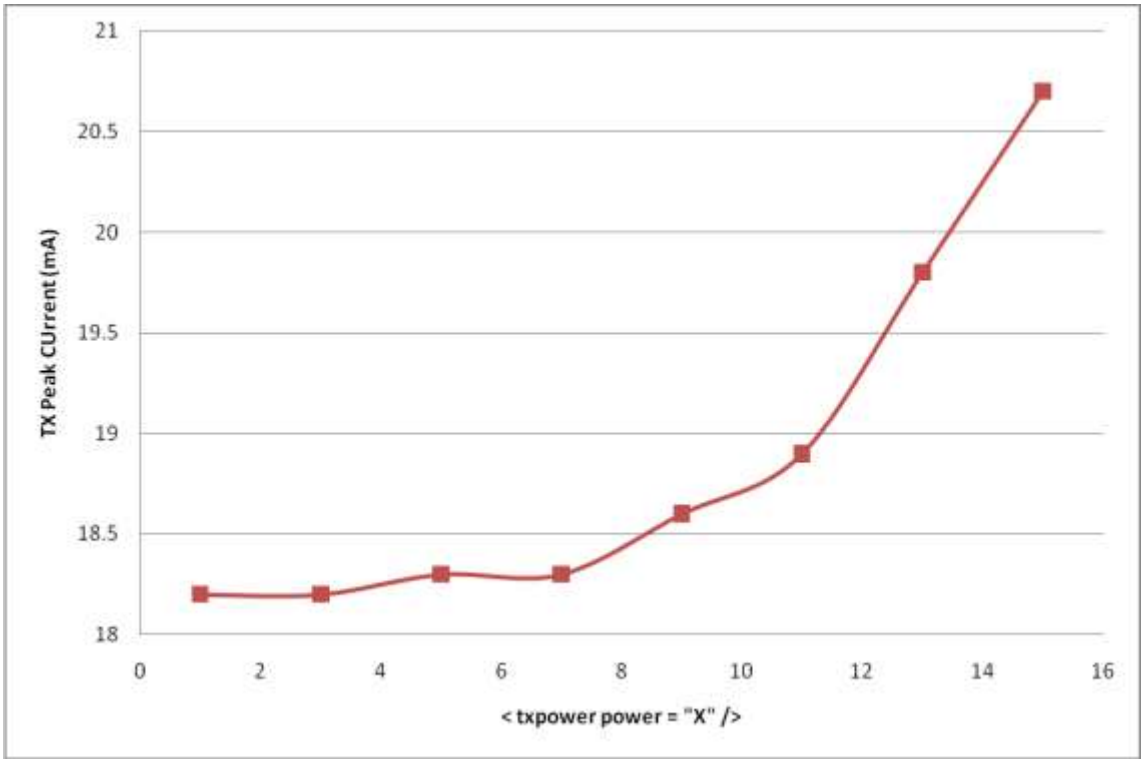

Figure 4: BLE113 TX peak current as a function of the setting in the HW configuration file

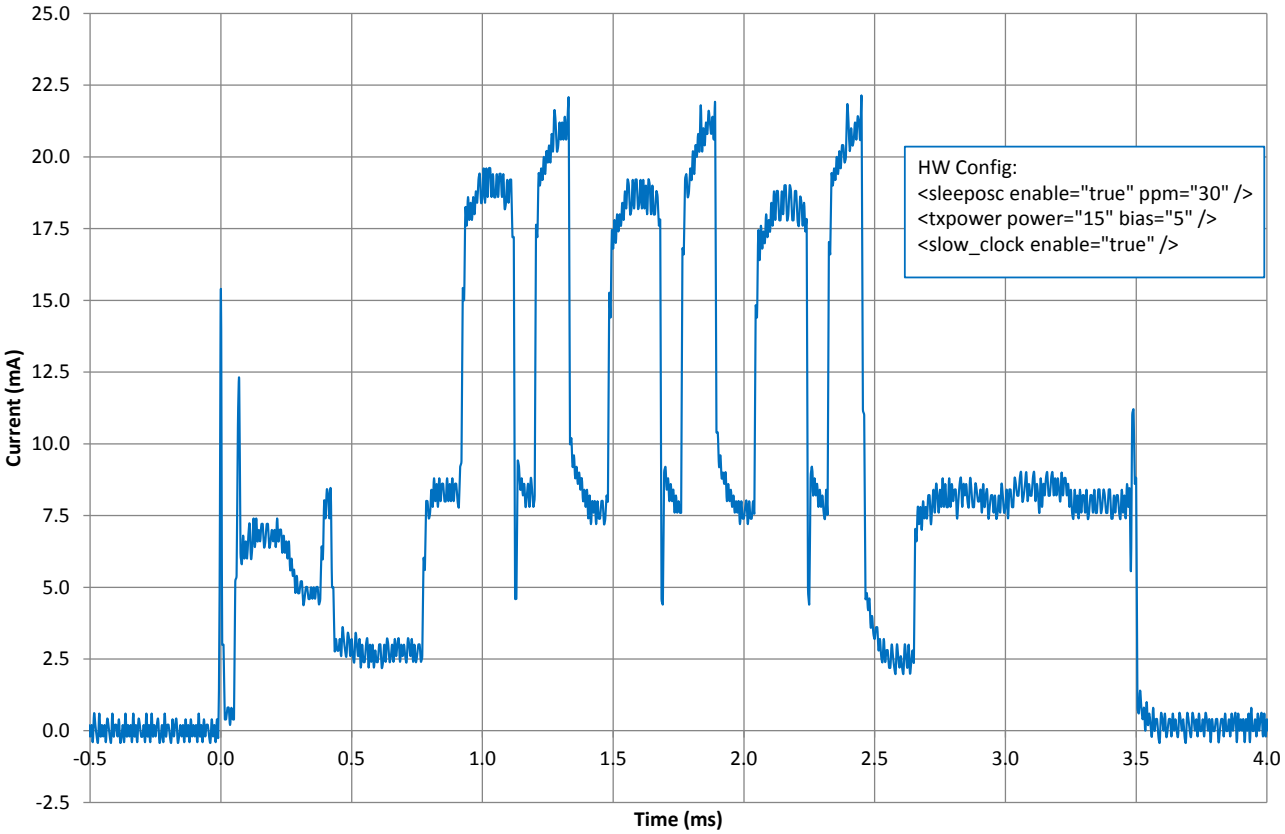

Figure 5: Current consumption profile of BLE113, HR example, advertising

2.8 RF Characteristics

Parameter	Min	Typ	Max	Unit
Transmit power	-1.5	0	1	dBm
Receiver Sensitivity		-93		dBm
Gain of the Antenna			0.5	dBi
Efficiency of the antenna		30		%

Table 9: RF Characteristic of BLE113

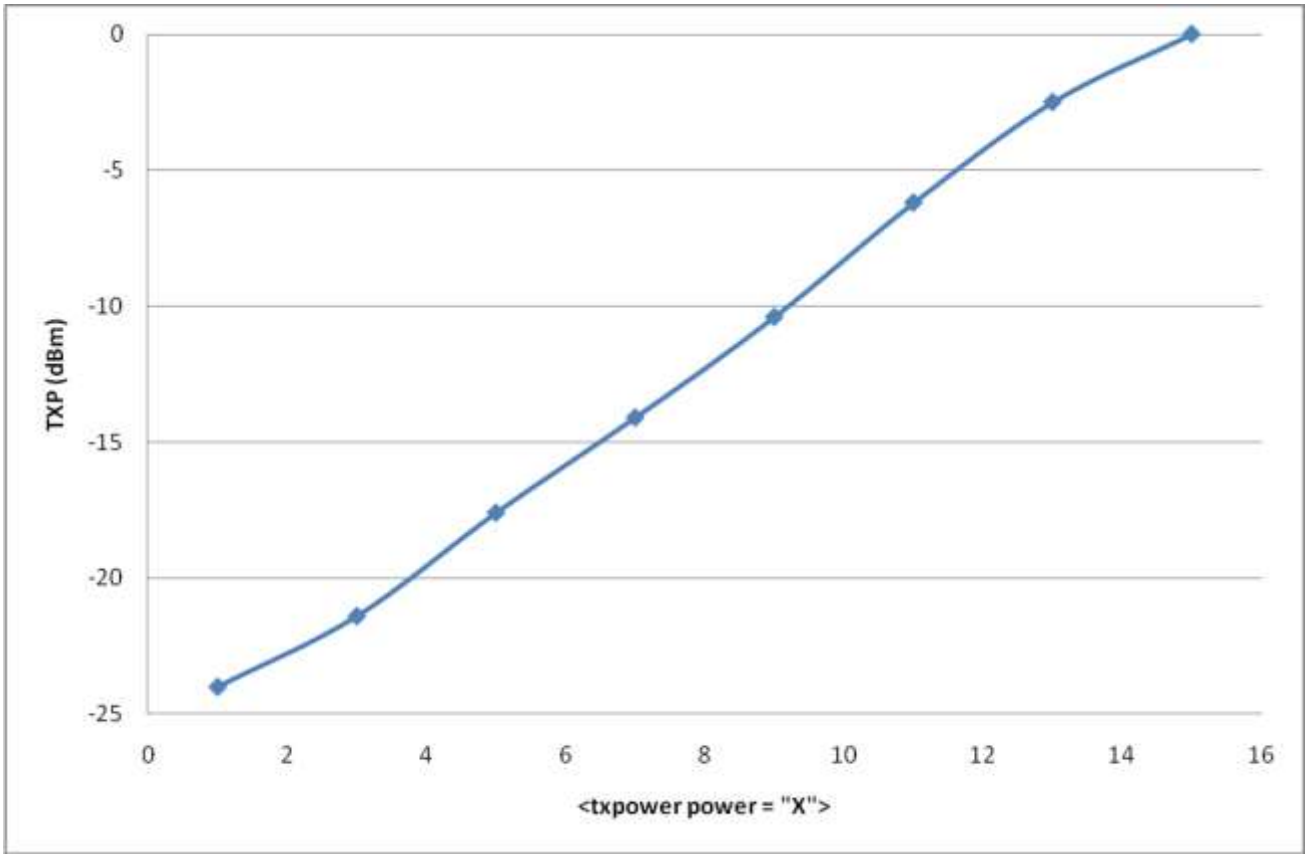

Figure 6: BLE113 TX power as a function of the setting in the HW configuration file

2.9 Antenna characteristics

The antenna is monopole type of chip antenna. The antenna impedance matching is optimized for 1 mm – 2 mm mother board PCB thickness. The radiation pattern is impacted by the layout of the mother board. Typically the highest gain is towards GND plane and weakest gain away from the GND plane. Figures 4 – 6 show the radiation pattern of BLE113 when mounted to the development board.

The typical efficiency of the antenna is 25…35% depending on the mother board layout. Maximum gain is 0.5 dBi.

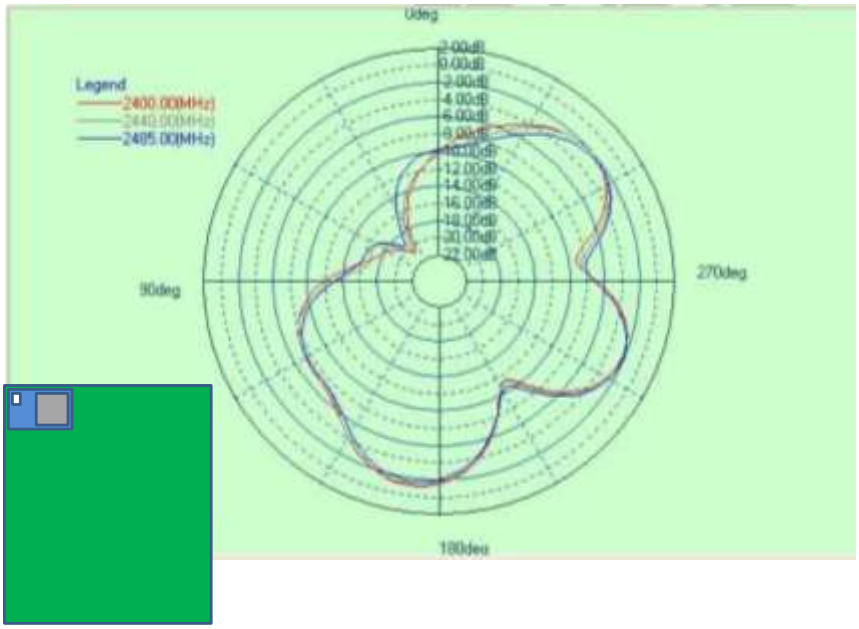

Figure 7: Radiation pattern of BLE113, top view

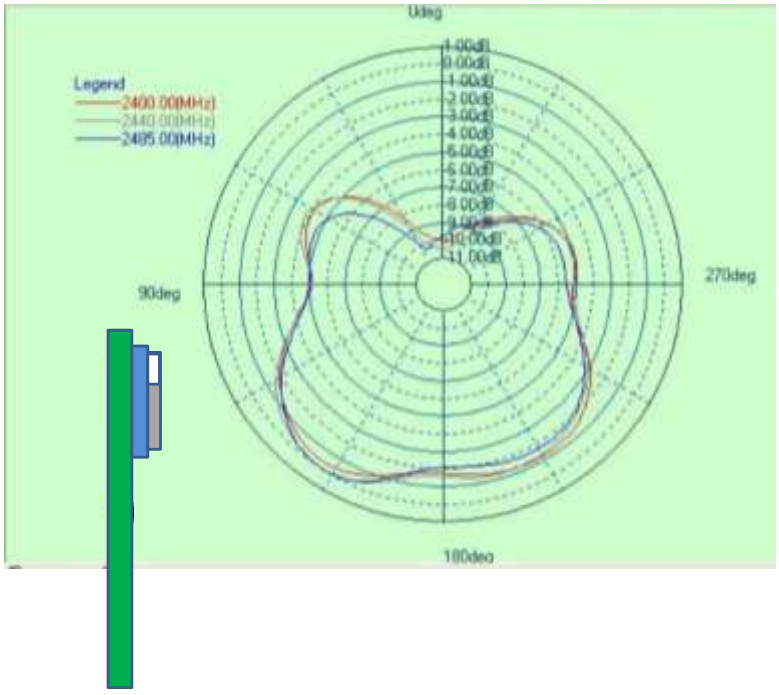

Figure 8: Radiation pattern of BLE113, front view

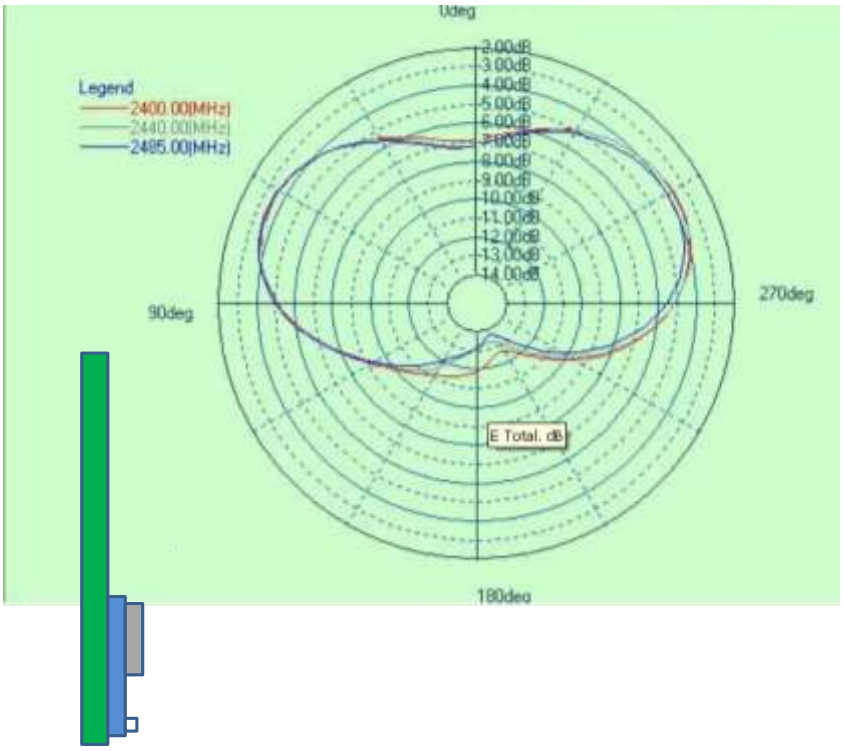

Figure 9: Radiation pattern of BLE113, side view

3 Physical Dimensions

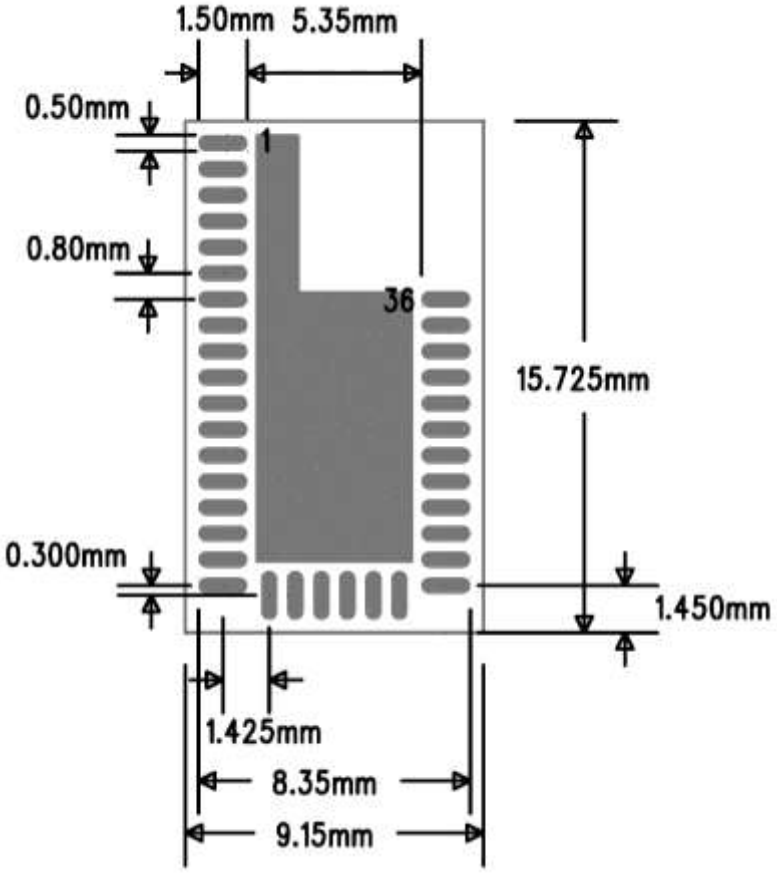

Figure 10: Physical dimensions and pinout (top view)

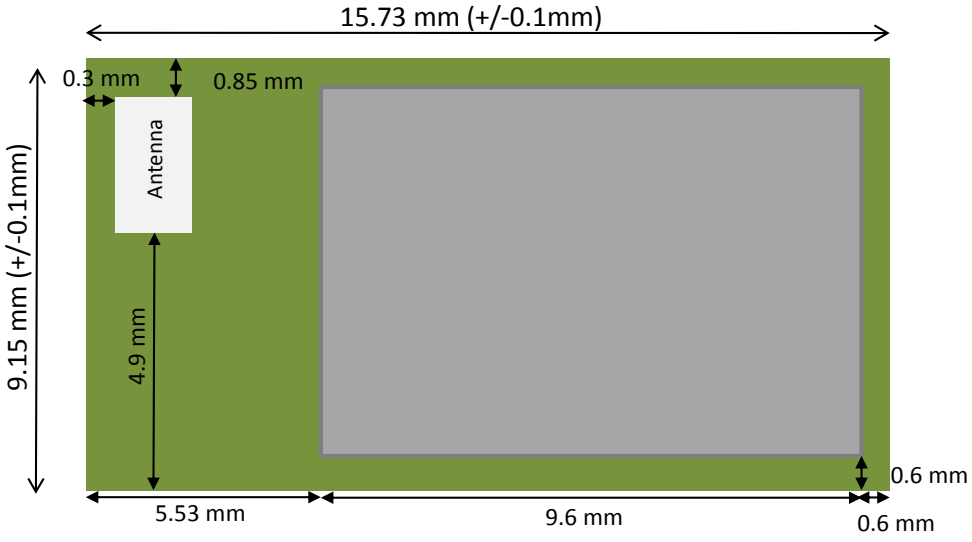

Figure 11: Physical dimensions (top view)

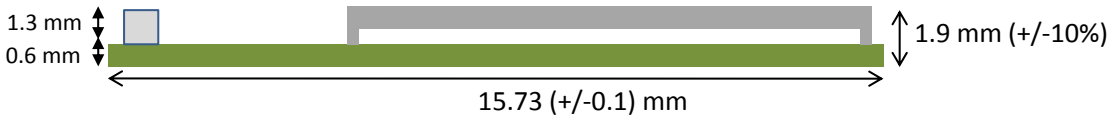

Figure 12: Physical dimensions (side view)

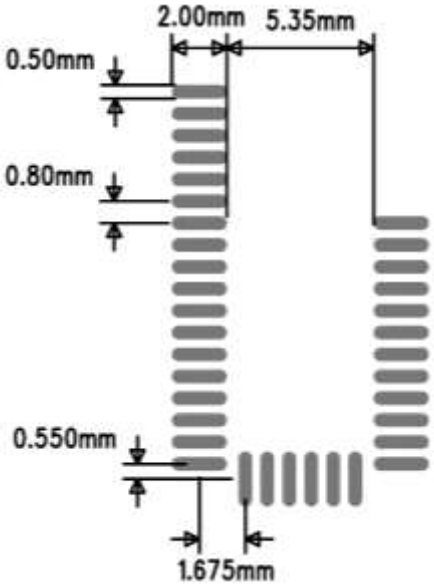

Figure 13: Recommended land pattern for BLE113-A

4 Power-On Reset and Brownout Detector

BLE113 includes a power-on reset (POR), providing correct initialization during device power on. It also includes a brownout detector (BOD) operating on the regulated 1.8-V digital power supply only. The BOD protects the memory contents during supply voltage variations which cause the regulated 1.8-V power to drop below the minimum level required by digital logic, flash memory, and SRAM. When power is initially applied, the POR and BOD hold the device in the reset state until the supply voltage rises above the power-on-reset and brownout voltages.

5 Design Guidelines

5.1 General Design Guidelines

LE113 can be used directly with a coin cell battery. Due to relatively high internal resistance of a coin cell battery it is recommended to place a 100uF capacitor in parallel with the battery. The internal resistance of a coin cell battery is initially in the range of 10 ohms but the resistance increases rapidly as the capacity is used. Basically the higher the value of the capacitor the higher is the effective capacity of the battery and thus the longer the life time for the application. The minimum value for the capacitor depends on the end application and the maximum transmit power used. The leakage current of a 100uF capacitor is in the range of 0.5 uA to 3 uA and generally ceramic capacitors have lower leakage current than tantalum or aluminum electrolytic capacitors.

Optionally TI's TPS62730 can be used to reduce the current consumption during TX/RX and data processing stages. TPS62730 is an ultra low power DC/DC converter with by-pass mode and will reduce the current consumption during transmission nominally by ~20% when using 3V coin cell battery.

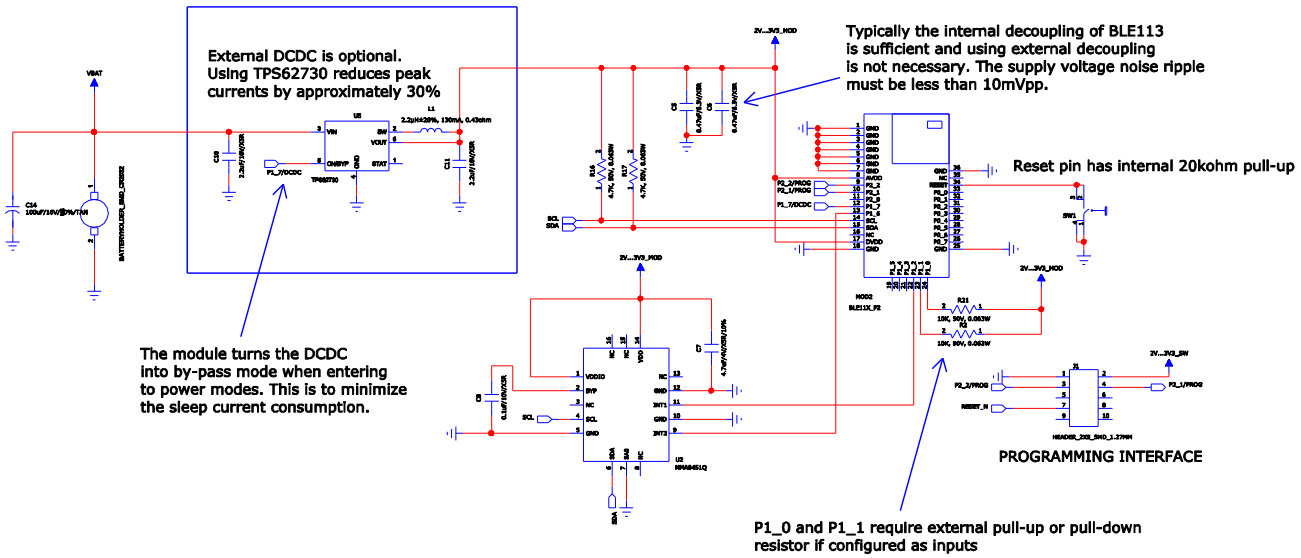

Figure 14: Example schematic for BLE113 with a coin cell battery, TPS62730 DCDC converter and an I2C accelerometer

5.2 Layout Guide Lines

Use good layout practices to avoid excessive noise coupling to supply voltage traces or sensitive analog signal traces. If using overlapping ground planes use stitching vias separated by max 3 mm to avoid emission from the edges of the PCB. Connect all the GND pins directly to a solid GND plane and make sure that there is a low impedance path for the return current following the signal and supply traces all the way from start to the end.

A good practice is to dedicate one of the inner layers to a solid GND plane and one of the inner layers to supply voltage planes and traces and route all the signals on top and bottom layers of the PCB. This arrangement will make sure that any return current follows the forward current as close as possible and any loops are minimized.

Figure 15: Typical 4-layer PCB construction

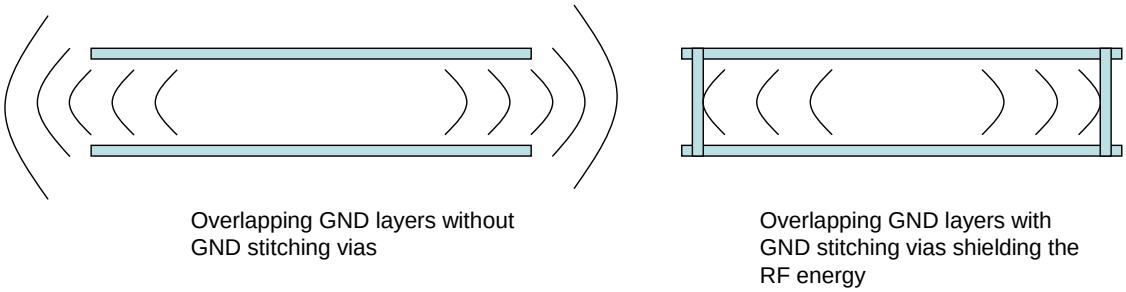

Figure 16: Use of stitching vias to avoid emissions from the edges of the PCB

5.3 BLE113-A Layout Guide

For optimal performance of the antenna place the module at the corner of the PCB as shown in the figure 14. Do not place any metal (traces, components, battery etc.) within the clearance area of the antenna. Connect all the GND pins directly to a solid GND plane. Place the GND vias as close to the GND pins as possible. Use good layout practices to avoid any excessive noise coupling to signal lines or supply voltage lines. Avoid placing plastic or any other dielectric material closer than 5 mm from the antenna. Any dielectric closer than 5 mm from the antenna will detune the antenna to lower frequencies.

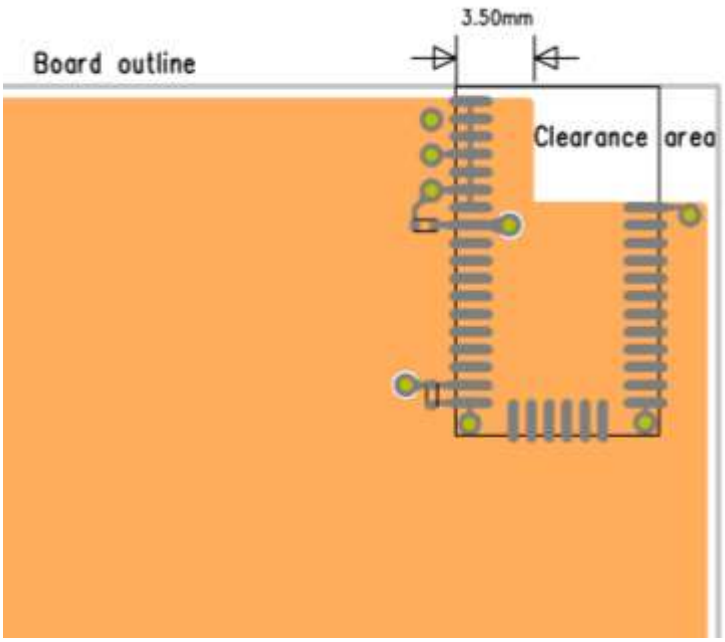

Figure 17: Recommended layout for BLE113-A

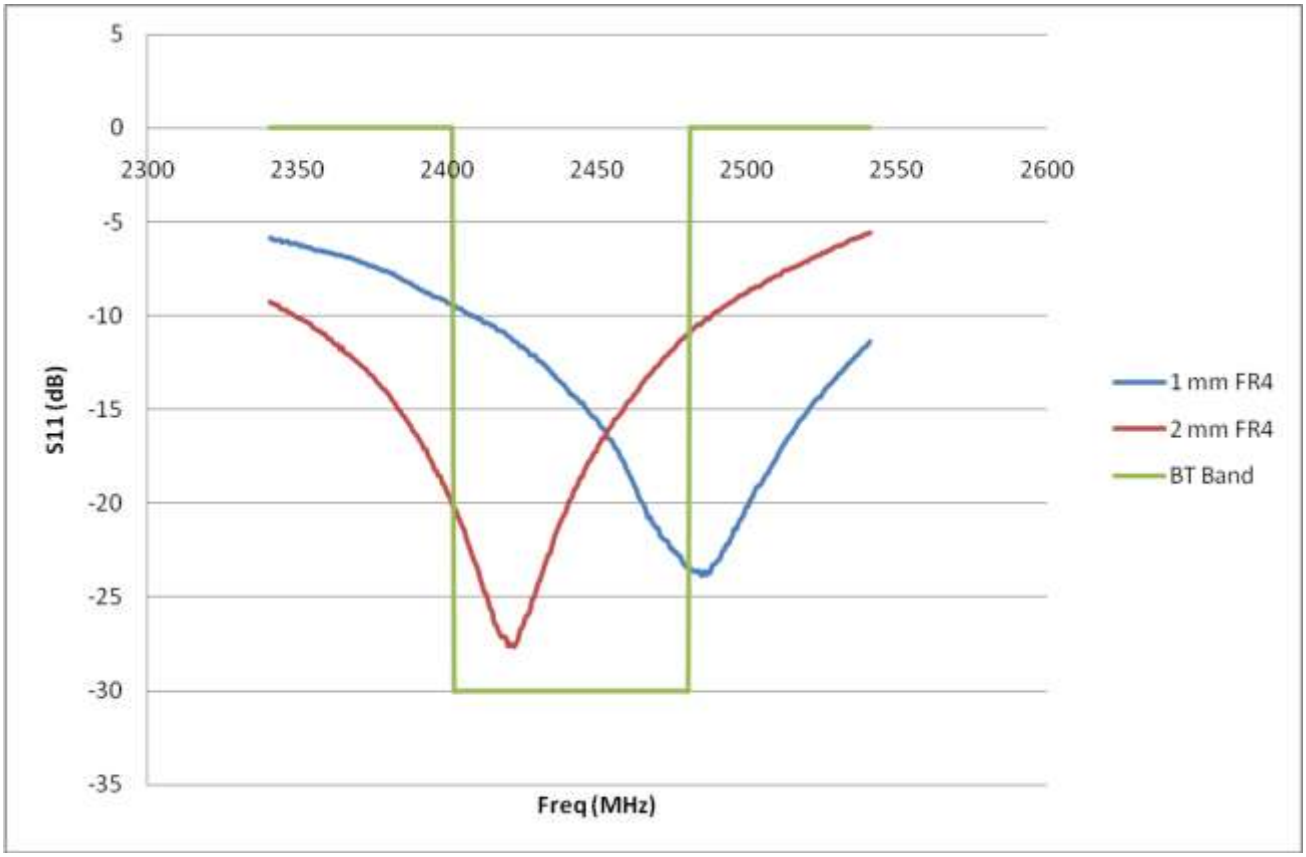

Figure 18: Typical return loss of BLE113-A with two different mother board PCB thickness

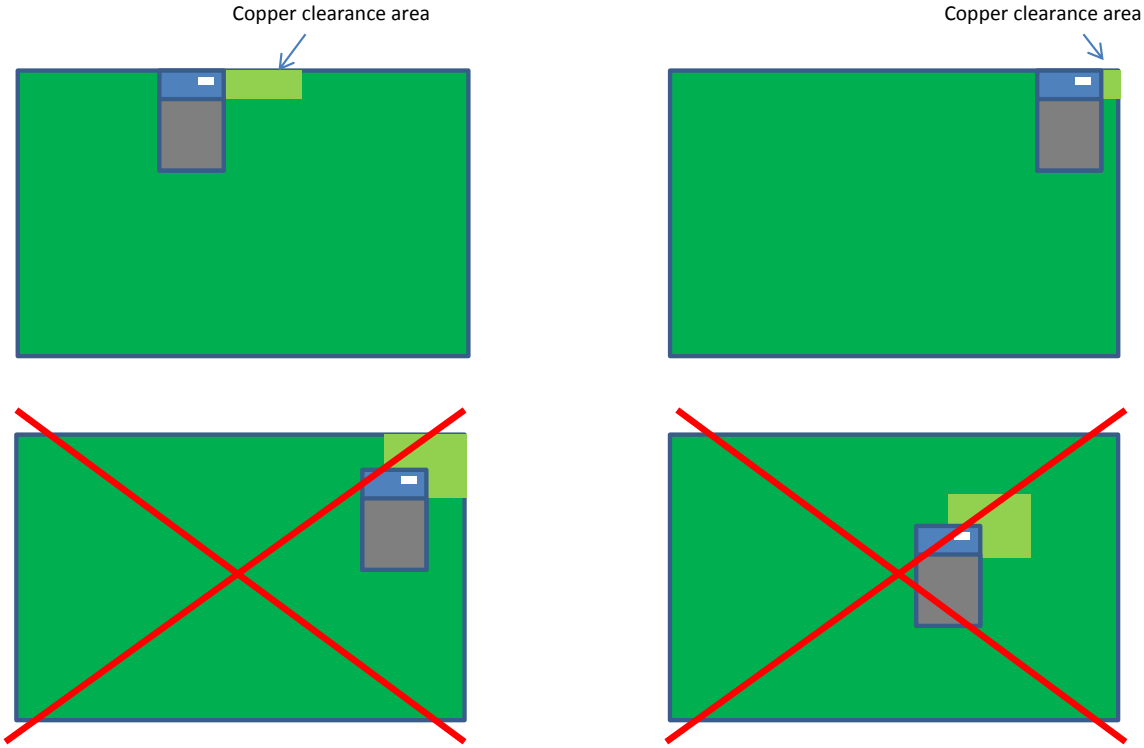

Figure 19: Example layouts for BLE113

6 Soldering Recommendations

BLE113 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Bluegiga Technologies will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for profile configurations
- Avoid using more than one flow.
- Reliability of the solder joint and self-alignment of the component are dependent on the solder volume. Minimum of 150μm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, “no clean” solder paste should be used due to low mounted height of the component.

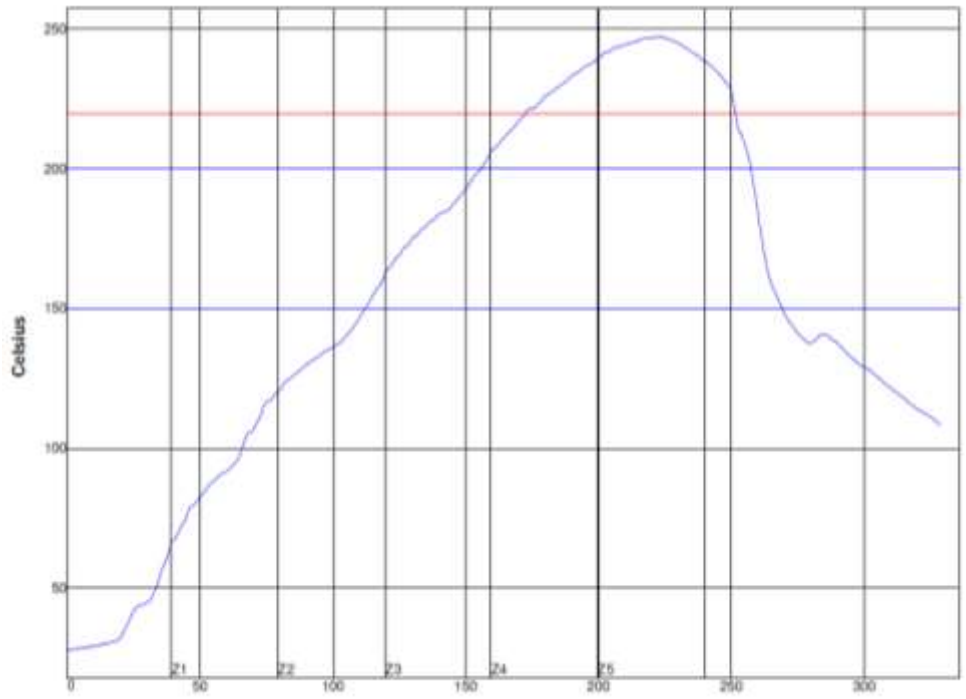

Figure 20: Reference reflow profile

7 Block diagram

BLE113 is based on TI's CC2541 chip. Embedded 32 MHz and 32.768 kHz crystals are used for clock generation. Matched balun and low pass filter provide optimal radio performance with extremely low spurious emissions. Small ceramic chip antenna gives good radiation efficiency even when the module is used in layouts with very limited space.

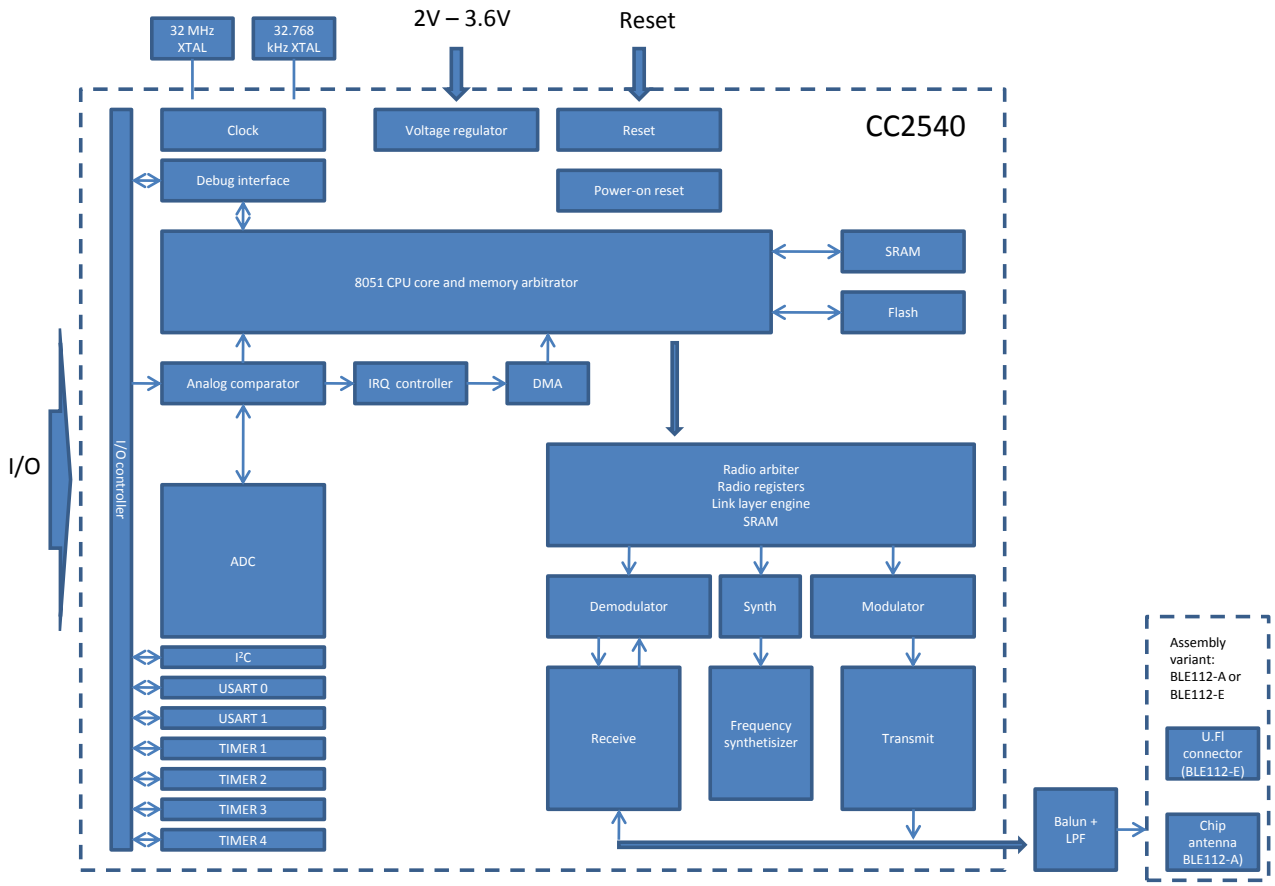

Figure 21: Simplified block diagram of BLE113

CPU and Memory

The 8051 CPU core is a single-cycle 8051-compatible core. It has three different memory access buses (SFR, DATA, and CODE/XDATA), a debug interface, and an 18-input extended interrupt unit.

The memory arbiter is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The SFR bus is a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The 8-KB SRAM maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The 128/256 KB flash block provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a flash controller that allows page-wise erasure and 4-bytewise programming.

A versatile five-channel DMA controller is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2541 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specification.

The interrupt controller services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2541 back to the active mode.

The debug interface implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The I/O controller is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The sleep timer is an ultra low power timer that uses an external 32.768-kHz crystal oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to exit power modes 1 or 2.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer used by the *Bluetooth* low energy stack. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit timer-compare registers and two 24-bit overflow-compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers

free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The AES encryption/decryption core allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The ADC supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The I^2C module provides a digital peripheral connection with two pins and supports both master and slave operation. I^2C support is compliant with the NXP I2C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit device addressing modes are supported, as well as master and slave modes..

The ultralow-power analog comparator enables applications to wake up from PM2 or PM3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

RF front end

RF front end includes combined matched balun and low pass filter, and ceramic chip antenna with matching network. Optimal matching combined with effective low pass filter provides extremely low in-band spurious emissions and harmonics.

8 Certifications

BLE113 is compliant to the following specifications.

8.1 Bluetooth

BLE113 is BT qualified as a controller subsystem. As a controller subsystem the module can be used as such with a Host Subsystem to make a Bluetooth end product without additional qualification or QDID. The Bluetooth QDID of BLE13 is B021015. The Bluetooth listing can be vied from the link below.

https://www.bluetooth.org/tpg/QLI_viewQDL.cfm?qid=21015

8.2 FCC and IC

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) this device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation.

Any changes or modifications not expressly approved by Bluegiga Technologies could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance. This transmitter meets both portable and mobile limits as demonstrated in the RF Exposure Analysis. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

IC Statements:

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

OEM Responsibilities to comply with FCC and Industry Canada Regulations

The BLE113 module has been certified for integration into products only by OEM integrators under the following condition:

- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

As long as the two condition above is met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions cannot be met (for certain configurations or co-location with another transmitter), then the FCC and Industry Canada authorizations are no longer considered valid and the FCC ID and IC Certification Number cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC and Industry Canada authorization.

End Product Labeling

The BLE113 module is labeled with its own FCC ID and IC Certification Number. If the FCC ID and IC Certification Number are not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"**Contains Transmitter Module FCC ID: QOQBLE113**"

"**Contains Transmitter Module IC: 5123A-BGTBLE113**"

or

"**Contains FCC ID: QOQBLE113**"

"**Contains IC: 5123A-BGTBLE113**"

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end product.

8.2.1 FCC et IC

Déclaration d'IC :

Ce dispositif est conforme aux normes RSS exemptes de licence d'Industrie Canada. Son fonctionnement est assujetti aux deux conditions suivantes : (1) ce dispositif ne doit pas provoquer de perturbation et (2) ce dispositif doit accepter toute perturbation, y compris les perturbations qui peuvent entraîner un fonctionnement non désiré du dispositif.

Selon les réglementations d'Industrie Canada, cet émetteur radio ne doit fonctionner qu'avec une antenne d'une typologie spécifique et d'un gain maximum (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Pour réduire les éventuelles perturbations radioélectriques nuisibles à d'autres utilisateurs, le type d'antenne et son gain doivent être choisis de manière à ce que la puissance isotrope rayonnée équivalente (P.I.R.E.) n'excède pas les valeurs nécessaires pour obtenir une communication convenable.

Responsabilités des OEM quant à la conformité avec les réglementations de FCC et d'Industrie Canada

Les modules BLE113 ont été certifiés pour entrer dans la fabrication de produits exclusivement réalisés par des intégrateurs dans les conditions suivantes :

- Le module transmetteur ne doit pas être installé ou utilisé en concomitance avec une autre antenne ou un autre transmetteur.

Tant que ces deux conditions sont réunies, il n'est pas nécessaire de procéder à des tests supplémentaires sur le transmetteur. Cependant, l'intégrateur est responsable des tests effectués sur le produit final afin de se mettre en conformité avec d'éventuelles exigences complémentaires lorsque le module est installé (exemple : émissions provenant d'appareils numériques, exigences vis-à-vis de périphériques informatiques, etc.)

REMARQUE IMPORTANTE : En cas d'inobservance de ces conditions (en ce qui concerne certaines configurations ou l'emplacement du dispositif à proximité d'un autre émetteur), les autorisations de FCC et d'Industrie Canada ne seront plus considérées valables et l'identification de FCC et le numéro de certification d'IC ne pourront pas être utilisés sur le produit final. Dans ces cas, l'intégrateur OEM sera chargé d'évaluer à nouveau le produit final (y compris l'émetteur) et d'obtenir une autorisation indépendante de FCC et d'Industrie Canada.

Étiquetage du produit final

Le module BLE113 est étiqueté avec sa propre identification FCC et son propre numéro de certification IC. Si l'identification FCC et le numéro de certification IC ne sont pas visibles lorsque le module est installé à l'intérieur d'un autre dispositif, la partie externe du dispositif dans lequel le module est installé devra également présenter une étiquette faisant référence au module inclus. Dans ce cas, le produit final devra être étiqueté sur une zone visible avec les informations suivantes :

« Contient module émetteur identification FCC : QOQBLE113 »

« Contient module émetteur IC : 5123A-BGTBLE113 »

ou

« Contient identification FCC : QOQBLE113 »

« Contient IC : 5123A-BGTBLE113 »

Dans le guide d'utilisation du produit final, l'intégrateur OEM doit s'abstenir de fournir des informations à l'utilisateur final portant sur les procédures à suivre pour installer ou retirer ce module RF ou pour changer les paramètres RF.

8.3 CE

The official R&TTE DoC is available at www.bluegiga.com

8.4 MIC Japan

BLE113 is certified as a module with type certification number 007-AB0103. As a certified module BLE113 can be integrated to an end product without a need for additional MIC Japan certification of the end product.

8.5 KCC (Korea)

BLE113 has type certification in Korea with certification number KCC-CRM-BGT-BLE113.

9 Contact Information

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