



1. Description

1.1. Project

Project Name	chalupa
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	11/21/2022

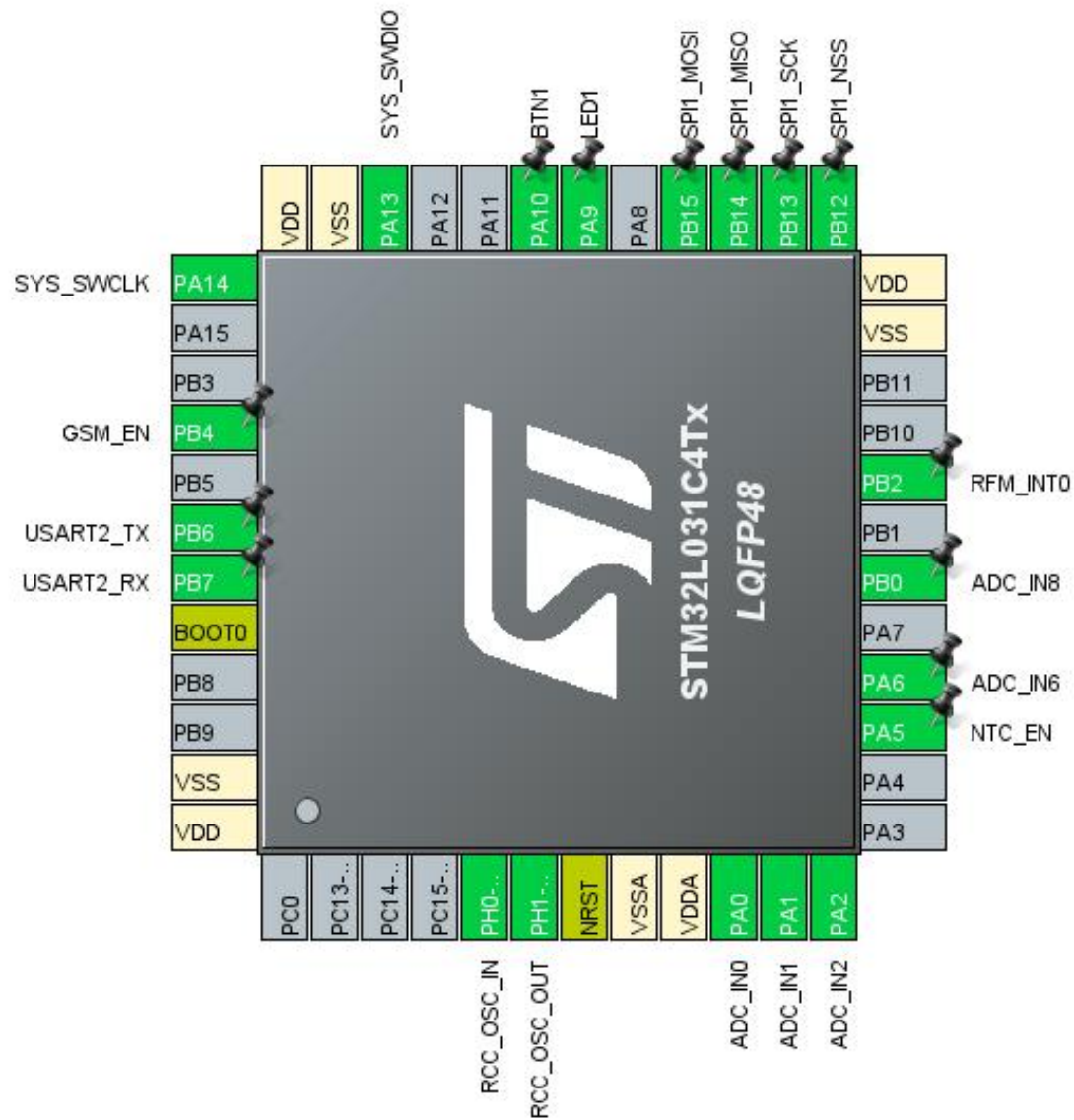
1.2. MCU

MCU Series	STM32L0
MCU Line	STM32L0x1
MCU name	STM32L031C4Tx
MCU Package	LQFP48
MCU Pin number	48

1.3. Core(s) information

Core(s)	Arm Cortex-M0+
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2. Pinout Configuration



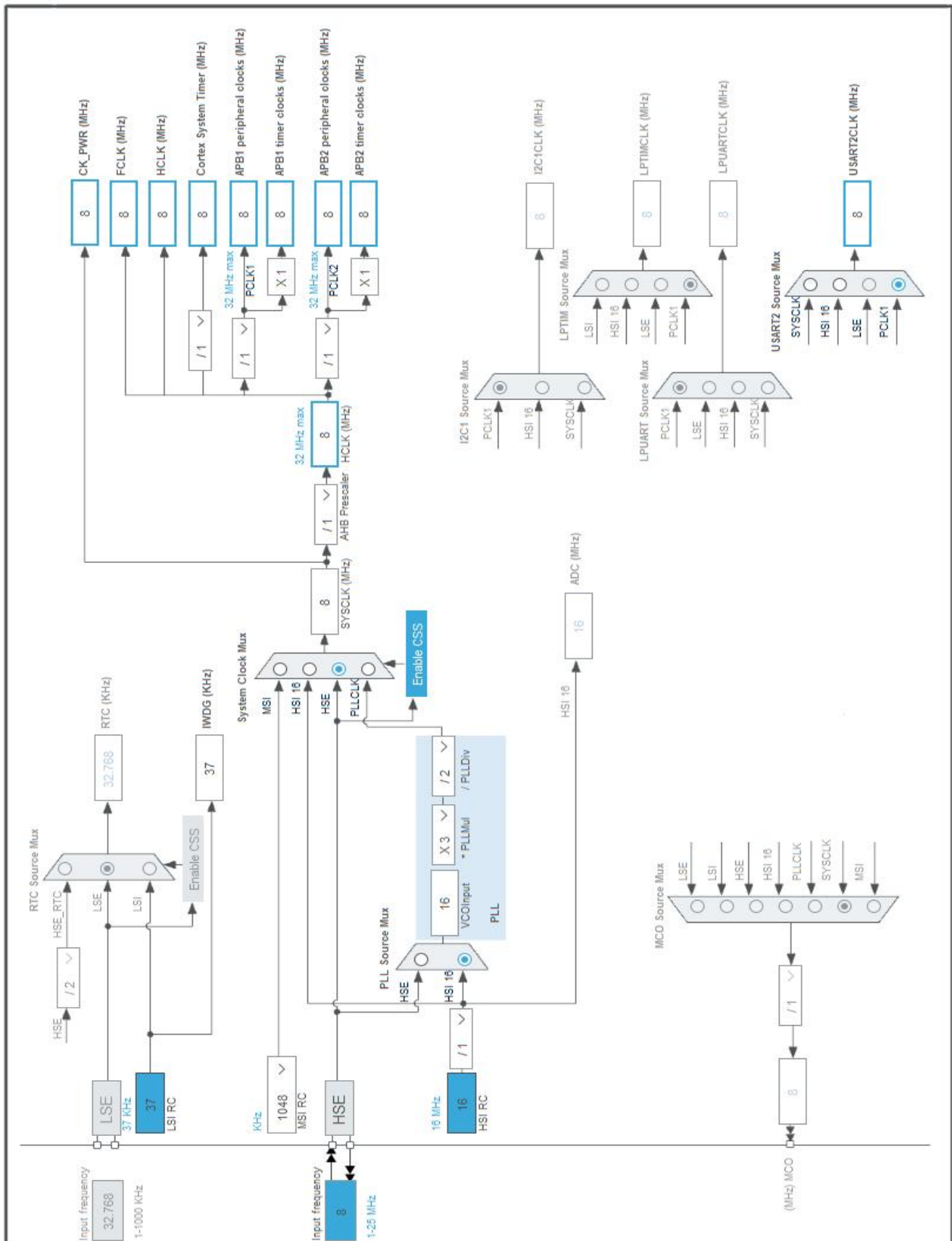
(Rotated -90°)

3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0	I/O	ADC_IN0	
11	PA1	I/O	ADC_IN1	
12	PA2	I/O	ADC_IN2	
15	PA5 *	I/O	GPIO_Output	NTC_EN
16	PA6	I/O	ADC_IN6	
18	PB0	I/O	ADC_IN8	
20	PB2	I/O	GPIO_EXTI2	RFM_INT0
23	VSS	Power		
24	VDD	Power		
25	PB12 *	I/O	GPIO_Output	SPI1_NSS
26	PB13	I/O	SPI1_SCK	
27	PB14	I/O	SPI1_MISO	
28	PB15	I/O	SPI1_MOSI	
30	PA9 *	I/O	GPIO_Output	LED1
31	PA10 *	I/O	GPIO_Input	BTN1
34	PA13	I/O	SYS_SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_SWCLK	
40	PB4 *	I/O	GPIO_Output	GSM_EN
42	PB6	I/O	USART2_TX	
43	PB7	I/O	USART2_RX	
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	chalupa
Project Folder	D:\projects\archiv\chalupa\chalupa
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L0 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC_Init	ADC
4	MX_USART2_UART_Init	USART2
5	MX_SPI1_Init	SPI1
6	MX_IWDG_Init	IWDG

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L0
Line	STM32L0x1
MCU	STM32L031C4Tx
Datasheet	DS10668_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(AAA700)
Capacity	700.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	10.0 mA
Max Pulse Current	30.0 mA
Cells in series	1
Cells in parallel	1

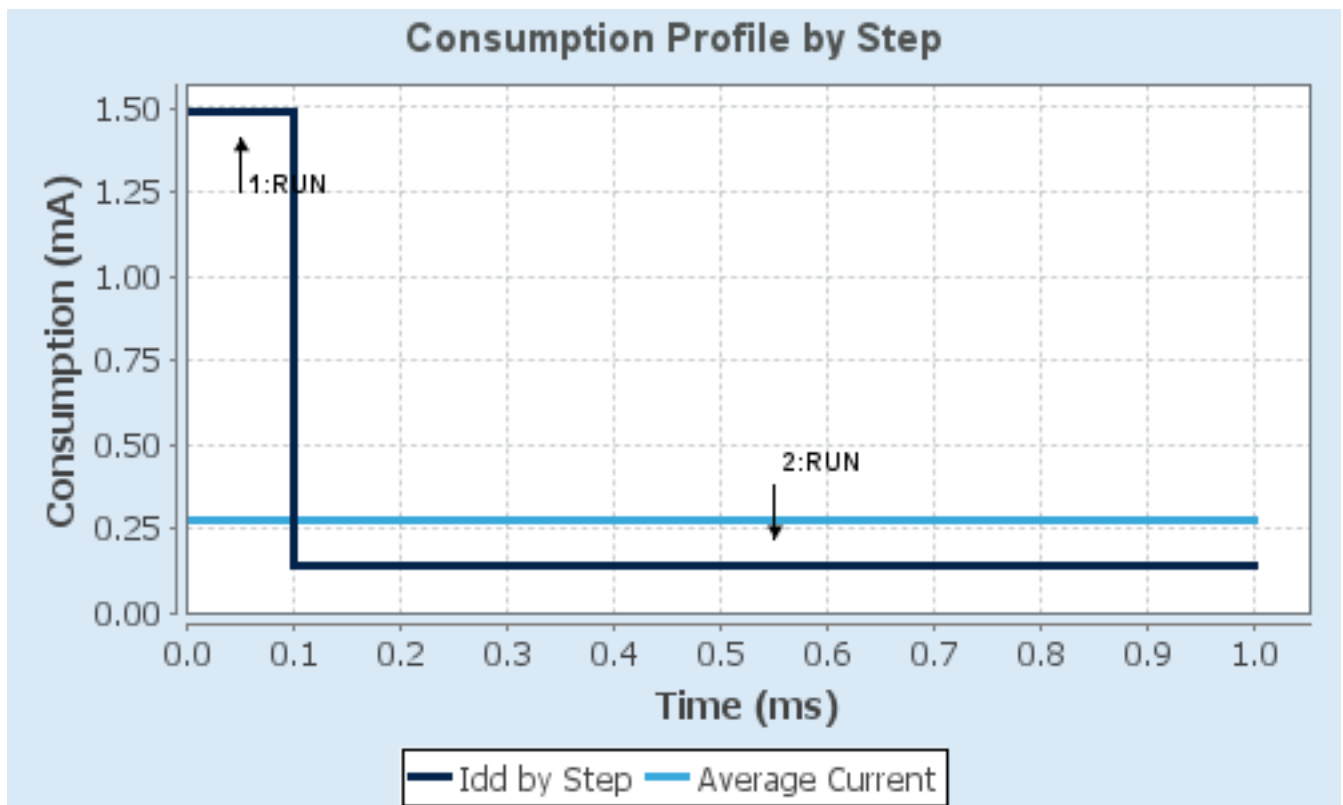
6.4. Sequence

Step	Step1	Step2
Mode	RUN	RUN
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range2-Medium	Range3-Low
Fetch Type	FLASH	FLASH
CPU Frequency	8 MHz	1 MHz
Clock Configuration	HSEBYP	HSEBYP
Clock Source Frequency	8 MHz	1 MHz
Peripherals	ADC:fs_10_ksps FLASH GPIOA GPIOB GPIOC GPIOH I2C1 IWDG PWR SYS USART2	
Additional Cons.	0 mA	0 mA
Average Current	1.49 mA	140 μ A
Duration	0.1 ms	0.9 ms
DMIPS	7.6	0.95
Ta Max	104.75	104.98
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	275 μ A
Battery Life	3 months, 14 days, 12 hours	Average DMIPS	1.615 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC

mode: IN0

mode: IN1

mode: IN2

mode: IN6

mode: IN8

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Synchronous clock mode divided by 1
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Direction	Forward
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of sequence of conversion *
Overrun behaviour	Overrun data overwritten *
Low Power Auto Wait	Disabled
Low Frequency Mode	Disabled
Auto Off	Disabled
Oversampling Mode	Enabled *
Right Bit Shift	4 bit shift *
Ratio	Oversampling ratio 16x *
Triggered Mode	Single trigger

ADC_Regular_ConversionMode:

Sampling Time	160.5 Cycles *
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false
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7.2. IWDG

mode: Activated

7.2.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	64 *
IWDG window value	4095
IWDG down-counter reload value	4095

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3 *
Buffer Cache	Enabled
Prefetch	Disabled
Preread	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 2 *
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7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	16 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	4 *
Baud Rate	2.0 MBits/s *
Clock Polarity (CPOL)	Low

Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled
NSS Signal Type Software

7.5. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

7.6. USART2

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate **19200 ***
Word Length 8 Bits (including Parity)
Parity None
Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit
Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable
TX Pin Active Level Inversion Disable
RX Pin Active Level Inversion Disable
Data Inversion Disable
TX and RX Pins Swapping Disable
Overrun Enable
DMA on RX Error Enable
MSB First Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PA0	ADC_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PB0	ADC_IN8	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB13	SPI1_SCK	Alternate Function Push Pull	Pull-down *	Very High *	
	PB14	SPI1_MISO	Alternate Function Push Pull	Pull-down *	Very High *	
	PB15	SPI1_MOSI	Alternate Function Push Pull	Pull-down *	Very High *	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
USART2	PB6	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB7	USART2_RX	Alternate Function Push Pull	Pull-down *	Very High *	
GPIO	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NTC_EN
	PB2	GPIO_EXTI2	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	RFM_INT0
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Very High *	SPI1_NSS
	PA9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA10	GPIO_Input	Input mode	Pull-up *	n/a	BTN1
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GSM_EN

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable Interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line 2 and line 3 interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash and EEPROM global interrupt	unused		
RCC global interrupt	unused		
ADC, COMP1 and COMP2 interrupts (COMP interrupts through EXTI lines 21 and 22)	unused		
SPI1 global interrupt	unused		
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable Interrupt	false	true	false
Hard fault interrupt	false	true	false
System service call via SWI instruction	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line 2 and line 3 interrupts	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware				
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System Core	Analog	Timers	Connectivity	Computing
DMA	ADC		SPI1	
GPIO			USART2	
IWDG				
IVIC				
RCC				
SYS				

10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00140359.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00108282.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00104451.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00182885.pdf
Application note	http://www.st.com/resource/en/application_note/CD00160362.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00085385.pdf
Application note	http://www.st.com/resource/en/application_note/DM00087593.pdf
Application note	http://www.st.com/resource/en/application_note/DM00108286.pdf
Application note	http://www.st.com/resource/en/application_note/DM00112257.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00145318.pdf
Application note	http://www.st.com/resource/en/application_note/DM00150423.pdf
Application note	http://www.st.com/resource/en/application_note/DM00151811.pdf
Application note	http://www.st.com/resource/en/application_note/DM00158601.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00206898.pdf

Application note http://www.st.com/resource/en/application_note/DM00209725.pdf

Application note http://www.st.com/resource/en/application_note/DM00209768.pdf

Application note http://www.st.com/resource/en/application_note/DM00209772.pdf

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Application note http://www.st.com/resource/en/application_note/DM00226326.pdf

Application note http://www.st.com/resource/en/application_note/DM00236305.pdf

Application note http://www.st.com/resource/en/application_note/DM00257177.pdf

Application note http://www.st.com/resource/en/application_note/DM00260952.pdf

Application note http://www.st.com/resource/en/application_note/DM00272912.pdf

Application note http://www.st.com/resource/en/application_note/DM00315319.pdf

Application note http://www.st.com/resource/en/application_note/DM00327191.pdf

Application note http://www.st.com/resource/en/application_note/DM00354244.pdf

Application note http://www.st.com/resource/en/application_note/DM00355687.pdf

Application note http://www.st.com/resource/en/application_note/DM00380469.pdf

Application note http://www.st.com/resource/en/application_note/DM00395696.pdf

Application note http://www.st.com/resource/en/application_note/DM00436604.pdf

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Application note http://www.st.com/resource/en/application_note/DM00660597.pdf

Application note http://www.st.com/resource/en/application_note/DM00725181.pdf