22.02.2017

EE540 Spring 2017, Assignment1, Due 6.3.2017

For all the gates and circuit blocks requested in this homework, write Verilog modules saved in *.v files. Simulate each Verilog module with all possible inputs in ISim using both a testbench file and a tcl file to verify correct functionality. In a testbench file for a module called XYZ, you will write a file named testXYZ.v containing a module named testXYZ that instantiates the module XYZ as design under test (DUT). In the tcl file, input signals of the module must be forced to take different logic values at different time points.

1. Write and simulate Verilog modules for the simple gates below:

a) Inverter (t_{plh}=2ns, t_{phl}=1ns)

b) NAND (t_{plh}=t_{phl}=2ns)

c) NOR (t_{plh}=3ns, t_{phl}=2ns)

d) XOR (t_{plh}=t_{phl}=5ns)

2. Using the simple gates described in 1, write and simulate a Verilog module for the circuits below. Draw the schematic of the circuits in terms of the gates you used:

a) 1-bit full adder

b) 1-bit 2-input multiplexer (MUX2)

3. Using the MUX2 described in 2, write and simulate a Verilog module for a 32-bit MUX2. (Hint: Create mux component instances using GENERATE statement.)

4. a) Using only the NAND gate described in 1, write and simulate a Verilog module for a positive-level D latch (Dlatch.v) and a negative-level D latch (DNlatch.v) in structural style. Draw the schematic of the Dlatch and DNlatch you have described.

b) Repeat (a) using only the NOR gate described in 1. Compare your results against the latches in (a) and comment on the differences if any.

5. Using the gates you have described so far, write and simulate a Verilog module in structural style for a positive edge-triggered, asynchronously resetable D flip-flop (DFF). Draw the schematic of the DFF you have described.

6. Using the DFF module described in 5, write and simulate a Verilog module in structural style for a 32-bit register. (Hint: Create flip-flop component instances using GENERATE statement.)

7. Write and simulate a UDP file for a 4-input MUX. Consider the possibility of unknown inputs as well.

Deliverables

Your reports should include snapshots for all simulation results, a summary of the synthesis results, schematics of the synthesized circuits, and your comments. Important considerations that went into the design, and extra features, if any, should also be documented. Your reports should not contain your Verilog codes, which will be submitted as individual files. Before emailing your homework, zip all relevant Verilog files including testbenches, tcl files, synthesis output files, and your report under a folder named as: *hw1_yourlastname_yourfirstname*.