LOW COST PACKET RADIO - ADVANCED TECHNOLOGY FOR PACKET RADIO SWITCHING APPLICATIONS

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ABSTRACT

The Low Cost Packet Radio (LPR) is a packet radio unit with low cost, low weight, low volume, and low power. It is to be used in support of experiments with large packet radio networks. The LPR incorporates a digitally controlled, direct sequence, minimum shift keyed, spread spectrum radio and a microprocessor-based packet switch. Code changeable surface acoustic wave matched filtering provides processing gain at burst symbol rates of 100 and 400 kilo symbols per second in the presence of interference. Coherent recursive integration enhances synchronization performance, provides synchronous detection of the data, and serves the adaptive multipath accumulator. Forward error correction (FEC) utilizing convolutional encoding and sequential decoding is incorporated at four different code rates for both burst symbol rates. The microprocessor runs the networking software. Requirements and design information for the LPR are presented in addition to performance data taken on several developmental units. The repeatability of the data taken on the units is demonstrated.

1 INTRODUCTION

The Low Cost Packet Radio (LPR) is the current generation packet radio supporting the development and evaluation of advanced packet networking concepts, techniques, and protocols.[1]

The LPR is a digitally controlled half-duplex spread spectrum radio and a microprocessor acting as a packet switch. The requirements placed on the design and development of the LPR are oriented toward its intended use: a radio to support large test beds for research and development on radio-based store and forward packet switching networks.

The LPR comprises radio frequency (RF) transmission and reception capabilities and a programmable digital processor, which together provide the functionality of the lower three levels of the International Standards Organization (ISO) Open System Interconnection Reference Model, viz, the physical, link, and network layers. This paper describes the hardware implementation of the LPR and compares its expected performance to measured performance on several development models.

2 LPR DESIGN DESCRIPTION

The LPR, nomenclatured the AN/PRC-118( ), is currently in limited production for experimental use. Figure 1 shows the completed development model with the size, weight, and power consumption achieved.

The LPR is functionally divided into two sections, the radio section and the microprocessor section (figure 2). The radio section modulates and transmits, receives and demodulates, and transfers packets between the microprocessor and the channel. The major performance goals for the LPR, enumerated below, are specified for a line-of-sight communications range of 10 km in a rural environment with rolling hills 15 to 45 meters high.

Probability of correct packet detection	$\geq$ 95%
Probability of false packet detection	$\leq 10^{-6}$
Undetected bit error rate (CRC)	$\leq 10^{-12}$
Bit error rate	$\leq 10^{-5}$

To support these goals, the radio operates with the RF characteristics summarized in Table I.

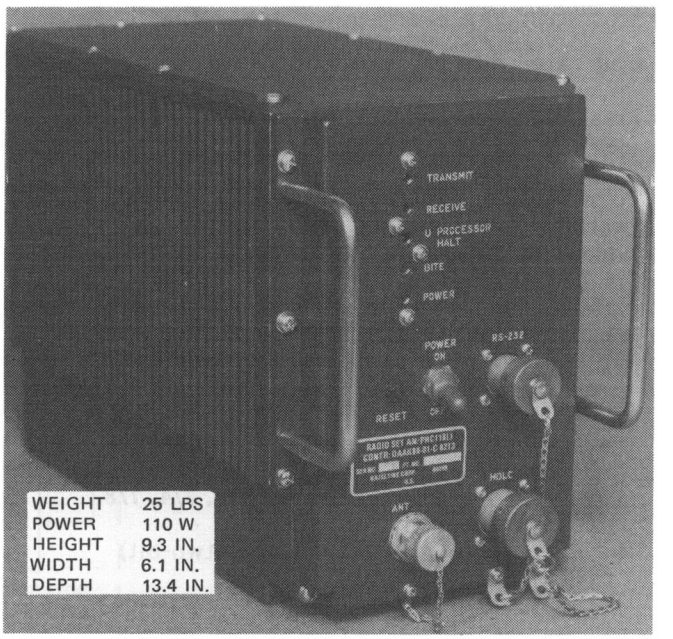

Fig. 1. The Low Cost Packet Radio

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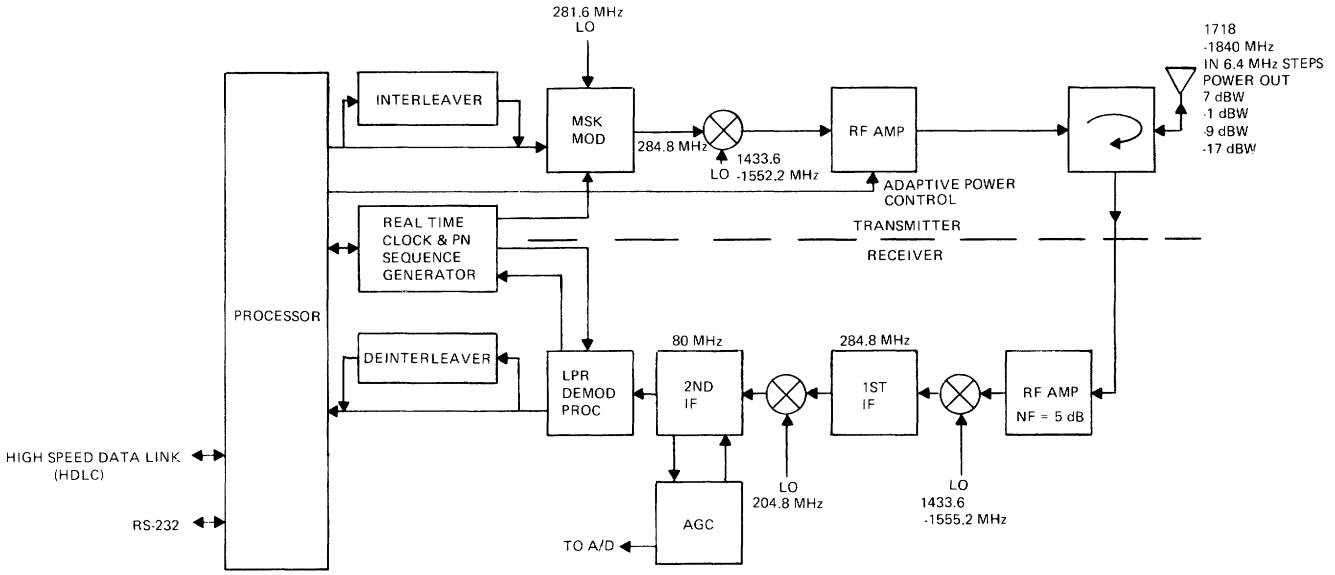

Fig. 2. LPR System Block Diagram

Table I. RF Signal Characteristics

Transmit Power	5 watts
Band of Operation	1718.4 to 1840 MHz
Number of Channels	20
Channel Separation	6.4 MHz
Channel Bandwidth	20 MHz
Modulation Type	Pseudorandom noise, direct sequence spread spectrum (DSPN)
Chip Modulation	Minimum shift keying (MSK)
Bit Modulation	Coherent phase shift keying (PSK)
Chip rate	12.8 megachips per second (MCPS)
Preamble	28 bits

To provide for experimentation in advanced networking techniques and protocols, the LPR provides flexibility with the following protocol controlled parameters.

- Alternative multiple access techniques
  - Carrier sense multiple access (CSMA)
  - Code division multiple access (CDMA)
- Convolutional encoding and sequential decoding for FEC with a choice of:
  - Variable code rates: 1/2, 3/4, 7/8, uncoded
  - Hard and soft decision (two-bit)
- Variable symbol rates
  - 100 kilo symbols per second (KSPS)
  - 400 KSPS
- 24 dB output power control selectable in 8 dB steps

2.1 LPR IMPLEMENTATION

Packets containing header and data are input to the LPR processor via (a) the wire connection to the HDLC port (data rates up to 1.544 MBS) or (b) the RF link and the LPR receiver. CRC and FEC encoding of the data is accomplished in the processor, interleaved if in an FEC mode, and added modulo 2 to the DSPN spectrum spreading code.

The combined pseudonoise (PN) sequence and data symbol phase-shift-key the 281.6 MHz LO, and the resultant signal is passed to the surface acoustic wave (SAW) filter in the MSK modulator.[2] The modulator implements the Amoroso offset filter technique[3] resulting in an MSK spread spectrum signal at an intermediate frequency (IF) of 284.8 MHz, with PSK data modulation. The MSK output signal is converted to one of 20 selectable L-band RF channels, amplified, and transmitted. The 5-watt maximum transmitter output has four selectable power levels controlled by the upper layer protocols, providing a power range of 24 dB in 8 dB steps. Both the power level and RF channel are selectable on a packet basis.

The processing yields a spreading factor (chips per symbol) of 32 for the 400 KSPS mode (2.5 μs symbol) and of 128 for the 100 KSPS mode (10 μs symbol). The PN sequences obtained from the Data

Encryption Standard (DES) algorithm of the National Bureau of Standards[4] yield codes that are random with respect to each other and mitigate against the effects of self-jamming, incidental interference, intentional jamming, and multipath fading. The 28-symbol preamble uses a repetitive 100 KSPS PN code sequence while the sequence for each data symbol varies from symbol to symbol to effect continuous code change. The symbol sequence and the PN sequence are synchronized with each other. The preamble sequence is selectable on a packet-by-packet basis.

On receive, the incoming signal is amplified, converted to the first IF of 284.8 MHz, amplified, converted to the second IF of 80 MHz, and amplified in the automatic gain controlled IF amplifier (bandwidth 12.8 MHz).

The IF output is passed to the LPR demodulator processor, detailed in figure 3. In the demodulator, the programmable SAW matched filter (MF) strips off the PN spreading sequence, leaving a compressed IF pulse that is PSK modulated by the packet symbols (preamble, header, data, etc).

2.2 LPR MATCHED FILTER AND COHERENT RECURSIVE INTEGRATOR

A block diagram of the LPR programmable matched filter implementation is shown in figure 4. A chip filter matched to an individual MSK chip (ideally one-half a cosine pulse) is followed by a tapped delay line with taps spaced at the chip duration (78.125 ns). The outputs of the taps are fed to either a plus or a minus bus according to the expected PN code, and the outputs of the two busses are subtracted to form the filter output. The matched filter is implemented using SAW techniques. Figure 5 shows a photograph of the LPR SAW matched filter. The chip filter is contained in the launching transducer, and the tap outputs are fed to an integrated circuit that routes them to the plus and minus bus according to the PN code. Each of the four integrated circuits sums 32 tap outputs. In the 128-tap mode (100 KSPS rate), the outputs of the integrated circuits are added together, while in the 32-tap mode (400 KSPS rate), the output of only the first integrated circuit is used.

The MF output is sent to both the data demodulator and, after a one-symbol delay, to the decision directed coherent recursive integrator (CRI).[5] The CRI provides enhanced carrier and multipath profile signals needed for coherent carrier demodulation in the data demodulator and, after envelope detection, for use in determining signal acquisition. The performance of these functions is enhanced through the increase in the SNR provided at the CRI output due to the coherent addition of the signal pulses. This increase depends upon the CRI loop gain, α, pulses (figure 3), and ideally equals $(1 + \alpha)\ (1 - \alpha)$. With α selected to equal 0.85, a 10.9 dB improvement in SNR is theoretically achievable. Gain variations in the loop amplifiers and ripple in the passband, in addition to the expected rate of change of the multipath profile, play major roles in limiting the maximum nominal design value for the loop gain.

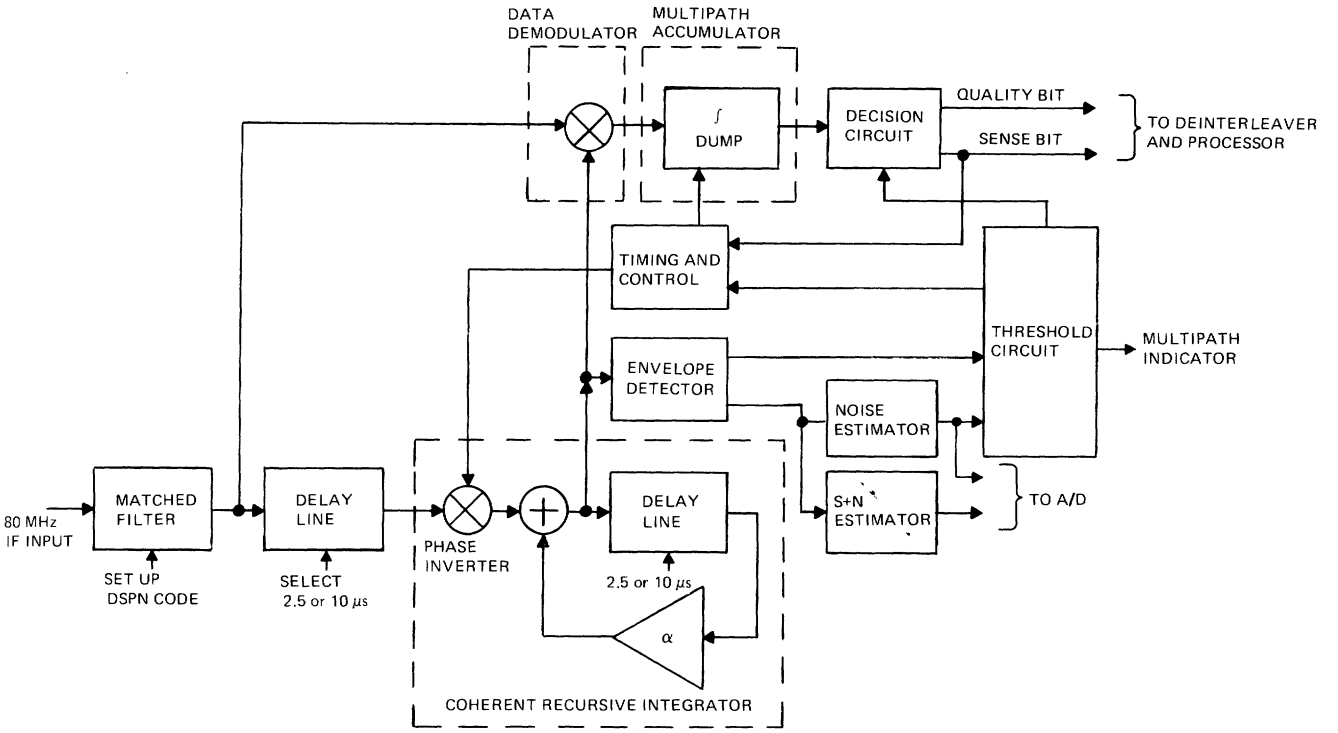

Fig. 3. LPR Demodulator

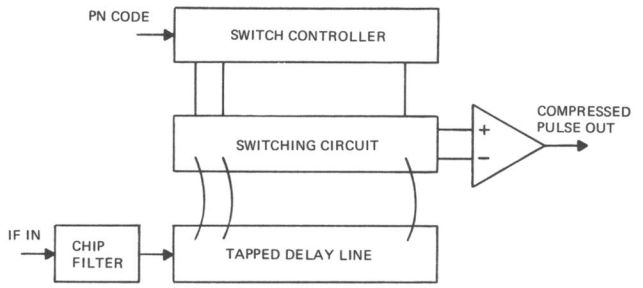

Fig. 4. Matched Filter

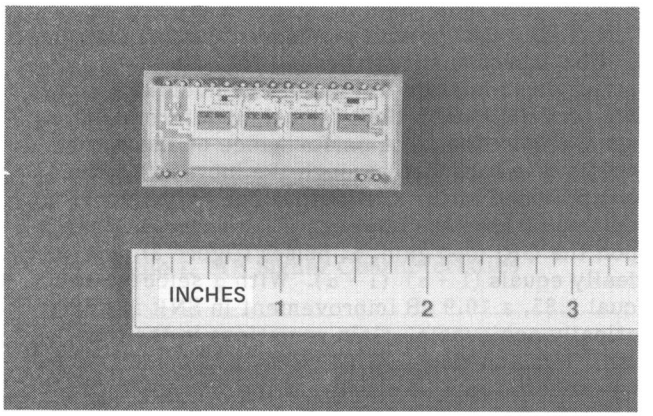

Fig. 5. LPR SAW Matched Filter

The SNR gain provided by the CRI is strongly dependent upon any residual carrier phase shift around the loop, such as caused by oscillator instability, SAW delay line length variations in manufacture, temperature effects, Doppler effects, and loop bandwidth.

The CRI loop phase is controlled over the ambient temperature range by placing the CRI ST quartz SAW delay line in a temperature-compensated package. The compensated package is stable to $\pm 10^{\circ}$C from the turnover temperature of the ST quartz substrate over an operating temperature of 0°C to 75°C. The maximum aggregate CRI loop phase error (excluding Doppler) that results under these conditions is $\pm 3^{\circ}$. This results in a decrease of SNR improvement of about 0.5 dB.

2.3 MULTIPATH ACCUMULATION AND DATA DEMODULATION

The multipath accumulation processor consists of the CRI, data demodulator, and integrate and dump circuit preceding the data decision circuit. The CRI builds up a replica of the multipath channel in amplitude and phase and is used as a coherent reference for data demodulation. In the data demodulator, the reference multiplies the output signal from the MF. The output compressed video MSK correlation pulses enable individual multipath signal components separated by approximately 1 chip, or about 78 ns to be resolved. The resulting weighted multipath components are summed in the integrate and dump circuit and passed to the decision circuit. The multiplication and integration approximate an optimum correlator to the multipath distorted input signal. This processing provides improved BER performance in a fading environment[6] for multipath spreads up to 6 µs, at the 100 KSPS rate, and about 1.6 µs, at the 400 KSPS rate.

Two bits are output from the decision circuit to the microprocessor at each decision time: a sense bit and a quality (level) bit used in the soft decision mode. The sense bit is also fed back to the phase inverter in the decision-directed CRI to provide a data free pulsed signal to the CRI. The noise estimator metric is used to set the threshold for the quality bit.[7]

2.4 TRACKING AND SYNCHRONIZATION

Once bit synchronization is obtained during the preamble, an open loop time base is set at the nominal incoming data rate to track the signal. The expected maximum packet length is less than 66 ms with ± 1/2 ppm oscillators. The maximum drift is less than one chip. To allow packet radio networks to acquire and maintain time synchronization, time transfer between packet radios is necessary. This is accomplished in the LPR by time stamping incoming packets at the radio receiver and allowing the higher layer protocols the option of transmitting a time tagged packet. Both the time tagging and the stamping functions are performed relative to the frame sync epoch. The time tag value is appended to the end of the data portion of the packet before the final CRC.

2.5 LPR PROVIDED METRICS

Upper layer protocols track radio link conditions through signal metrics provided by the LPR receiver. The available metrics are AGC control voltage, noise estimate, signal plus noise estimate, indication of multipath spread, and, when FEC is employed, a symbol error rate estimate. The smoothed AGC control voltage provides an estimate of in-band power (including signal, noise, and interference) during the packet. The noise estimate, obtained from the noise estimator after low pass filtering the envelope detected CRI output, is used to set all the threshold levels. The signal plus noise estimate provides an indication of signal strength and is obtained by peak detecting the output of the CRI. Multipath spreads greater than 1.6 µs are detected, and if present, a multipath indicator is set. The sequential decoder outputs an estimate of the number of errors corrected. This is used as a symbol error rate measurement.

The radio processing section can use the AGC voltage to determine link power variations on links that have enough received power to cause AGC attack. Power variations between different links may also be determined by their AGC readings. If

the received power on a link is too low to cause AGC attack, the signal plus noise and noise metrics may be used to give an estimate of the SNR on the link.

On links with higher powers, the signal plus noise and noise estimates will provide an estimate of the interference on the link. Since these metrics are measured at preamble time, pulse interference that occurs during the data reception time of the packet will not be measured.

2.6 LPR DIGITAL SECTION

The LPR Digital Section consists of the digital processors of the transmitter and receiver, the real-time clock, the data encryption standard (DES) pseudonoise generator, and the processor subsection.

The processor contains the hardware and software necessary to implement the link and network level protocol interpreters in the packet radio system and to interface the:

- Transmitter-receiver digital section
- High speed data interface
- Low speed data interface. (RS-232 port).

The processor is partitioned into four sections as shown in figure 6. The CPU section contains the 8086 CPU and peripherals to fulfill protocol functions, initialization, and debug/repair activities. The memory section contains 64K bytes of system ROM and 256K bytes of system RAM. The transmitter-receiver buffer section contains dual 8089 I/O processors, an A/D converter, and other peripherals that include the radio transmitter buffer, convolutional encoder/sequential decoder, CRC encoder/decoder, real-time clock/PN code generator, radio status/control registers, and subsystem RAM and ROM. The A/D converter digitizes the AGC, signal-plus-noise and noise metrics. The HDLC section contains the physical and data link layers for the serial high speed wire data port.

3 LPR PERFORMANCE

Several developmental LPRs have been built and their acquisition and data demodulation performance measured. Using the Longley-Rice model at 1.775 GHz and a range of 10 km, an available signal strength of -99 dBm is predicted.[8]

Table II presents average measured data (measurement accuracy ± 1 dB), taken on several radios. The data shows the average sensitivity signal performance for acquisition and data demodulation at various data rates and the margin relative to the calculated available received power.

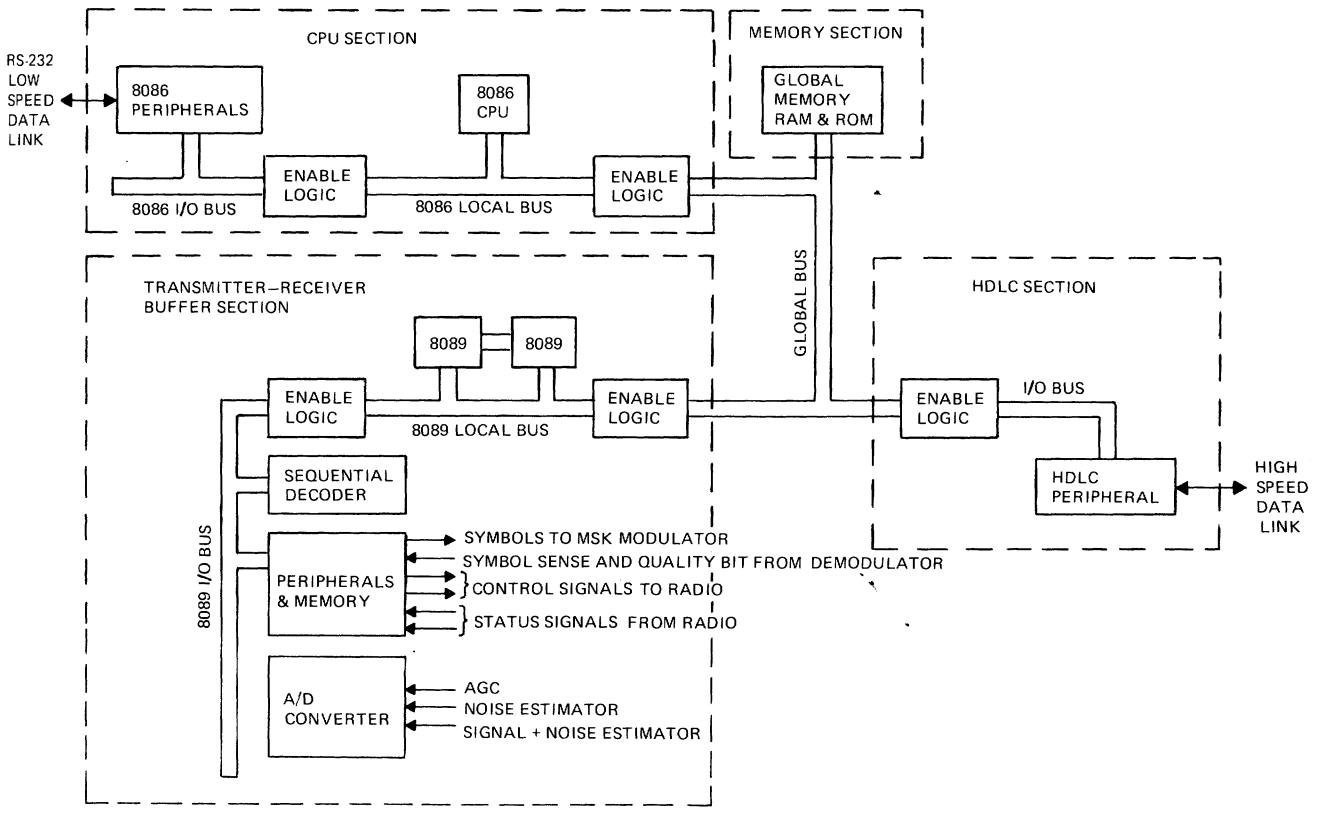

Fig. 6. LPR Microprocessor System

Table II. LPR Measured Received Signal Sensitivity Performance

Mode	Prototype Unit (dBm)	Preproduction Unit (dBm)	Margin dB (Relative to -99 dBm)
Synchronization	-109	-106	7
50 KBPS (1/2 Rate H)	-107	-108	9
75 KBPS (3/4 Rate H)	-108	-109	10
87.5 KBPS (7/8 Rate)	-106	-107	8
100 KBPS (CRC)	-104	-106	7
200 KBPS (1/2 Rate H)	-99	-99	0
300 KBPS (3/4 Rate H)	-100	-100	1
350 KBPS (7/8 Rate)	-99	-99	0
400 KBPS (CRC)	-96	-98	-1

Column 2 of Table II shows the measured minimum average power for the prototype units (discussed in reference 1) in the presence of front end noise. The third column shows the measured power needed to meet the same requirements on the first of two preproduction units. The data shows that the performance of the prototype and preproduction units are virtually the same, with the preproduction unit performing up to 2 dB better in some of the data modes. This improvement is mainly due to the use of increased isolation between the MF and CRI and the consequent reduction of spurs within the passband.

The synchronization performance of the preproduction unit is reduced by 3 dB. This is due to increasing the bit sync threshold setting, relative to that used in the prototype units, to ensure required performance at the high end of the 80 dB dynamic range (-20 dBm).

Column 4 of Table II shows the margin of the preproduction unit relative to the expected available received power.

Further tests and experimentation at the link and network levels are planned for the LPR in both medium and large scale packet-switched networks.

REFERENCES

[1] W. C. Fifer, F. J. Bruno, "The Low Cost Packet Radio", Proceedings of the IEEE, vol 75, pp 33-42, January 1987.

[2] G. Herring, P. Krencik, K. Henrich, P. Teicher, "Low Cost, Miniature Programmable SAW Matched Filter for Tactical Spread Spectrum Systems," MILCOM '83, vol 2, pp 396-401.

[3] F. Amoroso, J. Kivett, "Simplified MSK Signaling Technique," IEEE Trans-Communication April 1977, COM 25 No. 4, pp 433-441.

[4] V. Voydock, S. Kent, "Security Mechanisms in High-Level Network Protocols," ACM Computing Surveys vol 15, no. 2, pp 135-171, June 1983.

[5] M. H. Enein, "Coherent Signal Processing for Packet Radio," MILCOM '82, vol 3, pp 10.7-1--10.7-5.

[6] G. L. Turin, "Introduction to Spread Spectrum Antimultipath Techniques and Their Application to Urban Digital Radio," Proceedings of the IEEE, vol 68 No. 3, pp 328-353, March 1980.

[7] Linkabit Corporation - Private Correspondence.

[8] A. Longley, P. Rice, "Prediction of Tropospheric Radio Transmission Loss Over Irregular Terrain - A Computer Method," 1968 ESSA Tech Report ERL 79-ITS 67.