

Alexander Samoilov

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Areas of Strength Summary

CPU and GPU Architecture	deep knowledge of modern CPU architecture, caches, principles of memory organization acquired at the position of performance architect at NVidia while conducting performance analysis of High Performance Computing applications for various scientific areas such as Computational Fluid Dynamics, Quantum Chemistry, Molecular Dynamics.
Solid mathematical background	experience in prototyping complex physical design concepts in particular for Electronic Design Automation thus connecting theoretical mathematical physics concepts with practical physical problems.

Education

'1982 – '1987 **Moscow State University, Department of Mathematics and Mechanics**, Moscow.
Chair specialization: Gas and Wave Dynamics.
Grades *95%* Overall

Experience

September '16 – Present **Software Engineer for Embedded Linux Solutions on NVIDIA Jetson TX1 for Ultra-Precise 3D Scanners, Artec 3D** <https://www.artec3d.com>, Moscow, handheld 3D scanners.
state of the art programming for embedded Linux on ARM/GPU supercomputer NVIDIA Jetson TX1 for Ultra-Precise 3D scanners produced by Artec 3D. Programming languages for development: C++14, Python and **Rust**. for more details see the blog *NVIDIA Jetson Enables Artec 3D, Live Planet to Create VR Content in Real Time*

June '15 – August '16 **Software Development Engineer; Sr. Software Development Engineer from September '15, Mentor Graphics** www.mentor.com, Moscow.
Sr. Software Development Engineer for **Calibre Computational Lithography**

December '14 – **Principal Engineer for Advanced Projects, Huawei Corp**
 – June '15 <http://www.huawei.com>, Moscow.
 projects for Domain-Specific Languages for GPU programming based on:
Delite - stanford-ppl.github.io/Delite
Scalan - <https://github.com/scalan>

July 2010 – **Performance Architect, NVidia** www.nvidia.com, Moscow.
 December '14 – Worked on performance simulators for future GPU architectures.
 4.5 years – GPU architectures study and writing codes for simulating virtual memory
 – TLB cache study.
 Performance study of High-Performance Computing applications for
 Computational Fluid Dynamics, Quantum Physics, Molecular Dynamics.

April 2007 – **Sr. Software Engineer, Cadence Design Systems**
 June 2010 www.cadence.com, Moscow.
 3 years, 3 months – Support and development for Cadence products for Electronic Design
 Automation of VLSI.
 Some projects:
QCAP support - Cadence product tool for RC parasitic extraction. Bug
 fixing and further development to support *FINFET* technology process.
SNASND acceleration - a tool for substrate noise analysis was accelerated
 in more than 50 times by improving algorithm for solving large sparse
 matrices. The result was reported on TECCI 2009 conference.
Electrostatic BEM/FEM field solvers - tuned SVD low-rank matrices
 approximation approach for achieving acceleration without loss of precision.

August 2003 – **Sr. CAD Engineer, Intel Corp.** <http://www.intel.com>, Moscow.
 March 2007 – Research worker for Strategic CAD Labs.
 3.5 years – Experimental flow for future processor design technologies.
 Some of the projects:
Timing-Driven Routing - participated in the project led by Dr. Priyadarsan
 Patra.
 Honored for the project.
Dynamic power estimation - proposed original approach using Bayesian
 Nets for estimating switching activity.

Skills

CPU and GPU Architecture deep knowledge of modern CPU architecture, especially NVidia GPUs,
 modern pipeline architectures, caches, TLBs

Algorithms: numeric and for discrete optimization mastered in modern algorithms including NP-hard, graduated from
 Coursera course for discrete optimization, have experience in imple-
 menting numerical algorithms for Computational Fluid Dynamics in-
 cluding porting to parallel architectures.

Programming Preferred: C, C++, Scala, Fortran, Bash, Python, Perl, **CUDA**, MPI

Exposure: Haskell, Rust

Tools Linux, Emacs, Eclipse, IntelliJ, Ant, Ivy, Maven, Autotools, CMake, Make, Git, Subversion, Perforce

Languages Russian (Native), English (fluent)

Interests

Books

Traveling