



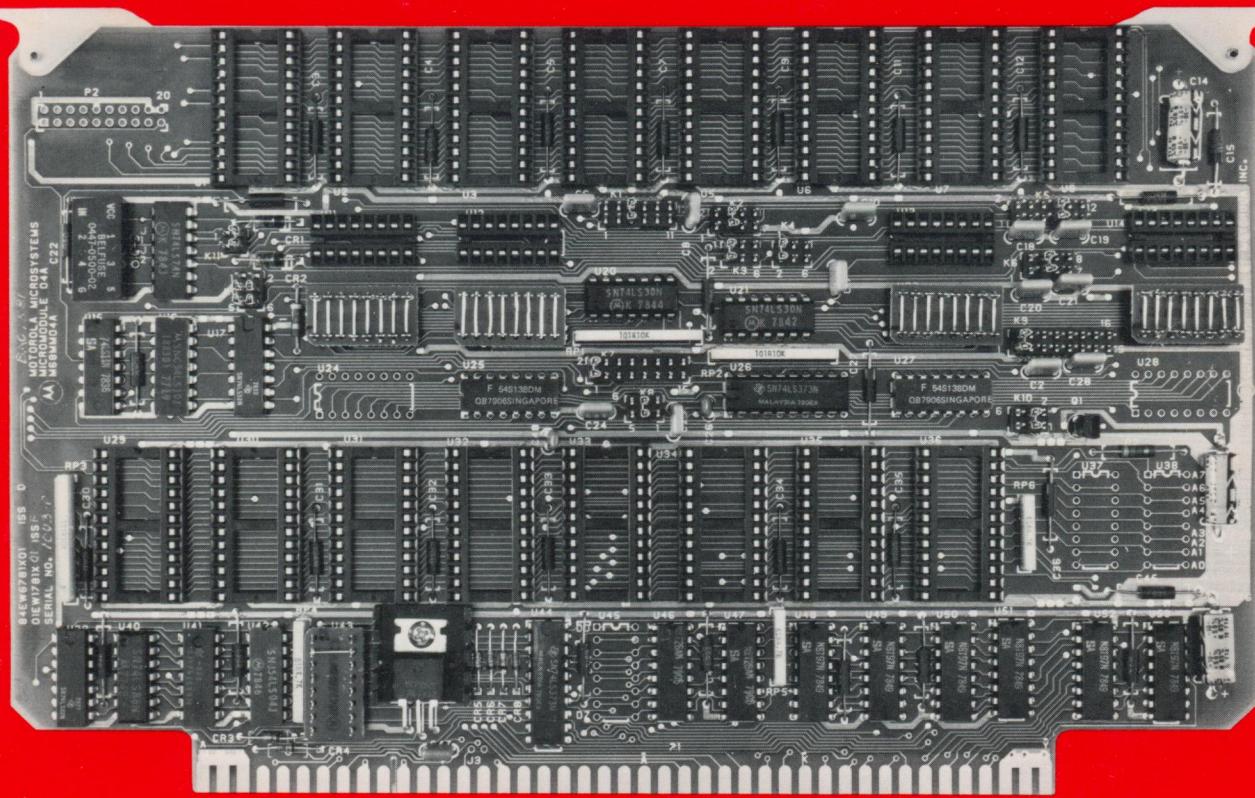
MOTOROLA

M68MM04A(D2)

M68MM04A

ROM/EPROM Module

Micromodule 4A



MICROSYSTEMS



M68MM04A(D2)

DECEMBER 1980

M68MM04A

ROM/EPROM MODULE

MICROMODULE 4A

USER'S GUIDE

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Second Edition

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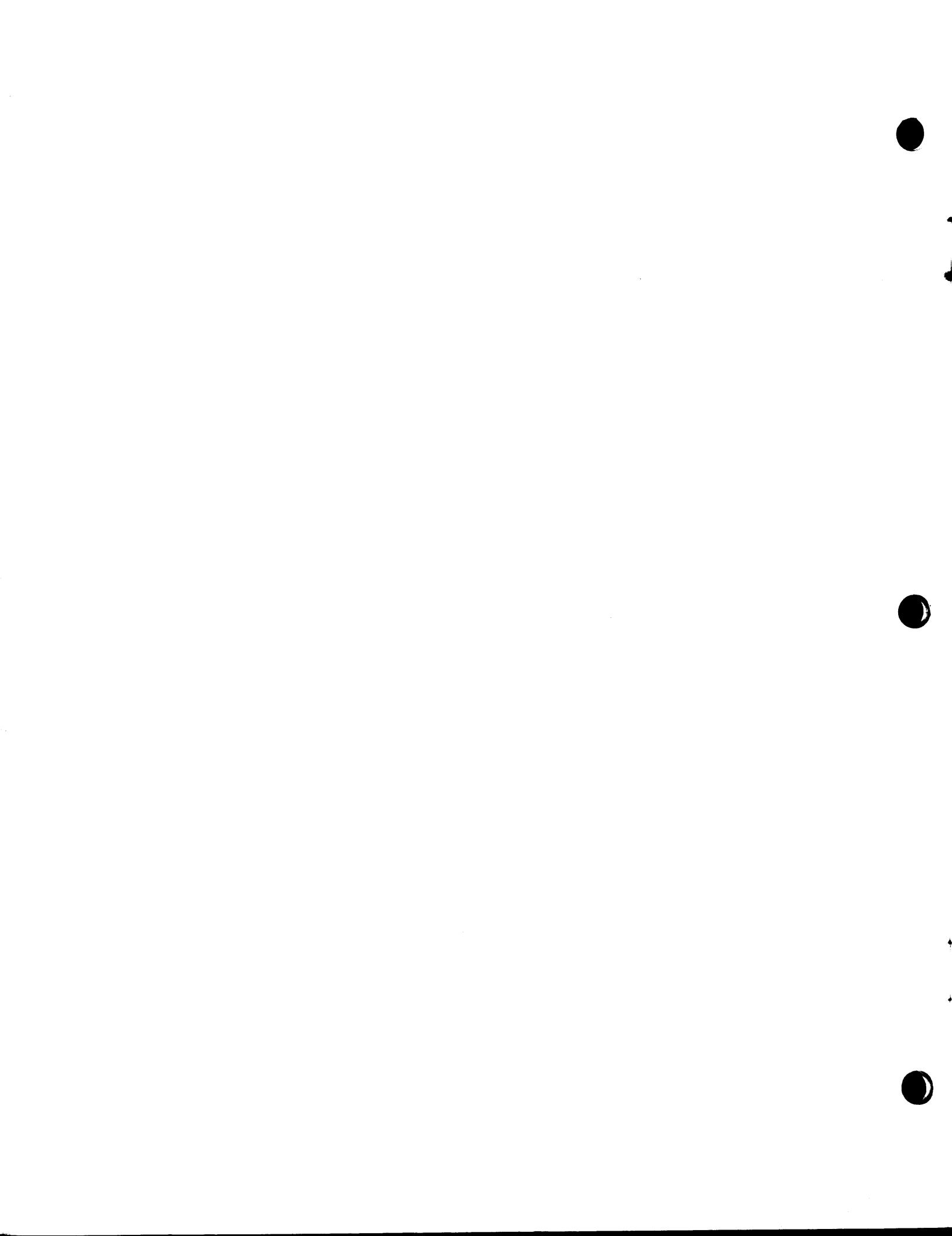
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CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

Micromodule 4A (M68MM04A), as shown in Figure 1-1, is a ROM/EPROM board. It has been designed to accommodate most of the 24-pin 1K, 2K, and 4K x 8-bit parts currently on the market. All address references in this manual are shown in hexadecimal, unless otherwise indicated.

1.2 FEATURES

The features of Micromodule 4A include:

- Supports 24-pin 1K, 2K, and 4K x 8 ROM/EPROM devices (either single or multiple voltage).
- Programmable memory mapping via a jumper select area.
- Organized into two independent 8-socket blocks.
- Slow memory capability is provided for 1.5 MHz or 2 MHz operation.
- Provision for Write function if RAM devices are used.
- Operates at clock speeds of 1 MHz, 1.5 MHz, or 2.0 MHz when the appropriate ROM/EPROM devices are used.

1.3 SPECIFICATIONS

Micromodule 4A specifications are identified in Table 1-1.

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FIGURE 1-1. Micromodule 4A

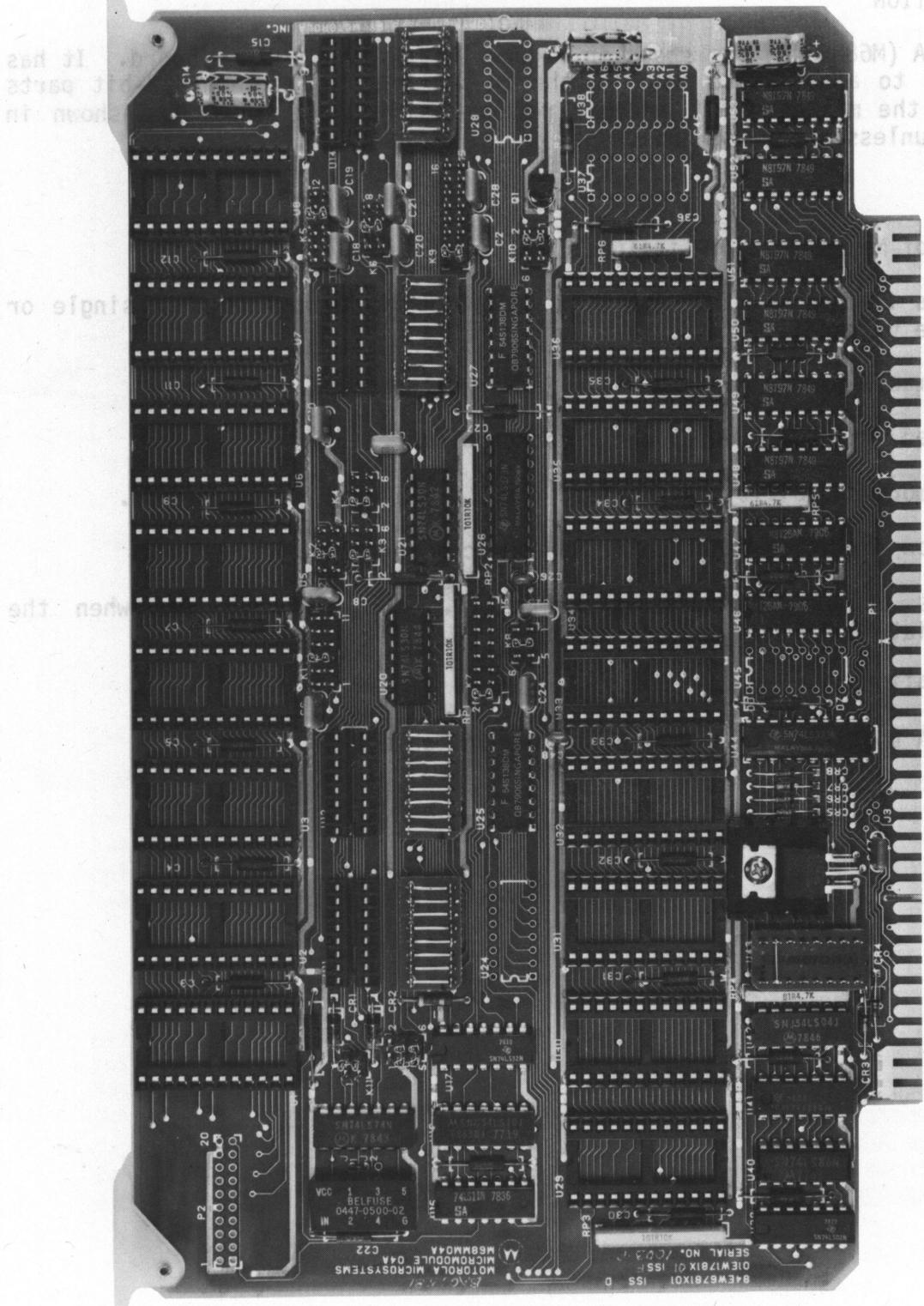


TABLE 1-1. MM04A Specifications

CHARACTERISTICS	SPECIFICATIONS
Power Requirements	
with no EPROM's	+5V @ 650 mA max. -12V @ 8 mA max.
with 16 2716 (5V only) 2K x 8 EPROM's	+5V @ 1000 mA
with 16 2708 EPROM's	+5V @ 730 mA +12V @ 800 mA -12V @ 480 mA
Memory Size	Sockets for mounting up to 16 EPROM's or ROM's such as the 2708, 2716, or 2732.
Memory Organization	16K, 32K, or 64K byte capability consisting of two 8K, 16K, or 32K byte memory blocks, depending on whether 1K, 2K, or 4K parts are used.
Base Address Selection	Jumper selectable in 8K, 16K, or 32K byte increments for 1K, 2K, and 4K parts, respectively. Delivered units are pre-addressed at 8000 to BFFF (U29-U36) and C000 to FFFF (U1-U8) (for 2K devices).
Micromodule Bus	
Address Bus	TTL compatible buffered input.
Control Bus	TTL compatible buffered input.
Data Bus	Three-state TTL compatible buffered input and output.
Operating Temperature	0° to 70° C
Physical Characteristics	
Width x Height	9.75 x 6.50 inches
Thickness	0.062 inches (board only) 0.5 inches (maximum device height)
Bus Mating Connector Types	
Connector P1 (86 pin)	Stanford Applied Engineering SAC-43D/l-2 or equivalent



CHAPTER 2

INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, and installation instructions for the M68MM04A ROM/EPROM board. This chapter also discusses the user options that have been incorporated into this module.

2.2 UNPACKING INSTRUCTIONS

NOTE

IF THE SHIPPING CARTON IS DAMAGED UPON RECEIPT,
REQUEST THAT THE CARRIER'S AGENT BE PRESENT
DURING UNPACKING AND INSPECTION OF THE MODULE.

Remove the module from its shipping carton. Refer to the packing list and verify that all of the items are present. Save the packing material for storing and reshipping the module.

2.3 INSPECTION

The module should be inspected upon receipt for broken, damaged, or missing parts, and for physical damage to the printed circuit board.

2.4 INSTALLATION INSTRUCTIONS

Since the ROM/EPROM module is intended for user-designed microcomputer based systems, no special installation instructions are provided. After the EPROM's and/or ROM's have been programmed by the user and the module has been configured per paragraph 2.5, each device is inserted into the appropriate socket and the module is then inserted into the user's system. Turn power OFF on the equipment in which module is being installed.

CAUTION

INSERTING A MODULE INTO A SYSTEM WHILE
POWER IS APPLIED TO THE SYSTEM MAY RESULT
IN DAMAGE TO COMPONENTS ON THE MODULE.

2.5 CONFIGURATION INSTRUCTIONS

Each block of eight sockets may be individually configured to work with 1024 x 8, 2048 x 8, or 4096 x 8-bit EPROM's, ROM's, or RAM's. The signals present at each 24-pin memory socket are listed in Table 2-1. The user should configure the module to meet his system requirements through the following steps:

- a. Select the type of devices to be used. (Each group of eight sockets may have a different type of device.)
- b. Select the base address desired for each eight-socket block. Install the required jumpers per Table 2-3 and Figure 2-1.

- c. Select VUA, VXA, or \overline{PE} jumper options (this may be different for each group of eight sockets).

VUA K3, 1-2 for lower eight sockets (U29-U36)
K4, 1-2 for upper eight sockets (U1-U8)

VXA K3, 3-4 for lower eight sockets (U29-U36)
K4, 3-4 for upper eight sockets (U1-U8)

\overline{PE} K3, 5-6 for lower eight sockets (U29-U36)
K4, 5-6 for upper eight sockets (U1-U8)

- d. Install jumper wires and jumper platforms for device size (1K, 2K, or 4K) and device pins 18 through 21. See Table 2-2.

NOTE

Pins on K8 and K10 are numbered from right to left for issue T and earlier boards, but they are numbered from left to right for issue U and later boards.

- e. If slow memories are to be used for systems with MPU II, move the jumper at K11 to pins 1 and 3. For all other systems, leave the jumper at K11 pins 2 and 4. Refer to the theory in Chapter 3.

NOTE

K11 pins 3 and 1 are the lower left and upper left pins.
K11 pins 4 and 2 are the lower right and upper right pins.

Install jumper J3 to connect the MEMRDY signal to P1 pin R. Then, for 1.5 MHz operation, install a jumper at J2; or for 2.0 MHz operation, install a jumper at J1. To disable the slow memory circuits for one bank of eight memories only, remove the jumper at K0 pins 3 and 4 (lower bank) or K0 pins 5 and 6 (upper bank), and ground this pin (3 or 5) to K0 pin 1.

- f. As delivered, U24 and U28 are straight-through connections on the printed wiring board. If the customer wants to free part of the memory map for off-board use, he may cut the printed wires at U24 and/or U28 and install a rocker switch (such as AMP type 435166-5 or equivalent). Opening a section of the switch three-states the corresponding buffer, making MM04A non-responsive to that 1K, 2K, or 4K block of memory. (Each section of the switch will disable one socket.)

NOTE

Switches on U24 disable higher-address sockets as you proceed from switches on the left to those on the right. This works from right to left, however, on U28.

- g. As delivered, U37, U38, and U45 are straight-through connections on the printed wiring board. If there is ringing (overshoot) on the address lines (U37, U38) and/or the data lines (U45), the customer may cut the printed wires and install a resistor pad (such as CTS type 761-3-R series or equivalent).

- h. Install devices in their appropriate sockets.

TABLE 2-1. ROM/EPROM Device Pin Connections

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	A7'	ADDRESS LINE 7 -- When enabled, this address line addresses the A7 input to the ROM/RAM sockets.
2	A6'	ADDRESS LINE 6 -- When enabled, this address line addresses the A6 input to the ROM/RAM sockets.
3	A5'	ADDRESS LINE 5 -- When enabled, this address line addresses the A5 input to the ROM/RAM sockets.
4	A4'	ADDRESS LINE 4 -- When enabled, this address line addresses the A4 input to the ROM/RAM sockets.
5	A3'	ADDRESS LINE 3 -- When enabled, this address line addresses the A3 input to the ROM/RAM sockets.
6	A2'	ADDRESS LINE 2 -- When enabled, this address line addresses the A2 input to the ROM/RAM sockets.
7	A1'	ADDRESS LINE 1 -- When enabled, this address line addresses the A1 input to the ROM/RAM sockets.
8	A0'	ADDRESS LINE 0 -- When enabled, this address line addresses the A0 input to the ROM/RAM sockets.
9	D0	DATA LINE 0 -- When enabled, this data line transfers data from or to the selected ROM/RAM device and the module data bus.
10	D1	DATA LINE 1 -- Same as D0 on pin 9.
11	D2	DATA LINE 2 -- Same as D0 on pin 9.
12	GND	GROUND
13	D3	DATA LINE 3 -- Same as D0 on pin 9.
14	D4	DATA LINE 4 -- Same as D0 on pin 9.
15	D5	DATA LINE 5 -- Same as D0 on pin 9.
16	D6	DATA LINE 6 -- Same as D0 on pin 9.
17	D7	DATA LINE 7 -- Same as D0 on pin 9.
18		
19		SIGNAL MNEMONIC Name and Description depends on the device being used. See Table 2-2.
20		
21		

TABLE 2-1. ROM/EPROM Device Pin Connections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
22	A9'	ADDRESS LINE 9 -- When enabled, this address line addresses the A9 input to the ROM/RAM sockets.
23	A8'	ADDRESS LINE 8 -- When enabled, this address line addresses the A8 input to the ROM/RAM sockets.
24	+5VDC	+5 Vdc

TABLE 2-2. Jumpers for Device Size and Signals (Sheet 1 of 2)

DEVICE	TYPE	MEMORY SIZE	PIN 18	PIN 19	PIN 20	PIN 21	DEVICE SIZE JUMPER	JUMPER PLATFORM POSITION
2708	EPROM	1KX8	GRD K1, 7-8 (K5, 5-6)	+12V K2, 5-6 (K6, 5-6)	\overline{CE}	-5V K7, 9-10 (K9, 9-10)	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
2758	EPROM	1KX8	\overline{CE}	GRD K2, 7-8 (K6, 7-8)	\overline{CE}	+5V K7, 1-2 (K9, 1-2)	K8, 1-2 (K10, 1-2)	U18, U19 (U22, U23)
2608	PROM	1KX8	GRD K1, 7-8 (K5, 5-6)	+12V K2, 5-6 (K6, 5-6)	\overline{CE}	-5V K7, 9-10 (K9, 9-10)	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
82S2708	PROM	1KX8	N.C.	\overline{CE}	N.C.	\overline{CE}	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
82S181	PROM	1KX8	CE4 K1, 11-12 (K5, 1-2)	CE3 K2, 1-2 (K6, 1-2)	$\overline{CE2}$	$\overline{CE1}$ K7, 15-16 (K9, 15-16)	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
3628	PROM	1KX8	CS4 K1, 11-12 (K5, 1-2)	CS3 K2, 1-2 (K6, 1-2)	$\overline{CS2}$	$\overline{CS1}$ K7, 15-16 (K9, 15-16)	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
82S281	ROM	1KX8	CE4 K1, 11-12 (K5, 1-2)	CE3 K2, 1-2 (K6, 1-2)	$\overline{CE2}$	$\overline{CE1}$ K7, 15-16 (K9, 15-16)	K8, 1-2 (K10, 1-2)	U11, U19 (U13, U23)
Am9208	ROM	1KX8	\overline{CE}	+12V K2, 5-6 (K6, 5-6)	\overline{CE}	N.C.	K8, 1-2 (K10, 1-2)	U18, U19 (U22, U23)
MK4118	RAM	1KX8	\overline{CS}	\overline{L} K2, 1-2 (K6, 1-2)	\overline{OE}	\overline{WE} K7, 5-6 (K9, 5-6)	K8, 1-2 (K10, 1-2)	U18, U19 (U22, U23)
MK4801	RAM	1KX8	\overline{CS}	\overline{L} K2, 1-2 (K6, 1-2)	\overline{OE}	\overline{WE} K7, 5-6 (K9, 5-6)	K8, 1-2 (K10, 1-2)	U18, U19 (U22, U23)

Data in parentheses refers to upper eight sockets.

TABLE 2-2. Jumpers for Device Size and Signals (Sheet 2 of 2)

DEVICE	TYPE	MEMORY SIZE	PIN 18	PIN 19	PIN 20	PIN 21	DEVICE SIZE JUMPER	JUMPER PLATFORM POSITION
2716	EPROM	2KX8	\overline{CE}	A10 K2, 3-4 (K6, 3-4)	\overline{OE}	VPP K7, 1-2 (K9, 1-2)	K8, 3-4 (K10, 3-4)	U18, U19 (U22, U23)
TMS2516	EPROM	2KX8	PD	A10 K2, 3-4 (K6, 3-4)	\overline{CS}	VPP K7, 1-2 (K9, 1-2)	K8, 3-4 (K10, 3-4)	U18, U19 (U22, U23)
TMS2716	EPROM	2KX8	\overline{CE}	+12V K2, 5-6 (K6, 5-6)	A10 K1, 3-4 (K5, 9-10)	-5V K7, 9-10 (K9, 9-10)	K8, 3-4 (K10, 3-4)	U12, U18 (U14, U22)
82S191	PROM	2KX8	CE3 K1, 11-12 (K5, 1-2)	CE2 K2, 1-2 (K6, 1-2)	$\overline{CE_1}$	A10 K7, 7-8 (K9, 7-8)	K8, 3-4 (K10, 3-4)	U11, U19 (U13, U23)
2316E	ROM	2KX8	$\overline{CS_2}$	A10 K2, 3-4 (K6, 3-4)	$\overline{CS_1}$	CS3 K7, 1-2 (K9, 1-2)	K8, 3-4 (K10, 3-4)	U18, U19 (U22, U23)
82S291*	ROM	2KX8	CE3 K1, 11-12 (K5, 1-2)	CE2 K2, 1-2 (K6, 1-2)	$\overline{CE_1}$	A10 K7, 7-8 (K9, 7-8)	K8, 3-4 (K10, 3-4)	U11, U19 (U13, U23)
TMS4016	RAM	2KX8	\overline{CS}	A10 K2, 3-4 (K6, 3-4)	\overline{OE}	\overline{W} K7, 5-6 (K9, 5-6)	K8, 3-4 (K10, 3-4)	U18, U19 (U22, U23)
2732	EPROM	4KX8	\overline{CE}	A10 K2, 3-4 (K6, 3-4)	\overline{OE}	A11 K7, 13-14 (K9, 13-14)	K8, 5-6 (K10, 5-6)	U18, U19 (U22, U23)
TMS2532	EPROM	4KX8	A11 K1, 9-10 (K5, 3-4)	A10 K2, 3-4 (K6, 3-4)	PD	VPP K7, 1-2 (K9, 1-2)	K8, 5-6 (K10, 5-6)	U11, U19 (U13, U23)
2332A	ROM	4KX8	\overline{CE}	A10 K2, 3-4 (K6, 3-4)	\overline{OE}	A11 K7, 13-14 (K9, 13-14)	K8, 5-6 (K10, 5-6)	U18, U19 (U22, U23)

Data in parentheses refers to upper eight sockets.

*Hookup shown is compatible with 82S191; User Device chip selects may possibly be different.

TABLE 2-3. Base Address Jumper Selects (Eight per Block)

1024X8

Jumper at K8, 1-2 (right)*

Jumper at K10, 1-2 (right)*

Address	Lower 8 Sockets (U29-U36)			Upper 8 Sockets (U1-U8)		
	AS2 U43 3-14	AS1 U43 2-15	AS0 U43 1-16	AS5 U43 6-11	AS4 U43 5-12	AS3 U43 4-13
\$0000-\$1FFF	L	L	L	L	L	L
\$2000-\$3FFF	L	L	H	L	L	H
\$4000-\$5FFF	L	H	L	L	H	L
\$6000-\$7FFF	L	H	H	L	H	H
\$8000-\$9FFF	H	L	L	H	L	L
\$A000-\$BFFF	H	L	H	H	L	H
\$C000-\$DFFF	H	H	L	H	H	L
\$E000-\$FFFF	H	H	H	H	H	H

2048X8

Jumper at K8, 3-4 (center)

Jumper at K10, 3-4 (center)

Address	Lower 8 Sockets (U29-U36)			Upper 8 Sockets (U1-U8)		
	AS2 U43 3-14	AS1 U43 2-15	AS0 U43 1-16	AS5 U43 6-11	AS4 U43 5-12	AS3 U43 4-13
\$0000-\$3FFF	L	L	H	L	L	H
\$4000-\$7FFF	L	H	H	L	H	H
\$8000-\$BFFF	H**	L**	H**	H	L	H
\$C000-\$FFFF	H	H	H	H**	H**	H**

4096X8

Jumper at K8, 5-6 (left)*

Jumper at K10, 5-6 (left)*

Address	Lower 8 Sockets (U29-U36)			Upper 8 Sockets (U1-U8)		
	AS2 U43 3-14	AS1 U43 2-15	AS0 U43 1-16	AS5 U43 6-11	AS4 U43 5-12	AS3 U43 4-13
\$0000-\$7FFF	L	H	H	L	H	H
\$8000-\$FFFF	H	H	H	H	H	H

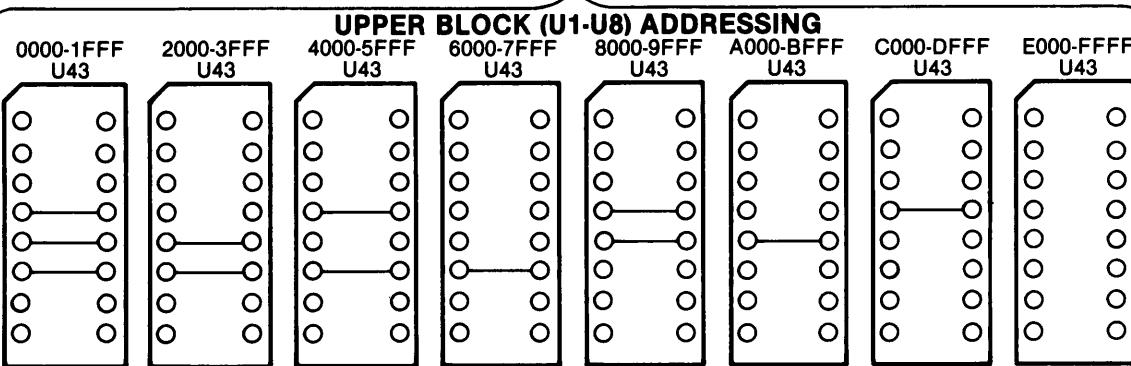
* K8 and K10 pins are numbered right to left on issue T and earlier boards, but are numbered left to right on issue U and later boards. Therefore, pins 1-2 are at the right on early boards, but on the left on later boards, and pins 5-6 are at the left on early boards, but on the right on later boards.

H = High Level (No Connection)

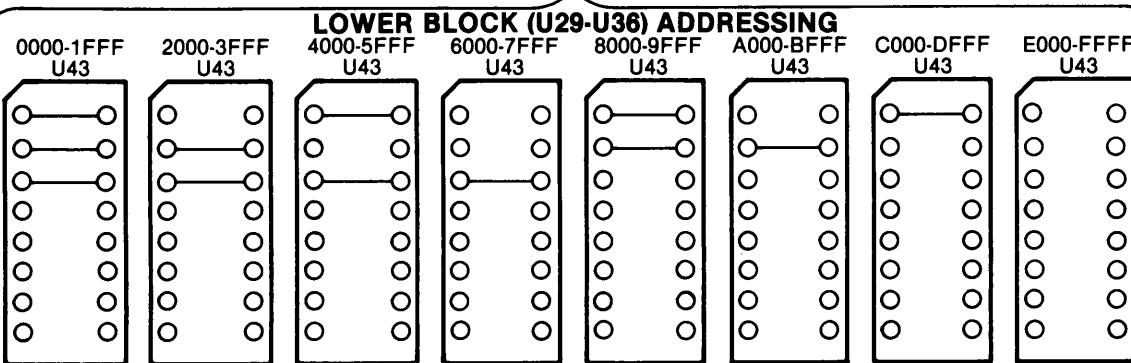
L = Low Level (Ground - Strap between pins indicated)

** = As-delivered configuration.

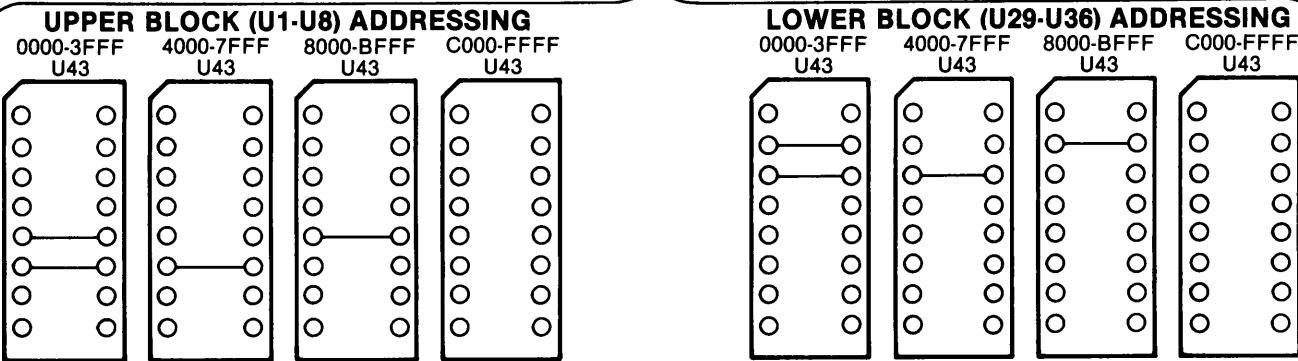
JUMPERS FOR 1Kx8 DEVICES



JUMPERS FOR 1Kx8 DEVICES



JUMPERS FOR 2Kx8 DEVICES



JUMPERS FOR 2Kx8 DEVICES

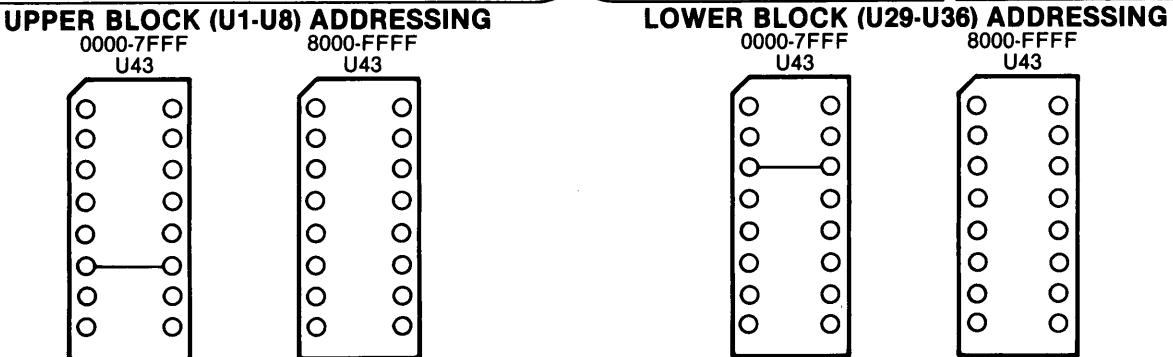


FIGURE 2-1. Base Address Jumpers

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter provides a block diagram description of Micromodule 4A. The block diagram is shown in Figure 3-1; a schematic is shown in Figure 4-2.

3.2 GENERAL DESCRIPTION

This module has provisions for up to sixteen memory elements arranged into two separate independent blocks. Each block contains eight 24-pin sockets for up to eight 1024X8, 2048X8, or 4096X8-bit EPROM, ROM, or RAM devices. An eight socket block can provide up to 8K, 16K, or 32K bytes of memory, depending on the devices used. To set up the module, the user: (1) selects the base address for each block (AS0, 1, 2 for the lower eight sockets; AS3, 4, 5 for the upper eight sockets); (2) selects VUA/VXA/ \overline{PE} Control; (3) selects the device size jumper (1K, 2K, or 4K parts); (4) selects the proper jumpers for pins 18 through 21 for the particular device used.

The MM04A ROM/EPROM Micromodule is compatible with devices like those listed in Table 2-2. That table also defines the pin connections (pins 18 through 21) for the different devices.

The sixteen individual chip enable jumpers permit the user to enable ROM/EPROM devices being used and to disable those that are not. Unless disabled by cutting the trace on U24 or U28 on the printed wiring board, each ROM/EPROM socket will occupy memory whether a device is installed or not. Memory locations assigned to disabled sockets may be assigned to other memory or peripheral devices in the user system.

3.3 BLOCK DIAGRAM DESCRIPTION

The MM04A ROM/EPROM Micromodule (refer to Figure 3-1) receives the sixteen address lines A0 through A15, along with the $\overline{Q2}$ and MEM CLK timing signals, VUA (Valid User Address), VXA (Valid Executive Address), and the R/W (Read/Write) signals, during each memory operation. During an MPU write operation, this module also receives the eight data lines $\overline{D0}$ through $\overline{D7}$.

All the address (A0 through A15) and data ($\overline{D0}$ through $\overline{D7}$) lines, as well as the R/W, $\overline{Q2}$, MEM CLK, VUA, VXA, and \overline{PE} signals, are buffered at the bus by the module. Address lines A0 through A9 and data lines D0 through D7 are bused directly from the buffers to all 16 memory sockets. Address lines A10 and A11 are made available at jumper areas for use when the larger size memories are used. The buffered R/W and $\overline{Q2}$ signals are used by the read/write and data buffer control logic to generate the data buffer R/W ENABLE (and the WRITE ENABLE \overline{W} signal, if RAM is used).

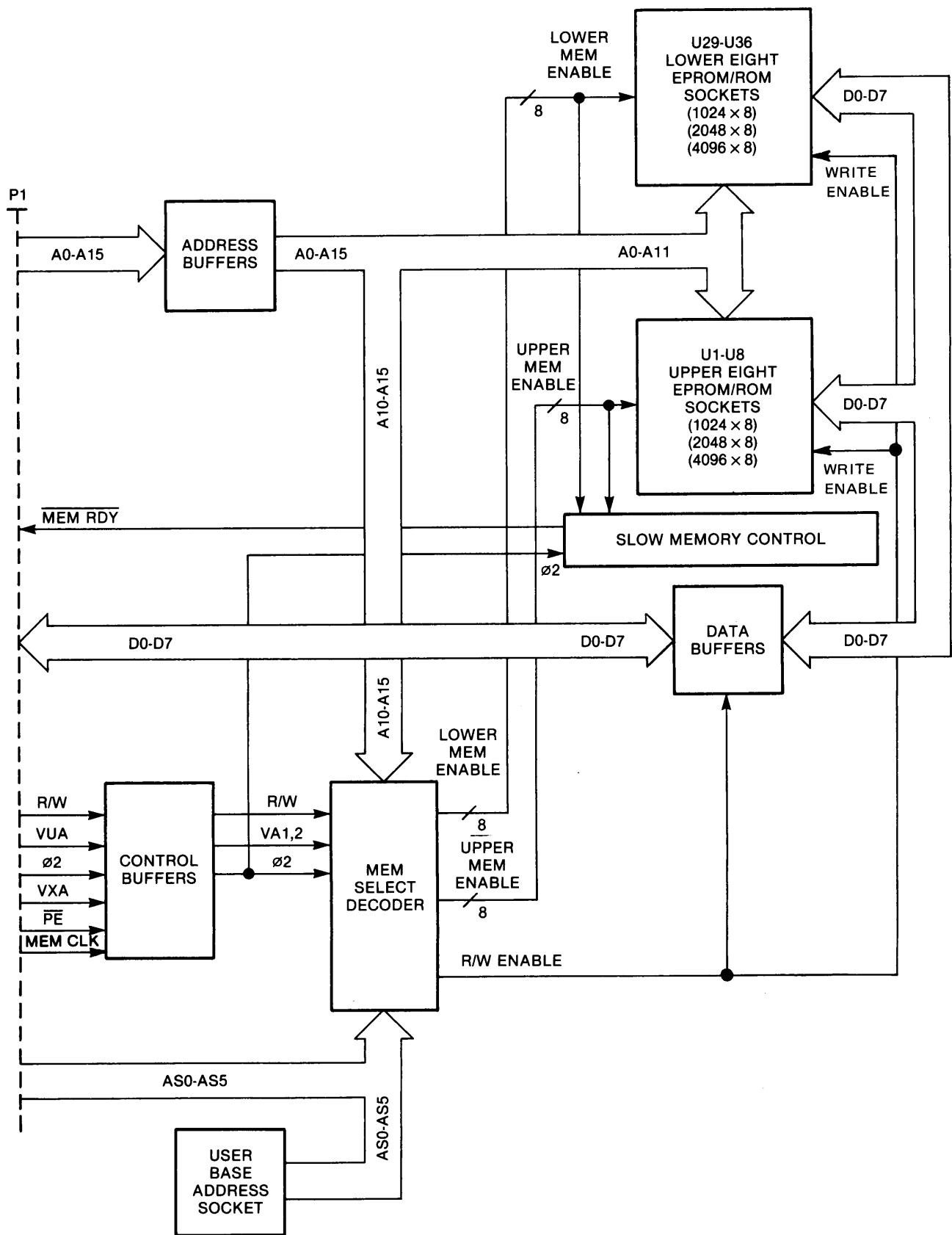


FIGURE 3-1. ROM/EPROM Module (MM04A) Block Diagram

The data bus interface (Data Buffers) provides a two-way data transfer between the module data bus and the EXORciser or Micromodule bus. The driver and receiver circuits in the data bus interface are three-state logic devices whose operations are controlled by the R/W ENABLE generated by the Memory Select Decoders and control logic. When the drivers and receivers are in their disabled or off state, they provide high impedance outputs to their respective buses.

The buffered VUA, VXA, and \overline{PE} signals (in the form of VA1 or VA2), along with address lines A10 through A15, are used by the two Memory Select Decoder circuits to determine whether the MPU is addressing one of the sockets in its memory array. Since both sets of sockets are identical in operation, only the decoding of the lower eight sockets will be discussed here. Jumpers on the User Base Address Select Socket (U43) determine the base address for the lower eight sockets, and the Memory Select Decoder determines when the MPU is trying to access one of the sockets in the block.

During an MPU memory read operation, the Control Buffers receive high level R/W and VUA or VXA signals and route them to the control logic. At the same time, the memory location to be read will appear on the address bus. If the address is located within the memory block (base address), the decoder is enabled and generates a low level \overline{CE} signal for the individual memory socket and a high level signal to the data bus control circuitry.

When $\overline{\theta_2}$ goes high, address lines A9 through A15, R/W, VUA, and VXA are latched into buffers, and will remain latched until the falling edge of $\overline{\theta_2}$. The data bus control circuitry will generate a high level READ ENABLE signal which enables the driver portion of the Data Buffers. After the access time of the memory has elapsed, the contents of the memory location will be present at the output of the Data Buffer to be read by the MPU when $\overline{\theta_2}$ goes low again.

If the user intends to use RAM's instead of ROM's, then what occurs during an MPU write operation is of interest here. The module now receives a low R/W signal and data lines $\overline{D_0}$ through $\overline{D_7}$, in addition to VUA or VXA. Again, the memory address which is to be written to appears at the Address Buffers. The Decoder will again be enabled, and generates a low level \overline{CE} signal to the appropriate memory socket and a high level signal to the data bus control circuitry. When $\overline{\theta_2}$ goes high, the data bus control circuitry will generate a low level WRITE ENABLE signal, which will enable the receiver portion of the Data Buffers. At the same time, it also generates a low level Write (\overline{W}) signal that is bused to the eight sockets. This allows the data present on the bus to be stored in that memory location.

If the control logic does not receive a low level \overline{CE} (Mem Enable) signal from the decoder circuitry, it will not generate a R/W ENABLE signal, and the data bus remains three-stated. This will occur if the address location does not reside on the module or if that particular socket \overline{CE} has been disabled.

The Memory Ready (MEM RDY) circuit allows the user to use "slow memory" in his system (for example, 1.0 MHz parts in a 2.0 MHz system). Two basic types of systems can be used: (1) one that requires that MEM RDY be low prior to the rising edge of $\overline{\theta_2}$, such as an MEX6800-2 MPU II Module; and (2) one that requires that MEM RDY be low prior to the normal falling edge of $\overline{\theta_2}$, such as one employing an MC6871 clock chip.

When used with an MPU II Module, the CE signal bypasses the timing circuitry and is fed directly into the 8T97 buffer (U52) input via K11 pins 1 and 3. When the board is accessed, CE goes high during ϕ_1 and will be latched in on the rising edge of ϕ_2 . CE will then remain high until the next falling edge of ϕ_2 . This would normally latch up the clock in most system. However, the MPU II Module internal circuitry will not allow ϕ_2 to be stretched for more than one cycle at a time.

When a system employing an MC6871 clock chip is used (or any other clock except that used on the MPU II board), the output of the timing circuit drives the 8T97 via K11 pins 2 and 4. Figure 3-2 shows a schematic representation of this circuit, as well as the associated waveform timing diagrams. This circuit guarantees that (1) MEM RDY is low prior to the normal falling edge of ϕ_2 , and that (2) MEM RDY will only remain low for a predetermined time period, ensuring that there will be no system latch up. This type of circuit could not be used with an MPU II Module because the CE signal is clocked in on the rising edge of ϕ_2 (in MM04A), and would not be present on the bus in time. For 1.5 MHz operation, a jumper at J2 should be installed on the delay line U9. For 2.0 MHz operation, the jumper should be installed at J1.

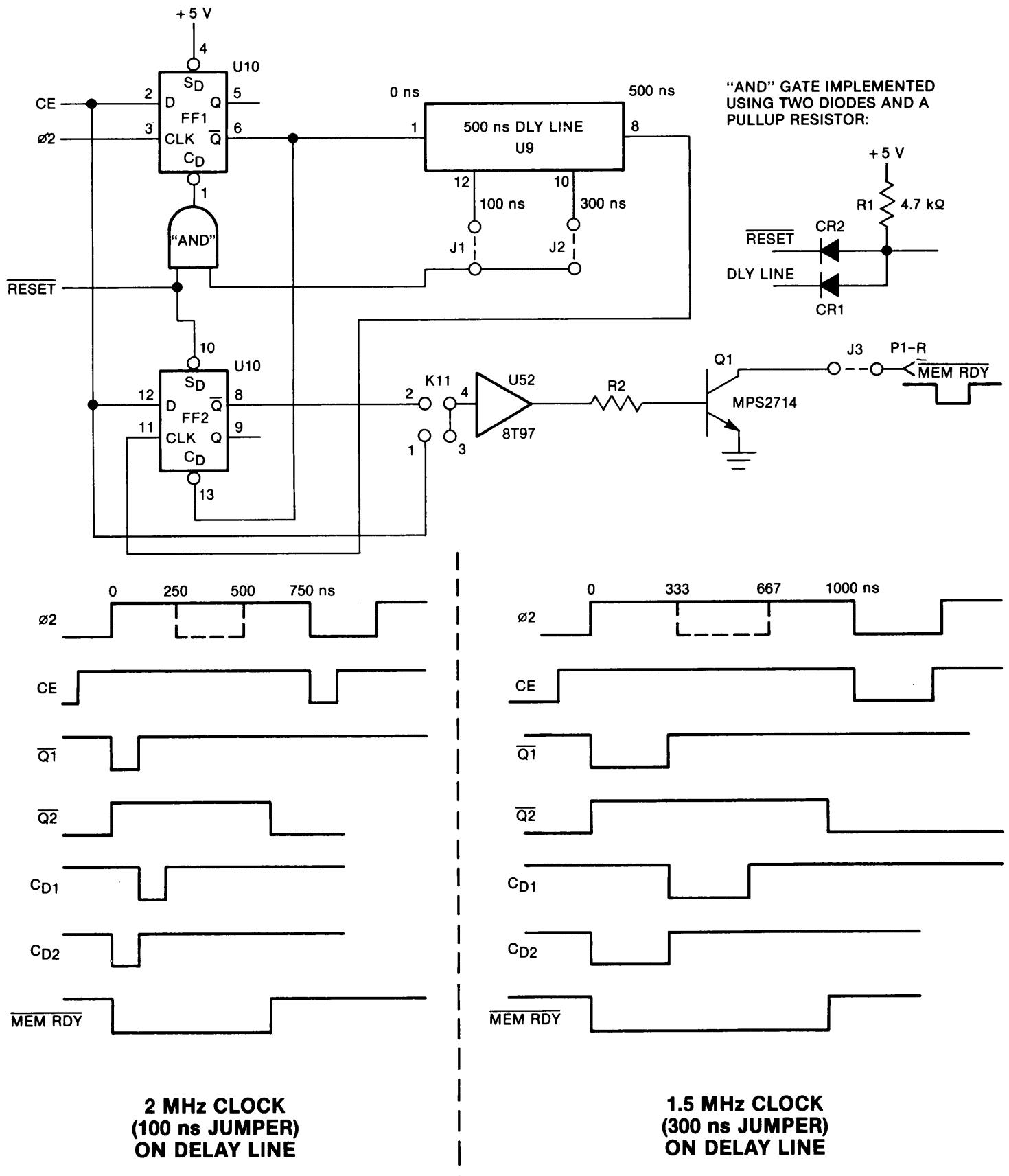
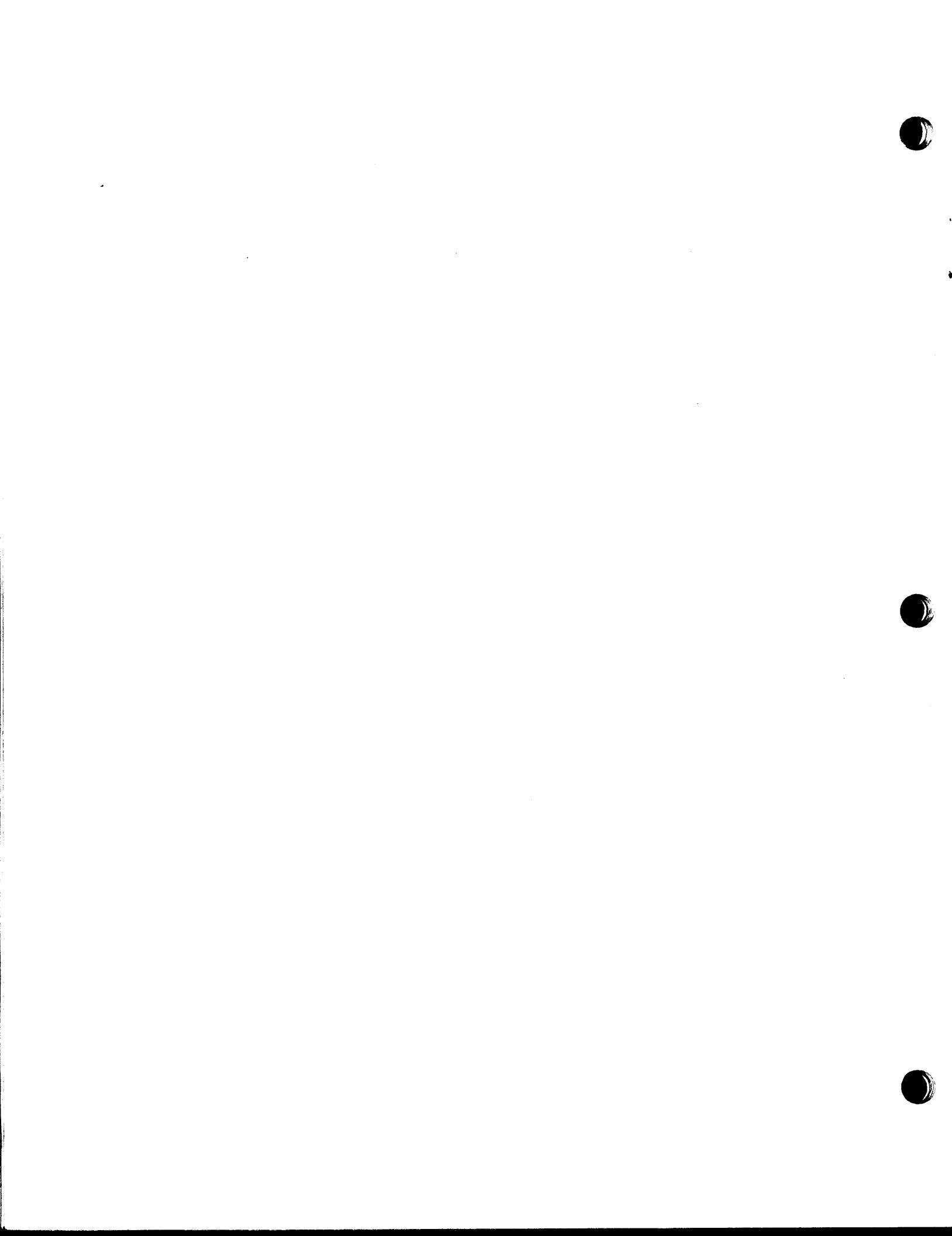


FIGURE 3-2. Slow Memory Circuits and Timing



CHAPTER 4

MAINTENANCE INFORMATION

4.1 INTRODUCTION

This chapter provides the parts list (Table 4-1) for Micromodule 4A. The list reflects the latest issue of hardware at the time of printing. Parts locations are shown in Figure 4-1. The MM04A schematic diagram is given in Figure 4-2.

Micromodule 4A is bus compatible with either the Micromodule bus or the EXORciser bus. These bus signals are identified in Table 4-2.

TABLE 4-1. Micromodule 4A (M68MM04A) Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
-	84EW6781X01	Printed Wiring Board, Micromodule 4A
-	55NW9403A05	Ejector Card, .062 thick, .250 wide, white (2 required)
C1,C3-C5,C7, C9,C11-C13, C15,C16,C22, C23,C27, C30-C37, C39-C45	21SW992C025	Capacitor, Ceramic, Axial Lead, 0.100 uF @ 50 Vdc, 20%
C2,C6,C8,C10, C17-C21,C24, C25,C28	21NW9604A08	Capacitor, Ceramic, 1 uF @ 50 Vdc, 20%
C14,C38,C46	23NW9618A33	Capacitor, Electrolytic, 25 uF @ 16 Vdc
C26,C48	21NW9702A09	Capacitor, Ceramic, 0.1 uF @ 50 Vdc
C29	-	Not used.
C47	21NW9604A18	Capacitor, Fixed, Ceramic, .68 uF @ 50 Vdc
CR1,CR2	48NW9616A02	Diode, Signal, Germanium, 1N270
CR3-CR8	48NW9607A09	Diode, Rectifier, Silicon, 1N4148
J1-J3	-	Jumper areas (on the printed circuit board)
K0,K3,K4, K8,K10	28NW9802B21	Header, Double Row, Post 6-pin
	28NW9802B88	Alternate Header, Double Row, Post 6-pin
K1,K5	28NW9802C63	Header, Double Row, 12-pin, .100 Center

TABLE 4-1. Micromodule 4A (M68MM04A) Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
K2 ,K6	28NW9802C43	Header, Double Row, 8-position
K7 ,K9	28NW9802B34	Header, Double Row, Post, 16-pin
K11	28NW9802C29	Header, Double Row, Straight, 4-pin
-	28NW9805B17	Jumper, Shorting, Insulated, (13 required) (Used on K0-K11)
Q1	48NW9610A10	Transistor, NPN, Hi-Speed Switch, Plastic, type MPS2714
R1	06SW-124A65	Resistor, Fixed Carbon, 4.7k ohms, 5%, 1/4W
R2	06SW-124A38	Resistor, Fixed Carbon, 360 ohms, 5%, 1/4W
RP1-RP3	51NW9626A37	Resistor Network, 9 per package, 10k ohms each
RP4	51NW9626A47	Resistor Network, 7 per package, 4.7k ohms each
RP5,RP6	51NW9626A46	Resistor Network, 5 per package, 4.7k ohms each
U1-U8 , U29-U36	-	Customer-provided ROM's, EPROM's, or RAM's (in 24-pin package)
-	09NW9811A15	Socket, I.C., Dual In-Line, Low Profile, 24-pin (Used at U1-U8, U29-U36)
U9	01NW9804B78	Digital Delay Line, 500 nsec (Bel Fuse part number 0447-0500-02)
U10	51NW9615C25	I.C. SN74LS74N
-	09NW9811A04	Socket, I.C., Dual In-Line, Low Profile, 16-pin (Used at U11-U14, U18-U19, U22-U23, U43)
*	28CW1957X01	Address Select Platform (4 required) *Used at U11,U12,U13,U14,U18,U19, U22, and/or U23 - see Chapter 2.
**	28CW1957X02	Address Select Platform **Used at U43 - see Chapter 2.
U15	51NW9615F76	I.C. SN74LS11N
U16	51NW9615E88	I.C. 74LS10A

TABLE 4-1. Micromodule 4A (M68MM04A) Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U17	51NW9615C24	I.C. SN74LS32N
U20 ,U21	51NW9615C23	I.C. SN74LS30N
U24 ,U28	-	As delivered, these are straight-through connections on the printed wiring board. They may be replaced with customer-provided rocker switches. See Chapter 2.
U25 ,U27	51NW9615C34	I.C. SN74S138N
U26 ,U44	51NW9615E98	I.C. SN74LS373N
U37 ,U38 ,U45	-	As delivered, these are straight-through connections on the printed wiring board. They may be replaced with customer-provided resistor pads. See Chapter 2.
U39	51NW9615C20	I.C. SN74LS02N
U40 ,U41	51NW9615F01	I.C. SN74LS86N
U42	51NW9615C21	I.C. SN74LS04N
U46 ,U47	51NW9615B35	I.C. 8T26
U48-U53	51NW9615B71	I.C. 8T97
VR1	51NW9615C39	I.C. MC7905CP
-	26NW9417A06	Heatsink, for TO-220 cases (used with VR1)
-	43NW9002A47	Bushing, insulator, nylon, shoulder (2 required)
-	03SW993A406	Screw, phillips-head, plain, 4-40x3/8
-	02SW990A408	Nut, hex, 4-40x1/4
-	04SW995A006	Washer, internal locking, No. 4 (Required only on boards of issue T or earlier. Washers are not used on boards of issue U or later.)

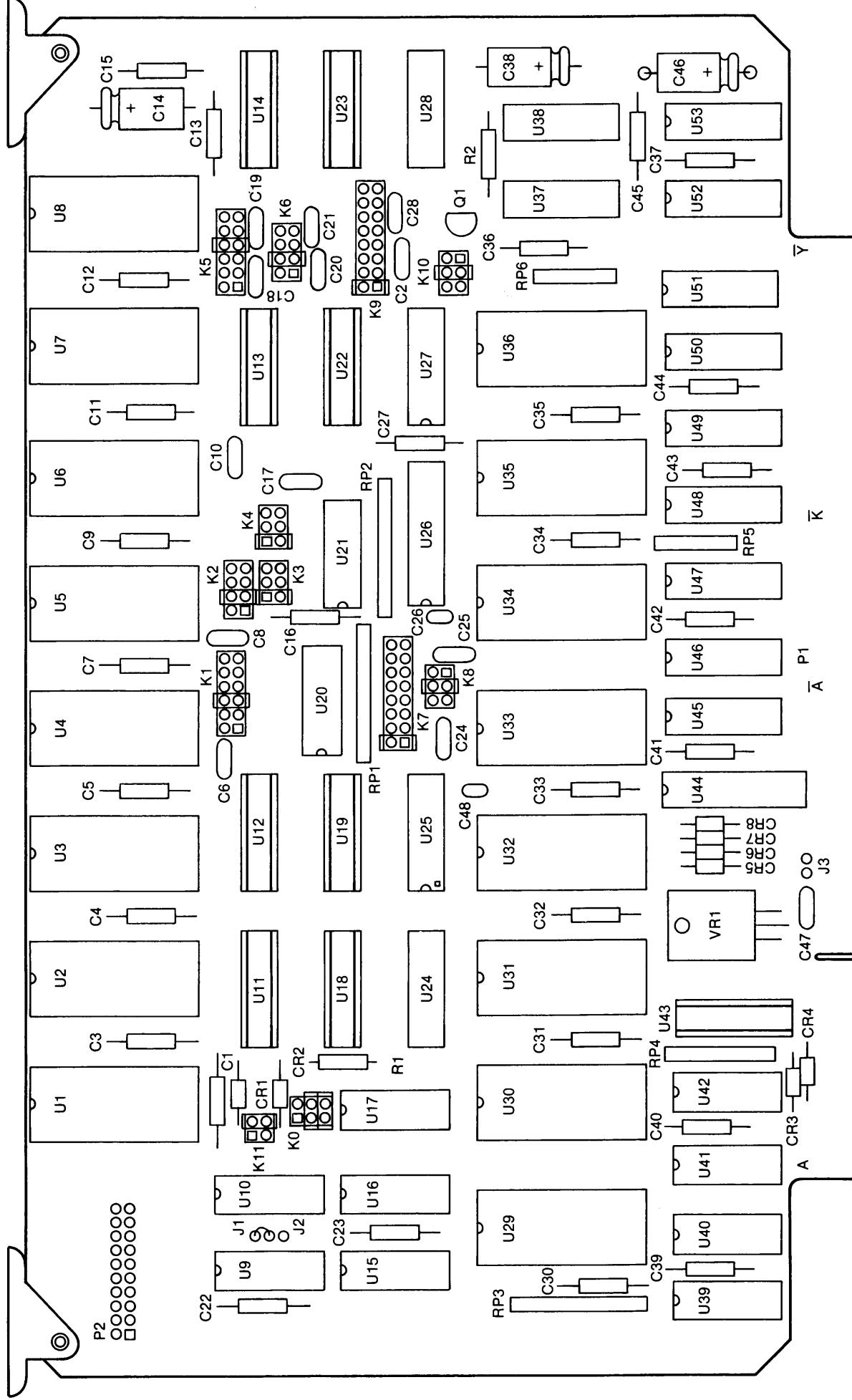


FIGURE 4-1. Micromodule 4A Parts Location

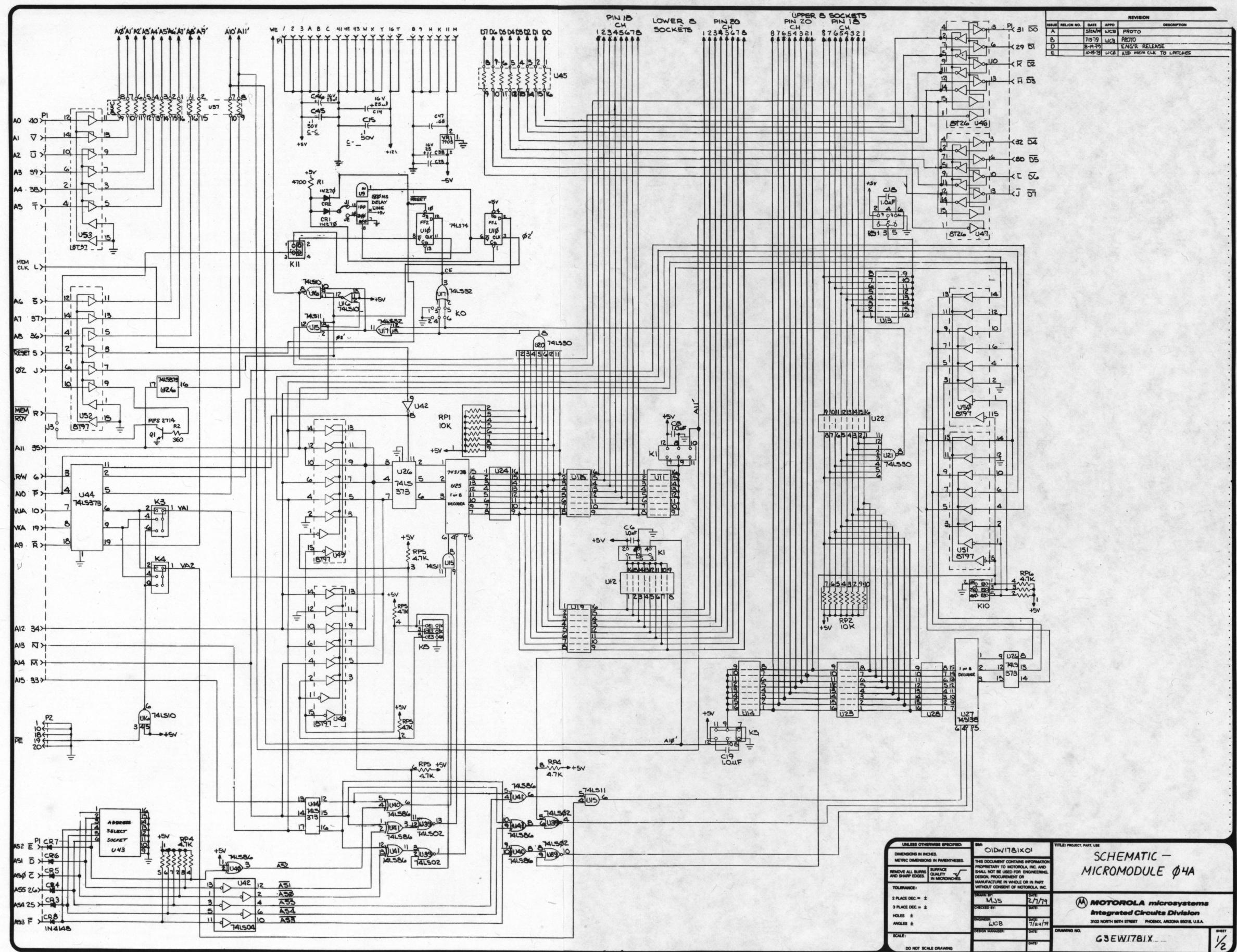


TABLE 4-2. ROM/EPRAM Module Bus Interface Connections

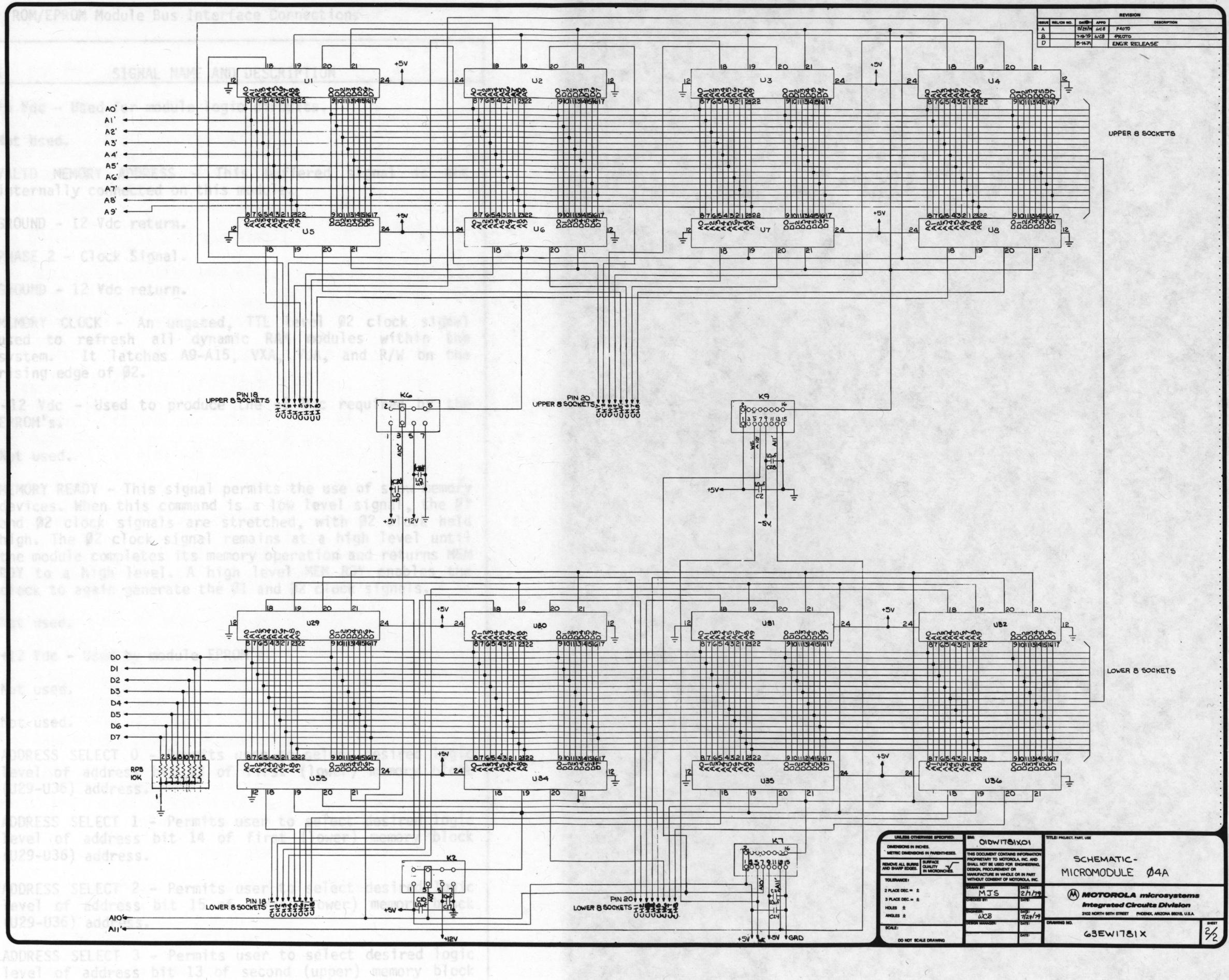


TABLE 4-2. ROM/EPROM Module Bus Interface Connections

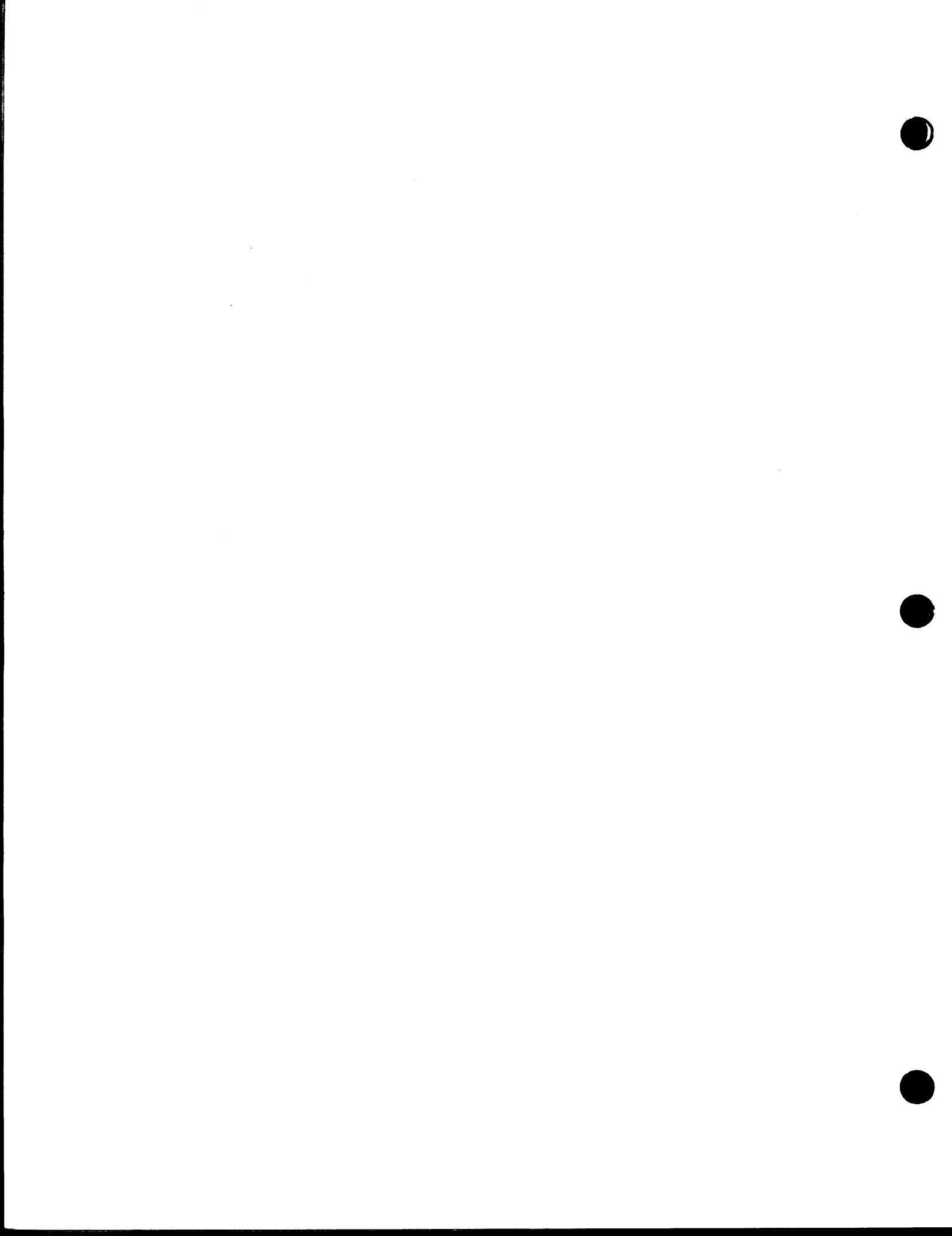
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A,B,C	+5V	+5 Vdc - Used for module logic circuits.
D,E		Not used.
F	VMA	VALID MEMORY ADDRESS - This buffered signal is not internally connected on this module.
H	GROUND	GROUND - 12 Vdc return.
J	Ø2	PHASE 2 - Clock Signal.
K	GROUND	GROUND - 12 Vdc return.
L	MEM CLK	MEMORY CLOCK - An ungated, TTL level Ø2 clock signal used to refresh all dynamic RAM modules within the system. It latches A9-A15, VXA, VUA, and R/W on the rising edge of Ø2.
M	-12V	-12 Vdc - Used to produce the -5 Vdc required by the EPROM's.
N,P		Not used.
R	MEM RDY	MEMORY READY - This signal permits the use of slow memory devices. When this command is a low level signal, the Ø1 and Ø2 clock signals are stretched, with Ø2 clock held high. The Ø2 clock signal remains at a high level until the module completes its memory operation and returns MEM RDY to a high level. A high level MEM RDY enables the clock to again generate the Ø1 and Ø2 clock signals.
S		Not used.
T	+12V	+12 Vdc - Used by module EPROM's.
U thru Z		Not used.
Ā,Ā		Not used.
Ā	AS0	ADDRESS SELECT 0 - Permits user to select desired logic level of address bit 13 of first (lower) memory block (U29-U36) address.
Ā	AS1	ADDRESS SELECT 1 - Permits user to select desired logic level of address bit 14 of first (lower) memory block (U29-U36) address.
Ā	AS2	ADDRESS SELECT 2 - Permits user to select desired logic level of address bit 15 of first (lower) memory block (U29-U36) address.
Ā	AS3	ADDRESS SELECT 3 - Permits user to select desired logic level of address bit 13 of second (upper) memory block (U1-U8) address.

TABLE 4-2. ROM/EPROM Module Bus Interface Connections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
H	D3	DATA bus (bit 3) - When enabled, this line provides a transfer between this module and any other plug-in module in the system. The data bus drivers on this module are in their off or high-impedance state except when the module is selected during a memory read operation.
J	D7	DATA bus (bit 7) - Same as D3 on pin H.
K	D2	DATA bus (bit 2) - Same as D3 on pin H.
L	D6	DATA bus (bit 6) - Same as D3 on pin H.
M	A14	ADDRESS bus (bit 14) - One of 16 address lines used to select a memory location on this module.
N	A13	ADDRESS bus (bit 13) - Same as A14 on pin M.
P	A10	ADDRESS bus (bit 10) - Same as A14 on pin M.
R	A9	ADDRESS bus (bit 9) - Same as A14 on pin M.
S	A6	ADDRESS bus (bit 6) - Same as A14 on pin M.
T	A5	ADDRESS bus (bit 5) - Same as A14 on pin M.
U	A2	ADDRESS bus (bit 2) - Same as A14 on pin M.
V	A1	ADDRESS bus (bit 1) - Same as A14 on pin M.
W,X,Y	GROUND	GROUND - +5 Vdc return.
1,2,3	+5V	+5 Vdc - Used for module logic circuits.
4		Not used.
5	RESET	RESET - This buffered input signal is used to precondition the MEM RDY circuitry whenever an external switch closure to ground or a low level RESET signal is received from the module containing the MPU.
6	R/W	READ/WRITE - When high, this input line enables data to be read from memory onto the data bus. When low, it enables data to be written to memory (if RAM's are used) from the data bus.
7		Not used.
8,9	GROUND	GROUND - -12 Vdc return.
10	VUA	VALID USER ADDRESS - This high level signal indicates that the user address on the address bus is valid.
11	-12V	-12 Vdc - Same as -12V on pin M.

TABLE 4-2. ROM/EPROM Module Bus Interface Connections (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
12 thru 15		Not used.
16	+12V	+12 Vdc - Same as +12V on pin T.
17 thru 24		Not used.
25	AS4	ADDRESS SELECT 4 - Permits user to select desired logic level of address bit 14 of second (upper) memory block (U1-U8) address.
26	AS5	ADDRESS SELECT 5 - Permits user to select desired logic level of address bit 15 of second (upper) memory block (U1-U8) address.
27,28		Not used.
29	D1	DATA bus (bit 1) - Same as $\overline{D3}$ on pin \overline{H} .
30	D5	DATA bus (bit 5) - Same as $\overline{D3}$ on pin \overline{H} .
31	D0	DATA bus (bit 0) - Same as $\overline{D3}$ on pin \overline{H} .
32	D4	DATA bus (bit 4) - Same as $\overline{D3}$ on pin \overline{H} .
33	A15	ADDRESS bus (bit 15) - Same as A14 on pin \overline{M} .
34	A12	ADDRESS bus (bit 12) - Same as A14 on pin \overline{M} .
35	A11	ADDRESS bus (bit 11) - Same as A14 on pin \overline{M} .
36	A8	ADDRESS bus (bit 8) - Same as A14 on pin \overline{M} .
37	A7	ADDRESS bus (bit 7) - Same as A14 on pin \overline{M} .
38	A4	ADDRESS bus (bit 4) - Same as A14 on pin \overline{M} .
39	A3	ADDRESS bus (bit 3) - Same as A14 on pin \overline{M} .
40	A0	ADDRESS bus (bit 0) - Same as A14 on pin \overline{M} .
41,42,43	GROUND	GROUND - +5 Vdc return.



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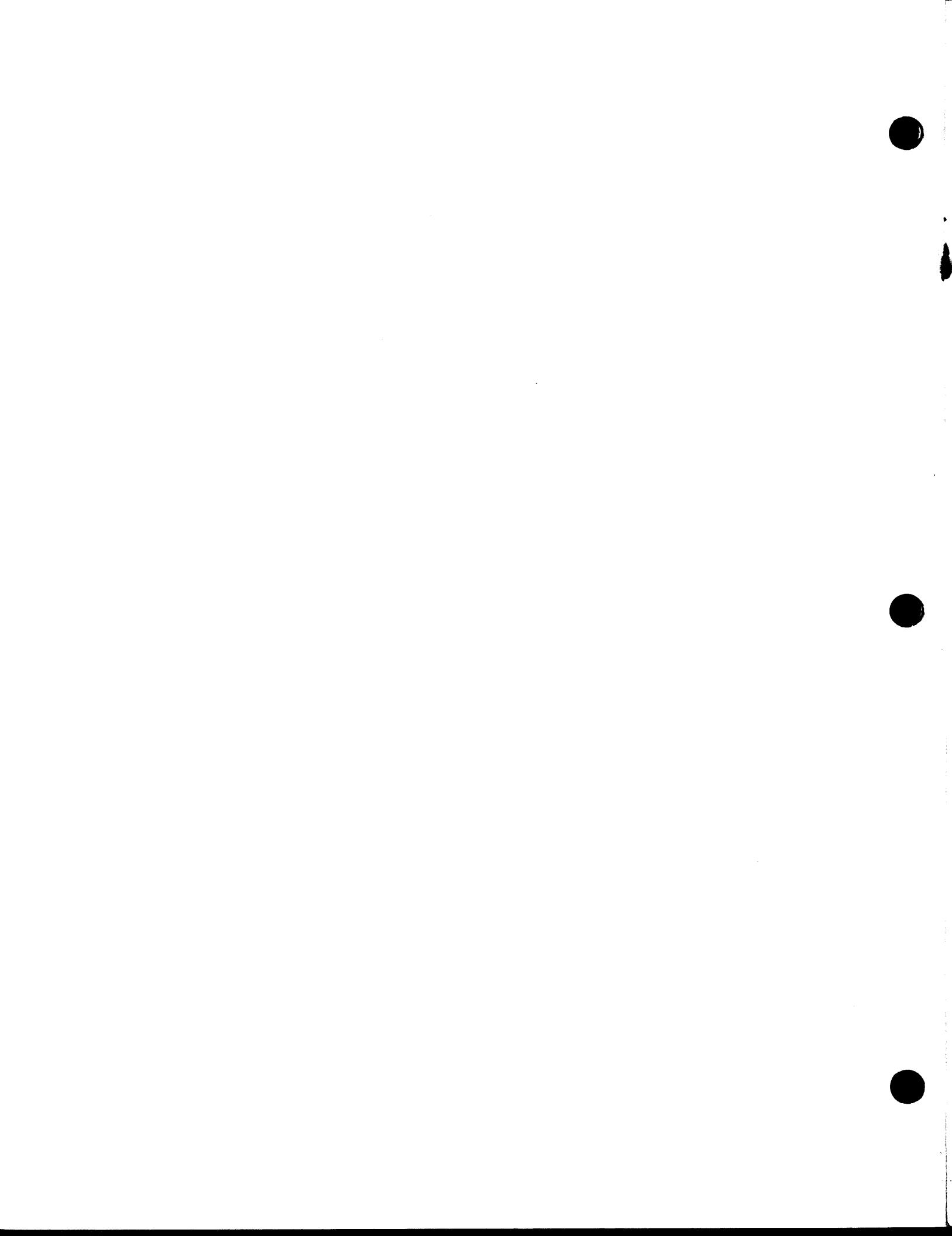
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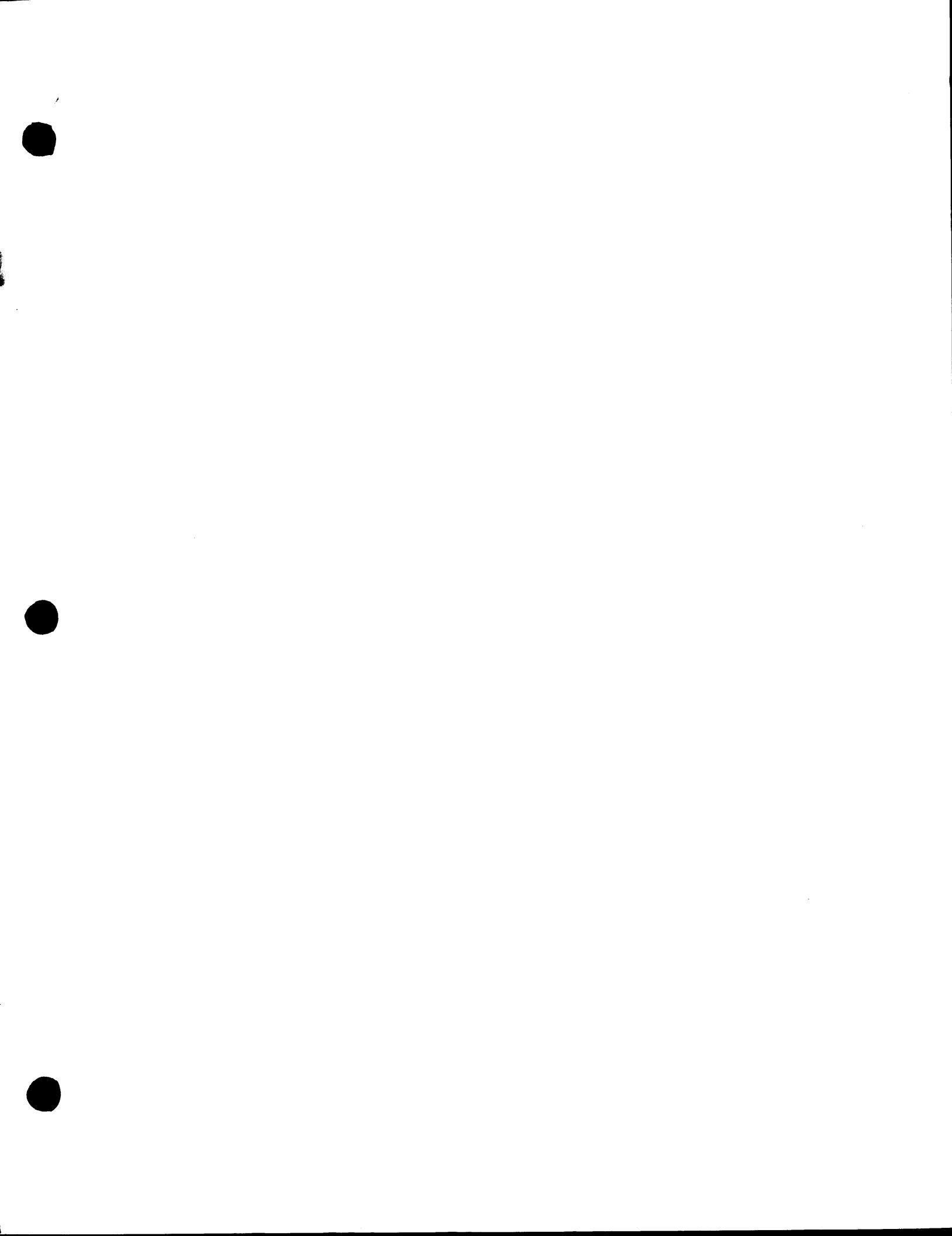
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