MOTOROLA
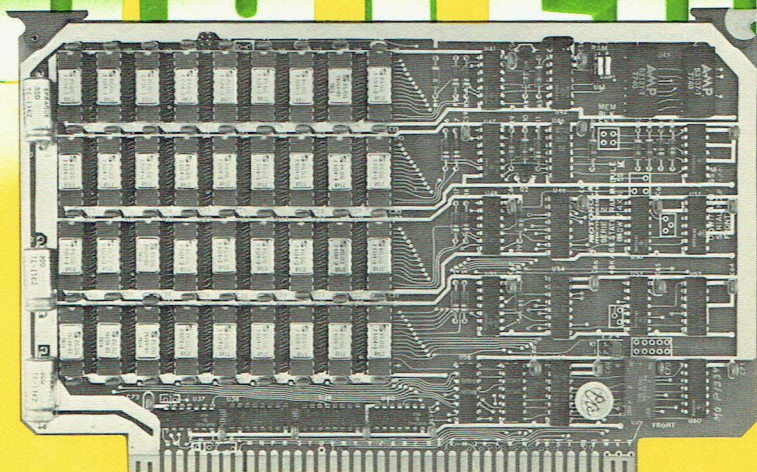
**MEX6808-21
MEX6808-22
MEX6816-21
MEX6816-22S**

8K/16K, 1.0 MHz and 2.0 MHz STATIC RAM MODULE

User's Guide

SYSTEMS

MICROSYSTEMS

MEX6808-21
MEX6808-22
MEX6816-21
MEX6816-22S

8K/16K, 1.0 MHz and 2.0 MHz Static RAM User's Guide

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CHAPTER I
GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, programming considerations, and theory of operation for the Static RAM Modules MEX6808-21, 8K, 1 MHz; MEX6808-22, 8K, 2 MHz; MEX6816-21, 16K, 1 MHz; and MEX6816-22S, 16K, 2 MHz. A typical module is shown in Figure 1-1. All address references within this manual are shown in hexadecimal unless otherwise indicated.

1.2 FEATURES

The features of the Static RAM Modules include:

- 16,384 x 8 bits of static memory organized into two 8192 x 8 bit memory arrays (16K module). 8192 x 8 bits, single array (8K module).

- Switch selectable base memory address for each memory array.

- Switch selectable RAM/ROM for each memory array.

- Series II DSB (Dynamic System Bus) provides Page Enable and Parity Error.

- Enable jumpers allow module to be addressed via VXA, VUA, or Page Enable.

- Bus drive capability.

- Even parity.

- TTL voltage compatible high impedance inputs.

- Standby/power down options provided on module.

- 1 MHz or 2 MHz memory speed.

1.3 SPECIFICATIONS

Static RAM specifications are identified in Table 1-1.

1.4 GENERAL DESCRIPTION

The 8K Static RAM Module, consisting of 18 (4096x1) bit static RAM devices, provides the system with 8192 x 8 bit bytes of random access memory. The memory is organized in a single array. A base address switch permits the user to select base memory addresses in 8K increments. A RAM/ROM switch permits the user to program the array to function as RAM or ROM.

The 16K Static RAM Module, consisting of 36 (4096x1) bit static RAM devices, provides the system with 16,384 x 8 bit bytes of random access memory. The memory is organized into two 8192 x 8 bit byte arrays. Two base address switches permit the user to select base memory addresses for both arrays in 8K increments. A RAM/ROM switch for each array permits the user to program the array to function as RAM or ROM.

The module circuitry generates and detects even parity. The module outputs a parity error signal to the system whenever a parity error is detected.

In the upper left-hand portion of the module is a 4-pin header, P2, known as the Dynamic System Bus (DSB). Parity error and page enable lines are connected to the DSB. The parity error and page enable lines are typically high speed lines and are, therefore, paired with a ground for twisted-pair connections.

The module will operate in a Power Fail/Power Down mode. In this mode, power is applied only to the memory arrays and the power fail/power down circuitry. A control signal from the system bus is required to maintain the mode of operation.

TABLE 1-1. Static RAM Module Specifications

| CHARACTERISTIC	SPECIFICATION
Memory Type	Depletion Load N-channel MOS static RAM (4096X1)
Memory Speed	1.0 MHz or 2.0 MHz
Memory Organization	16,384 x 8 bits (two 8192 x 8 bit arrays) 16K 8192 x 8 bits (single array) 8K
Parity	Even parity
Read Access Time	230 ns from leading edge of memory clock

Input Signals
  Commands
  Address
	
	TTL voltage compatible
	TTL voltage compatible

Data Bus	Three-state TTL voltage compatible
Operating Temperature	0 to 70°C
Power Requirements	+5 Vdc at 2.6A (MAX.)

Dimensions
  Width x Height
  Board Thickness
	
	9.75 in. x 6.15 in.
	0.062 in.
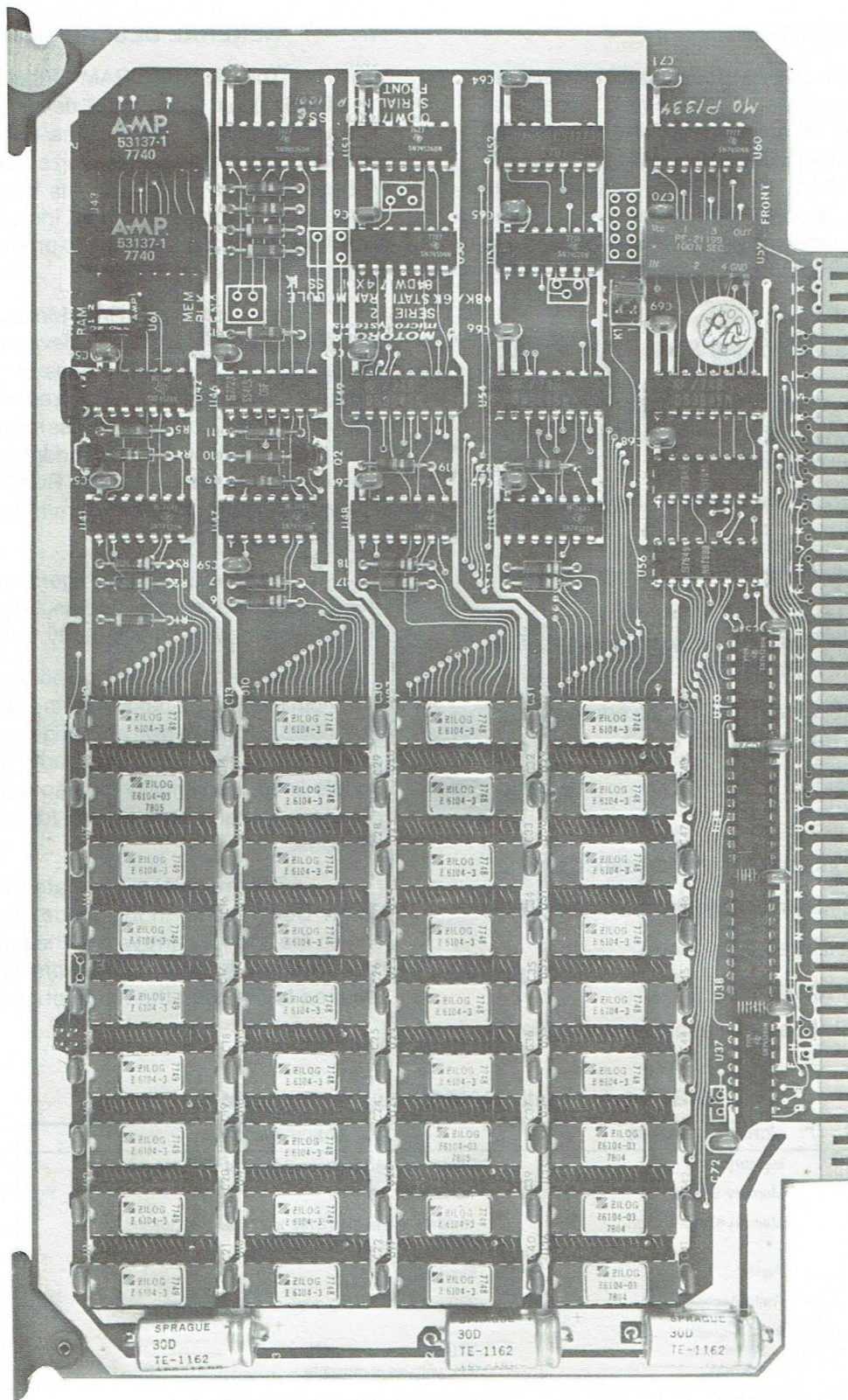
FIGURE 1-1. Typical Static RAM Module

CHAPTER 2
INSTALLATION INSTRUCTIONS, PROGRAMMING AND INTERCONNECTION CONSIDERATIONS

2.1 INTRODUCTION

This chapter provides the unpacking, inspection, installation, programming and interconnection instructions for the Static RAM Modules. This chapter also discusses the modules' interconnection signals, the function of the switches, and the programming considerations.

2.2 UNPACKING INSTRUCTIONS

Unpack the Static RAM Module from its shipping carton and, referring to the packing list, verify that all the items are present. Save the packing material for storing and shipping the module. If the shipping carton is damaged upon receipt, request that the carrier's agent be present while the module is being unpacked and inspected.

2.3 INSPECTION

The Static RAM Module should be inspected upon receipt for broken, damaged, or missing parts and physical damage to the printed circuit board.

2.4 HARDWARE PREPARATION

Figure 2-1 illustrates the location of the user options that are available on the Static RAM Modules. The 16K module has two arrays of independently addressable 8K bytes of static RAM with parity. The 8K module has a single array. Each array can be treated like a read-only memory via a RAM/ROM switch option. The modules are available for processor speeds of 1.0 or 2.0 MHz.

2.4.1 Base Address Selection

Two hex rotary switches are provided that allow each 8K half (array) of the module to be assigned a base address. Switch S1 (U43) selects the base address for Array 1, and switch S2 (U44) selects the base address for Array 2. The even positions are valid, as indicated in Table 2-1. The user must exercise care in making address assignments so that multiple modules are not assigned to overlapping address ranges.

TABLE 2-1. Base Memory Addresses

MEMORY LOCATION		SWITCH S1(U43) SWITCH S2(U44)
FROM	TO	SWITCH POSITION
0000	1FFF	0
2000	3FFF	2
4000	5FFF	4
6000	7FFF	6
8000	9FFF	8
A000	BFFF	A
C000	DFFF	C
E000	FFFF	E

2.4.2 Memory Map Assignment

The user must assign the module to either one of the three memory map modes:

VUA — Valid User Address
VXA — Valid Executive Address
Page Enable — For multiple "pages" of 64K bytes

A jumper at K1 is used for this purpose, as illustrated below.
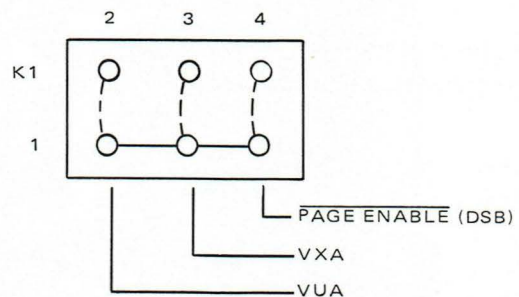
2.4.3 Parity Option

The signal $\overline{\text{PARITY ERROR}}$ is connected by the printed circuitry to both P1, pin W and P2, pin 17 of the DSB, as shown here.
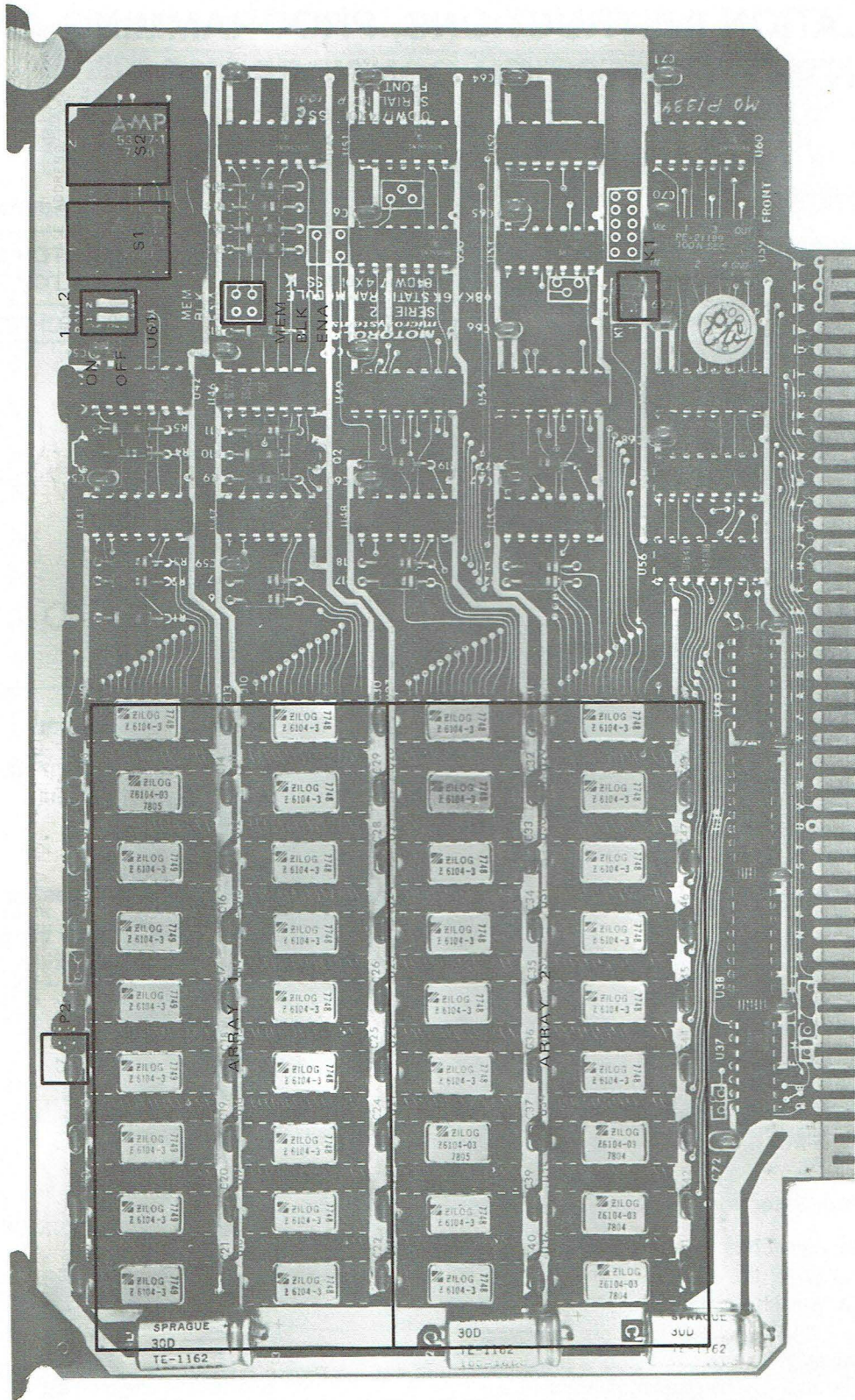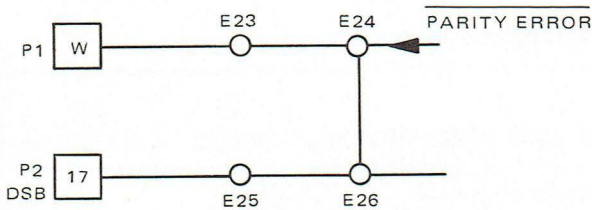
FIGURE 2-1. Typical Static Memory Module

If, for some reason, the user needs to disconnect one or both of these connections, jumpers E23-E24 and E25-E26 are provided.

2.4.4 Disable Block Option

At the area labeled MEM-BLK-ENA, printed circuitry exists that may be cut in order to disable one of the arrays. The circuitry is located on the back of the module. On 8K modules, Array 1 is disabled.
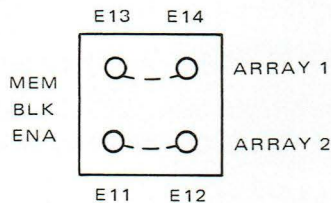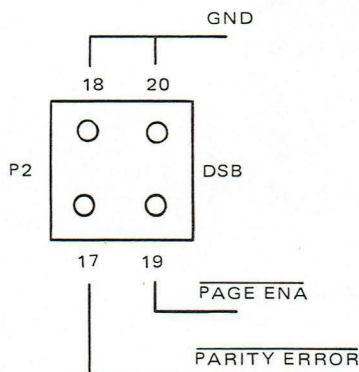

2.4.5 RAM/ROM Option

Two rocker switches are provided at location U61 to configure each array as RAM or ROM. Switch 1 controls Array 1, and Switch 2 controls Array 2. The OFF position selects RAM; the ON position selects ROM.

2.4.6 Dynamic System Bus

The four pin connector P2 has two signal connections: PAGE ENABLE and PARITY ERROR, each with ground.

2.4.7 Power Fail/Power Down Option

When battery power backup is supplied for memory standby, the Power Fail/Power Down mode can be initiated. To operate on this mode, a jumper (18 AWG) must be installed between E21 and E22 on the module. Cut track as indicated in sketch below.
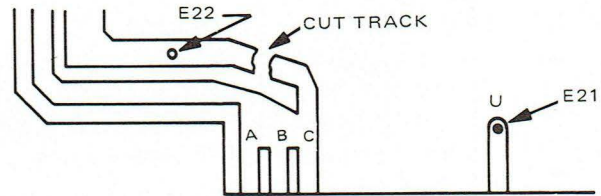
2.4.8 Valid Memory Address (VMA) Option

The Static RAM Module may be used in a system without a DEbug Module. To do this, a jumper must be installed between E9 and E10, and the circuit track cut between E8 and E9 as shown below:
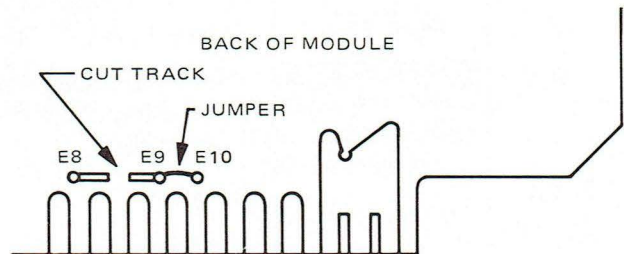
Refer to paragraph 2.4.2 and jumper K1 for VUA operation.

2.5 INSTALLATION INSTRUCTIONS

Install the Static RAM Module as follows:

a. Turn power OFF on equipment in which module is being installed.

CAUTION
INSERTING MODULE WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON MODULE.

b. Install module in the selected card slots. The module may be installed in any of the 14 card slots in the system.

c. Turn power ON.

2.6 MODULE INTERCONNECTIONS

The Static RAM Module interconnects directly with the system bus. The bus signals are identified in Table 2-2. This table lists each pin connection, signal mnemonic, and signal characteristic. Table 2-3 identifies the Dynamic System Bus interface signals on connector P2.

2-3

TABLE 2-2. Connector P1 Bus Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A,B,C	+5V	+5Vdc — Used by the module logic circuits
D,E		Not used
F	VMA	VALID MEMORY ADDRESS — This input is available, jumper selected, when the Static RAM is used without the DEbug Module.
H		Not used
J	$\phi2$	Phase 2 clock signal
K		Not used
L	MEM CLK	MEMORY CLOCK — This signal is an ungated TTL level $\phi2$ clock used to refresh memory in the module.
M–T		Not used
U	STANDBY	STANDBY POWER — This input is available, jumper selected, when battery power backup memory is supplied.
V	$\overline{\text{PWR-FAIL}}$	POWER FAIL — This signal line used with STANDBY battery power backup.
W	$\overline{\text{PARITY-ERROR}}$	PARITY ERROR — This signal line is normally high until a parity error is detected by the parity check circuit on the module at which time the signal will go low for one clock cycle.
X,Y,Z		Not used
$\overline{\text{A}}$ — $\overline{\text{F}}$		Not used
$\overline{\text{H}}$	$\overline{\text{D3}}$	DATA bus (bit 3) — One of 8 bidirectional data lines used to provide a two-way data transfer between the static RAM and any other plug-in modules in the system.
$\overline{\text{J}}$	$\overline{\text{D7}}$	DATA bus (bit 7) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
$\overline{\text{K}}$	$\overline{\text{D2}}$	DATA bus (bit 2) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
$\overline{\text{L}}$	$\overline{\text{D6}}$	DATA bus (bit 6) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
$\overline{\text{M}}$	A14	ADDRESS bus (bit 14) — One of 16 address lines used to select a memory location on this module.
$\overline{\text{N}}$	A13	ADDRESS bus (bit 13) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{P}}$	A10	ADDRESS bus (bit 10) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{R}}$	A9	ADDRESS bus (bit 9) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{S}}$	A5	ADDRESS bus (bit 6) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{T}}$	A2	ADDRESS bus (bit 5) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{U}}$	AZ	ADDRESS bus (bit 2) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{V}}$	A1	ADDRESS bus (bit 1) Same as A14 on P1-$\overline{\text{M}}$
$\overline{\text{W}},\overline{\text{X}},\overline{\text{Y}}$	GND	GROUND
1,2,3	+5V	+5Vdc — Used by the module logic circuits.
4		Not used

TABLE 2-2.   Connector P1 Bus Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
5	$\overline{\text{RESET}}$	RESET — This buffered input signal provides reset signal to the parity error circuit on the module.
6	R/$\overline{\text{W}}$	READ/WRITE — This signal is generated by the MPU and indicates whether the MPU is performing a memory read (high or write (low) operation. The normal standby state of this signal is read (high). Also, when the MPU is halted, this signal will be in the read state.
7,8,9		Not used
10	VUA	VALID USER'S ADDRESS — This signal, jumper selectable, is produced by the DEbug module. When high, this signal indicates that the address on the address bus is valid and the MPU is NOT addressing the EXbug program.
11–16		Not used
17	STANDBY	STANDBY POWER — Same as STANDBY on P1-U
18		Not used
19	VXA	VALID EXECUTIVE ADDRESS — A high level signal, jumper selectable, generated by the DEbug module in place of the VUA signal when the system is operating in the Dual Map mode and the EXbug Program is addressing the Executive portion of the memory map.
20–28		Not used
29	$\overline{\text{DI}}$	DATA bus (bit 1) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
30	$\overline{\text{D5}}$	DATA bus (bit 5) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
31	$\overline{\text{D0}}$	DATA bus (bit 0) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
32	$\overline{\text{D4}}$	DATA bus (bit 4) Same as $\overline{\text{D3}}$ on P1-$\overline{\text{H}}$
33	A15	ADDRESS bus (bit 15) Same as A14 on P1-$\overline{\text{M}}$
34	A12	ADDRESS bus (bit 12) Same as A14 on P1-$\overline{\text{M}}$
35	A11	ADDRESS bus (bit 11) Same as A14 on P1-$\overline{\text{M}}$
36	A8	ADDRESS bus (bit 8) Same as A14 on P1-$\overline{\text{M}}$
37	A7	ADDRESS bus (bit 7) Same as A14 on P1-$\overline{\text{M}}$
38	A4	ADDRESS bus (bit 4) Same as A14 on P1-$\overline{\text{M}}$
39	A3	ADDRESS bus (bit 3) Same as A14 on P1-$\overline{\text{M}}$
40	A0	ADDRESS bus (bit 0) Same as A14 on P1-$\overline{\text{M}}$
41,42,43	GND	GROUND

TABLE 2-3. Connector P2 Dynamic System Bus

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
17	$\overline{\text{PARITY ERROR}}$	PARITY ERROR — Same as PARITY ERROR on P1-W Ground
18	GND	GROUND
19	$\overline{\text{PAGE ENA}}$	PAGE ENABLE — If a user builds a controller than can convert the VMA signal from the MPU into one of several pages, an unlimited number of "pages" of 64K bytes can be realized. This signal port is jumper selectable.
20	GND	GROUND

CHAPTER 3
THEORY OF OPERATION

3.1   INTRODUCTION

This chapter provides a block diagram description of a Static RAM Module. The block diagram is shown in Figure 3-1; a schematic is shown in Figure 3-2.

3.2   THEORY OF OPERATION

The Static RAM Module receives the 16 address lines A0 through A15, a MEM CLK and phase symbol $\phi2$ timing signals, the R/W command, and a VA command during each memory cycle. The VA signal is either VUA, VXA, or PAGE ENA. It is a jumper option at K1 and is selected by the user. The Data Bus, D0-D7, transfers data between the memory module and the system bus. RESET and PWRFAIL are control inputs. PARITY ERROR is an output signal from the module.

In a memory operation, addresses A0 through A15, R/W and VA are inverted by the ADDRS LATCH and become MA0 through MA15, MR/W, and MVA, respectively. The ADDRS LATCH applies MA0 through MA11 to the internal address inputs of the RAMS in the memory arrays, MA12 through MA15 and MVA to the ARRAY SELECT LOGIC, and MR/W to the DATA/PARITY LOGIC.

The ARRY SELECT LOGIC decodes MA13 through MA15, MVA and the inputs from BASE ADDRS S2 and determines if the memory module is addressed and, if so, what array will respond. An address for MEM ARRAY 1 will cause ARRAY 1 ENA to go high (true). An address for MEM ARRAY 2 will cause ARRAY 2 ENA to go high (true). MA12 and MA12 determine whether the HIGH or LOW order of MEM ARRAY 1 or MEM ARRAY 2 is addressed. When MA12 is high, the low order is addressed; when MA12 is high, the high order is selected. The VADDRS output also goes low (low true) when the memory module is addressed. It is a control input to the DATA/PARITY logic.

On the leading edge of MEMCLK, after A0 through A15, R/W, and VA become stable, the TIMING LOGIC generates CECLK, and ADDRS LATCH ENA. CECLK is the timing input to the ARRAY CONTROL LOGIC and determines the time that the addressed RAMs are enabled. During ADDRS LATCH ENA, A0 through A15, R/W, and VA are stored in the ADDRS LATCH.

The ARRAY CONTROL LOGIC decodes MA12, MA12, ARRAY 1 ENA, and ARRAY 2 ENA, RAM/ROM S1, RAM/ROM S2, and determines which memory array is addressed. The CE for the addressed array (CE1L, CE1H, CE2L, or CE2H) goes low (low true) during CECLK.

3.2.1   Memory Read

During a memory read operation (R/W HIGH) and after the chip select is enabled, data at the location specified by the address inputs appears at D0 OUT through D7 OUT and PAR OUT. Also, the DATA/PARITY LOGIC generates DOE, connecting the 3-state DATA BUS DRIVERS to the DATA BUS. DOG is low (true) during $\phi2$, and data is transferred from the memory array to the DATA BUS during this time.

Data from the memory arrays is checked for even parity by the PARITY DETECTOR. When a parity error is detected, PARERR is asserted and the DATA/PARITY LOGIC generates PARITY ERROR on the falling edge of $\phi2$. PARITY ERROR remains true (low level) until the next falling edge of $\phi2$ and PARERR is not asserted.

60 ns after the training edge of $\phi2$, CECLK and ADDRS LATCH ENA go false, disabling the memory array and releasing the ADDRS LATCH.

3.2.2   Memory Write

During a memory write operation, the memory location is selected as in the memory read operation. The R/W signal is low, indicating a write operation, and the MPU transfers data to the DATA BUS during the last half and slightly beyond the training edge of $\phi2$. The DATA/PARITY LOGIC decodes VADDRS and MR/W, and disables DATA LATCH ENA (high false) during M$\phi2$. Data on the DATA BUS is inverted by the DATA BUS LATCH and becomes D0IN-D7IN. D0IN-D7IN is applied to DATA IN of the Memory Arrays and to the PARITY GEN. The PARITY GEN outputs even parity PARIN, which is also applied to DATA IN. 60 ns after the leading edge of $\phi2$, the TIMING LOGIC generates WECLK and applies it to the ARRAY CONTROL LOGIC. The ARRAY CONTROL LOGIC asserts WE to the addressed memory array for the duration of WECLK if its RAM/ROM switch is in the RAM position. RAM/ROM S1 controls MEM ARRAY 1, and RAM/ROM S2 controls MEM ARRAY 2. If the switch for the addressed array is in the ROM position, the WE is not asserted and the array can only be read. When $\phi2$ goes low, DATA IN LATCH ENA goes low (low true) latching D0IN–D7IN. D0IN–D7IN will be stored until $\phi2$ of the next write operation. 60 ns after the falling $\phi2$, WECLK goes low and WE for the addressed array goes high, disabling its write enable input. Data is latched into the addressed memory location at this time. The CECLK goes low and CE for the addressed array goes high, disabling the array. This is followed by ADDRS LATCH ENA going high, unlatching the ADDRS LATCH. A new memory cycle can be initiated 135 ns after the trailing edge of $\phi2$.

3.2.3 Power Fail

The Static RAM Module can operate with a POWER-FAIL (POWER-DOWN) option. During this mode, power is applied only to the Memory Array and associated power down circuitry. In the Power-Fail/ Power Down mode, PWR-FAIL is asserted (low true) by the system. The PWR FAIL LOGIC applies $\overline{MP/F}$ to the ARRAY CONTROL LOGIC, inhibiting all MEM ARRAY CE's even during time +5V is reduced to 0V.
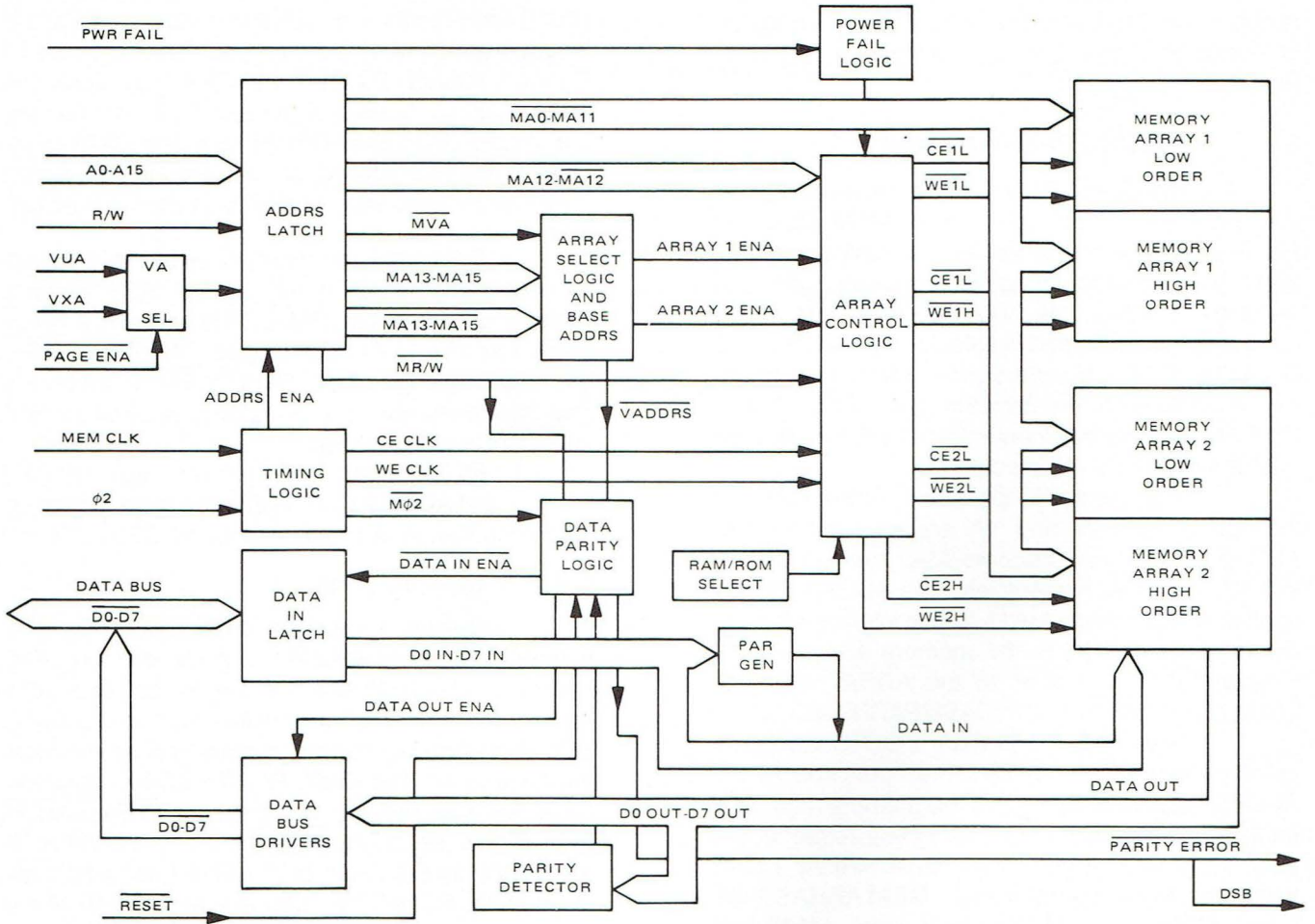

Figure 3-1. Static RAM Block Diagram

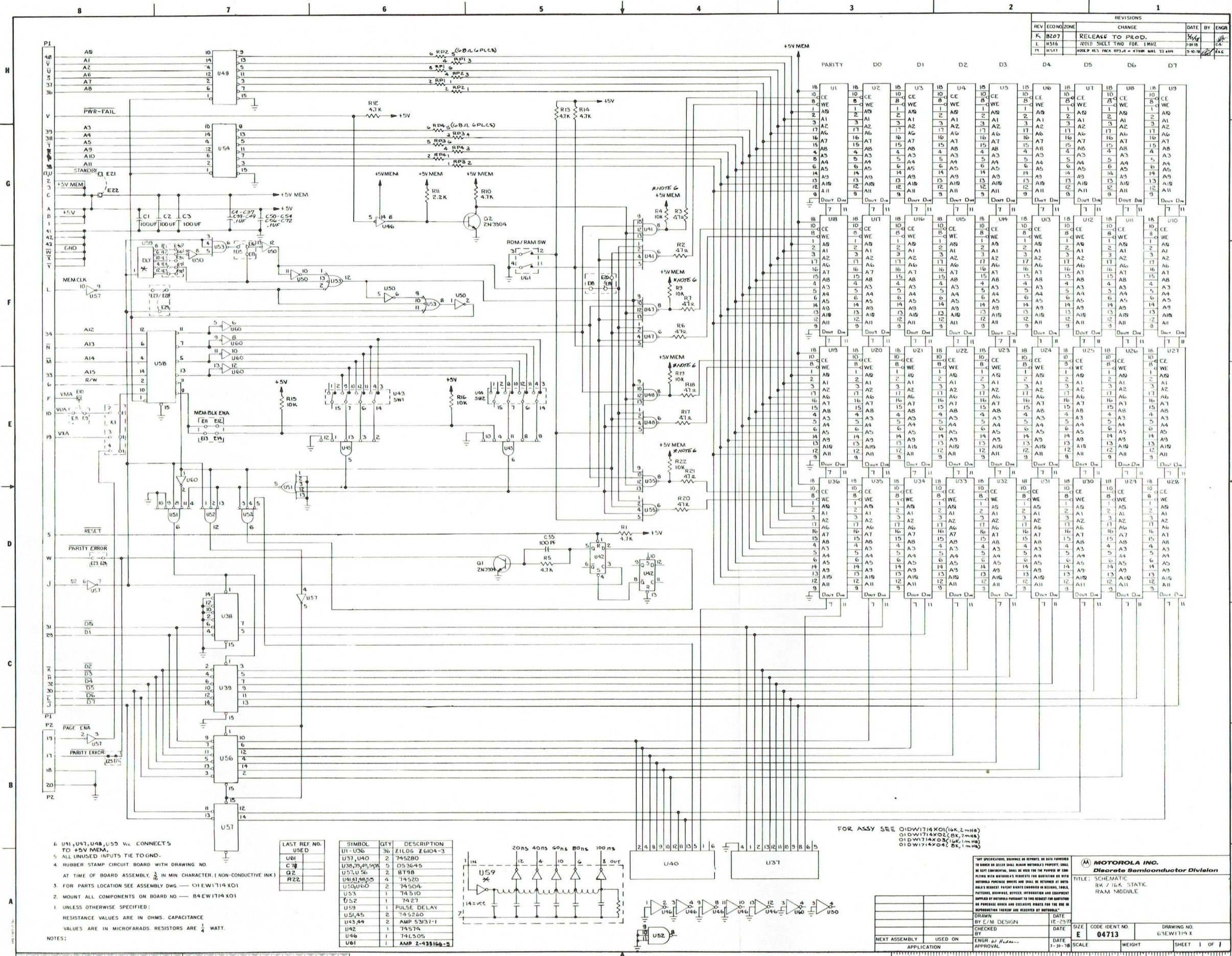FIGURE 3-2. Static RAM Schematic Diagram

CHAPTER 4
PARTS

4.1   INTRODUCTION

This chapter provides the parts list and parts location for a Static RAM Module (Table 4-1 and Figure 4-1). The parts list reflects the latest issue of the hardware at the time of printing.

TABLE 4-1.   Static RAM Module Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
	84DW6714X01	Printed Wiring Board, Static RAM	L
	55NW9403AXX (NOTE)	Ejector, Circuit Card with Roll Pin Attachment, 2 required	L
C1,C2,C3	23NW9618A09	Capacitor, Electrolytic, 100μF @ 16 Vdc	L
C4-C37, C39-C54, C56-C72	21NW9702A09	Capacitor, Fixed, Ceramic, 0.1 μF @ 50 Vdc	L
C38		Not used	
C55	21NW9605A05	Capacitor, Fixed, Mica, 100 pF @ 500 Vdc	L
K1	28NW9802B88	Header, Double Row Post, 6 Pin	L
P2	28NW9802C29	Header, Double Row Post, 4 Pin	L
Q1, Q2	48NW9610A14	Transistor, 2N3904	L
R1,R5,R10,R12, R13,R14	06SW-124A65	Resistor, Fixed, Carbon, 4.7K Ohm, 5%, ¼W	L
R2,R3,R6,R7, R17,R18,R20,R21	06SW-124A17	Resistor, Fixed, Carbon, 47 Ohm, 5%, ¼W	L
R4,R9,R15,R16 R19, R22	06SW-124A73	Resistor, Fixed, Carbon, 10K Ohm, 5%, ¼W	L
R8		Not Used	
R11	06SW-124A57	Resistor, Fixed, Carbon, 2.2K Ohm, 5%, ¼W	L
RP1,RP2,RP3,RP4	51NW9626A43	Resistor Network, 3/68 Ohm (1.0 MHz only)	L
U1-U36	51NW9615E90	I.C., 2.0 MHz (NOTE) (16K)	L
U19-U36	51NW9615E90	I.C., 2.0 MHz (NOTE) (8K)	L
U1-U36	51NW9615E37	I.C., 1.0 MHz (NOTE) (16K)	L
U19-U36	51NW9615E37	I.C., 1.0 MHz (NOTE) (8K)	L

TABLE 4-1. Static RAM Module Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION	EFFEC-TIVITY
U37	51NW9615E35	I.C., 74S280A	L
U38,U39,U49,U54,U58	51NW9615E32	I.C. DS3645N	L
U40	51NW9615F12	I.C. 74LS280 (1.0 MHz only)	L
U41,U47,U48,U55	51NW9615D92	I.C. SN74S20N	L
U42	51NW9615C95	I.C. SN74S74N	L
U43, U44	40NW9801A31	Switch, Hex., 53137-1	L
U45, U51	51NW9615E67	I.C. SN74S260N	L
U46	51NW9615D98	I.C. SN54LS05J	L
U50, U60	51NW9615C96	I.C. SN74S04N	L
U52	51NW9615D19	I.C. MC7427P	L
U53	51NW9615E27	I.C. SN74S10N	L
U56, U57	51NW9615C36	I.C. 8T98	L
U59	01NW9804B35	Module, Digital Delay, 100ns	L
U61	40NW9801A69	Switch, DIL, 2PST, 2POS.	L
	28NW9802C04	Socket, I.C., 18 pin, 36 required	L
	29NW9805A91	Jumper, 2 position, use at KI	L

NOTE: Integrated circuits are supplied by several manufacturers.

    51NW9615F90 — Zilog   P/N Z6104PS-3
    51NW9615F37 — TI   P/N 4044-30
    55NW9403A05 — For 1 MHz modules
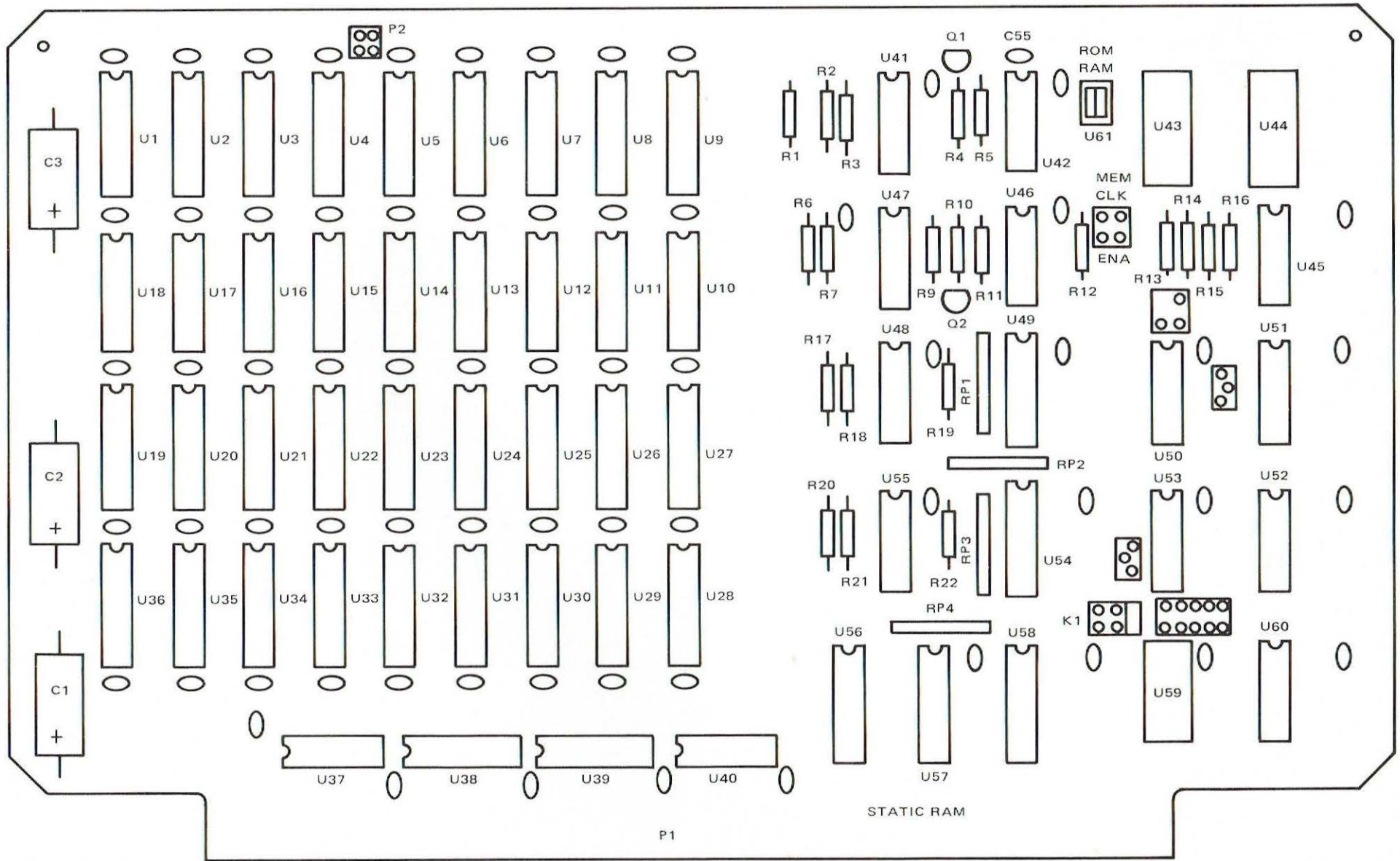   55NW9403A10 — For 2 MHz modules

FIGURE 4-1. Typical Static RAM Parts Location

EXORciser II/EXORterm 200/220

with 16K Static RAM Modules

ADDENDUM
to

MEX6808-21
MEX6808-22
MEX6816-21
MEX6816-22S

8K/16K, 1.0 MHz and 2.0 MHZ
STATIC RAM MODULES

LIMITED USE OF 16K STATIC RAM MODULES
in EXORciser II, EXORterm 200, and EXORterm 220

Because of the high power consumption of the 16K Static RAM Modules, MEX6816-
and MEX6816-22S, certain user configurations of EXORciser II and EXORterm 200,
could exceed the 15 ampere current rating of the power supply.

With a standard module configuration,

- -- MPU
- -- DEbug
- -- Floppy Disk Controller
- -- Printer Interface
- -- 16K Static RAM
- -- 16K Static RAM

the average of 5 volt current requirement is 10 amperes. The average current
per 16K Static RAM Module is 2.7 amperes. EXORciser II, therefore, is limited
to 48K of static memory, and EXORterm 200/220 to 32K of static memory, since
the CRT logic draws an additional 4.2 amperes.