MOTOROLA Semiconductors

MEX6815-1

Advance Information

EXORciser
8K DYNAMIC RAM
MODULE

8K DYNAMIC RAM MODULE

The MEX6815-1 8K Dynamic RAM Module, consisting of 16 MCM6605L-1 N-Channel memory circuits, provides the EXORciser with 8192 x 8 bits of dynamic random access memory. This memory is organized into two separate 4096-byte memory arrays. The module base memory address selection switches permit the user to select the base memory address for each memory array in 4K byte increments (0000, 4096, 8192, etc.). The RAM/ROM switch for each memory array permits its respective memory array to be used as RAM or pseudo ROM (protecting the memory contents by inhibiting the memory write function). The module refreshes its dynamic memory devices on a cycle stealing basis approximately once every 60 μs.

In systems using multiple 8K Dynamic RAM Modules, one module (master refresh module) is used to control the memory refresh operation of the other modules (slave refresh modules).

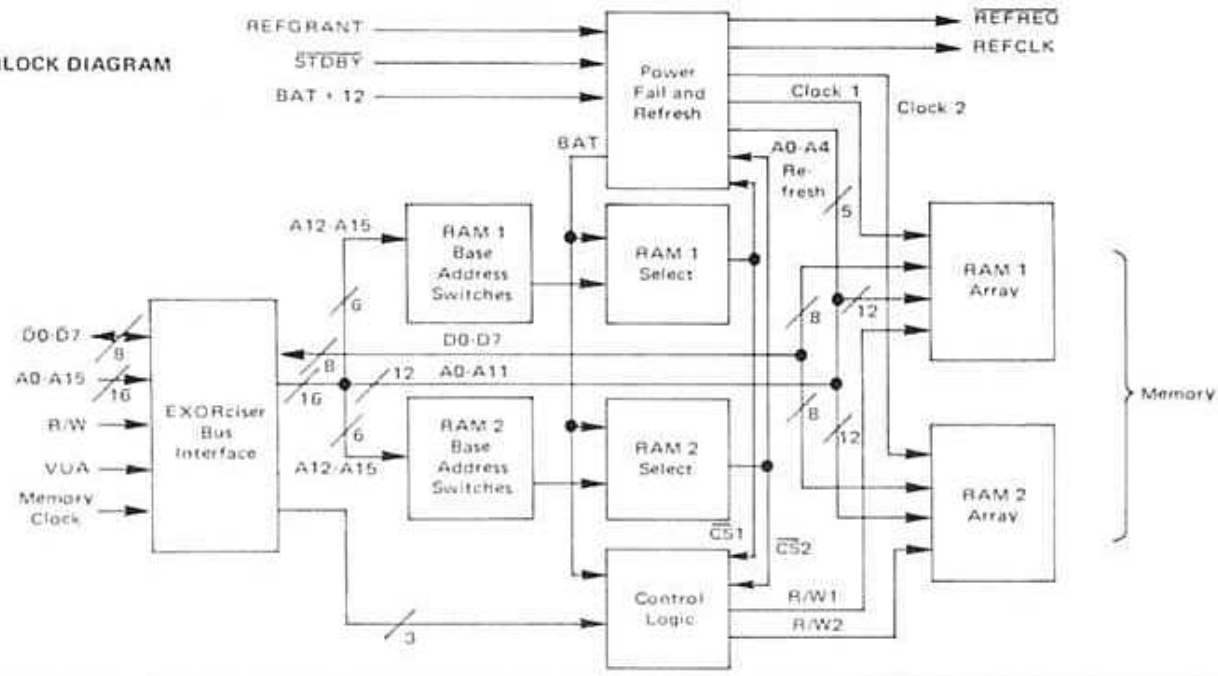
The 8K Dynamic RAM Module can be used with an external battery backup circuit to provide refreshing when power is removed from the primary of the EXORciser power supply transformer. This refresh capability enables the module to retain its data during a power off condition.

- TTL Voltage Compatible
- Three-State Data Bus
- 8192 x 8 Bits of Dynamic MOS Memory in Two 4096-Byte Arrays
- Switch-Selectable Base Location Address for Each Array
- Each Array Switch-Selectable as a RAM or ROM (RAM Protected by Inhibiting Memory Write Function)
- Cycle-Stealing Memory Refresh
- Memory Refresh Capability During Power-Fail Condition when Using External Battery Backup
- Bus Driver Capability

EXORciser

8K DYNAMIC RAM MODULE

BLOCK DIAGRAM



MODULE SPECIFICATIONS

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification	Value
Memory Type	N-channel MOS dynamic RAM
Memory Organization	8192 x 8 bits organized into two 4096 x 8 bit arrays
Read Access Time	350 ns from memory clock typical, 400 ns maximum
Cycle Time	750 ns typical, 1 μs minimum
Input Signals A0-A11 Logic "0" Logic "1" A12-A15 and Control Lines Logic "0" Logic "1"	TTL voltage compatible 0.0-0.8 V (-400 μA max at 0.5 V) 2.0-5.25 V (10 μA max at 4.5 V) 0.0-0.85 V (-200 μA max at 0.4 V) 2.0-5.25 V (25 μA max at 5.25 V)
Data Bus Input Logic "0" Input Logic "1" Output Logic "0" Output Logic "1" Output Off-State Leakage Current	Three-state TTL voltage compatible 0.0-0.85 V (-200 μA max at 0.4 V) 2.0-5.25 V (25 μA max at 5.25 V) 0.5 V max at −40 mA through a resistor to ground 2.6 V min at −10 mA through a resistor to V_{CC} 100 μA max at 2.6 V
Operating Temperature	0 to 70°C
Power Requirements	5 Vdc at 860 mA 12 Vdc at 300 mA*
Powerfail Refresh	5 Vdc not used 12 Vdc at 25 mA maximum
Dimensions Width Height Thickness	 9.75 in. 5.75 in. 0.062 in.

*Power consumption is dependent on the number of memory accesses of the module.

EXORciser INTERFACE SIGNALS

The MEX6815-1 8K Dynamic RAM Module interfaces directly with the EXORciser bus using the following signals. These signals permit the EXORciser to have complete control over the 8K Dynamic RAM Module.

Data Bus ($\overline{D0}$-$\overline{D7}$) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the 8K Dynamic RAM Module. The data bus drivers and receivers on the 8K Dynamic RAM Module are three-state devices. The data bus drivers and receivers are in their off or high-impedance state except when this module is selected in a memory read or a memory write operation.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the selected memory address to the 8K Dynamic RAM Module. The MPU Module controls the operation of these three-state lines.

Read/Write (R/W) – This MPU Module output signal indicates to the 8K Dynamic RAM Module whether the EXORciser is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the MPU Module is halted, this signal will be in the read state.

Valid User's Address (VUA) – This signal indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program (upper 4K bytes of memory).

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi1$ and $\phi2$ clock signals. The 8K Dynamic RAM Module uses this signal to control its timing.

Refresh Clock (REFCLK) – This clock signal is generated by the 8K Dynamic RAM Module to refresh its memory. In systems using multiple 8K Dynamic Modules, the master refresh module uses this signal to refresh the slave refresh modules.

Stand By ($\overline{STDBY}$) – This line is a low level during a powerfail condition and a high level during normal EXORciser operation.

Refresh Request ($\overline{REFREQ}$) – This signal, when present, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the $\phi1$ and $\phi2$ clock signals with $\phi1$ high and, through the Refresh Grant command, instructs the 8K Dynamic RAM Module to refresh its memories. The 8K Dynamic RAM Module generates this pulse approximately once every 60 μs.

Refresh Grant (REFGRANT) – This signal, when present, instructs the 8K Dynamic RAM Module to refresh its memories.

Battery + 12 (BAT + 12) – This is the 12-volt source for the MCM6605-1 memory circuits.