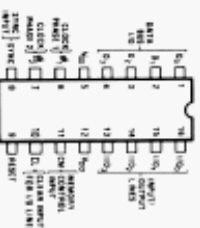


256 x 8 MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT

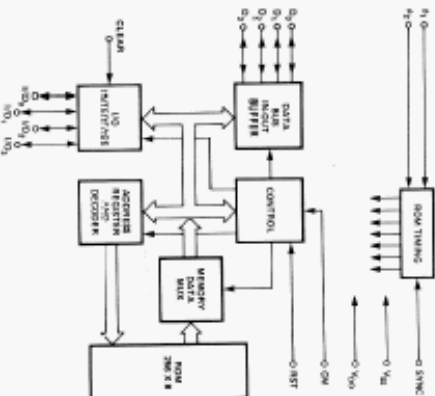
- Direct Interface to MCS-40™
4 Bit Data Bus
- I/O Port Low-Power TTL
Compatible
- 16 Pin Dual In-Line Package
- Standard Operating
Temperature Range of
0° to 70° C
- Also Available With -40° to
+85° C Operating Range

The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40™ devices.

PIN CONFIGURATION



BLOCK DIAGRAM



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
14	D ₀ , D ₃ /Neg.	Bidirectional data bus. All address and data communication between the processor and ROM is handled by these lines.
5	V _{SS}	Most positive supply voltage.
6,7	φ ₁ , φ ₂ /Neg.	Non-overlapped clock signals which determine device timing.
8	SYN/C/Neg.	System synchronization signal generated by processor.
9	RESET/Neg.	Reset input. A negative level (V _{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
10	CL/Neg.	Clear input for I/O lines. A negative level on this pin will clear the I/O buffers. This pin may be driven by a TTL output and a 1K pull-up to V _{SS} .
11	CM-ROM/Neg.	CM-ROM enable generated by the processor.
12	V _{DD}	Main supply voltage value. Must be V _{SS} - 15.0V ±5%.
13,16	I/O ₀ -I/O ₃ /Neg.	A single I/O port consisting of 4 bidirectional and selectable lines.

Functional Description

Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, φ₁ and φ₂, and a SYNC signal supplied by the CPU. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command ROM Line (CM-ROM) is also provided and it is used to select a ROM bank (group of 16 ROM's).

During the two time periods of the instruction cycle (M₁ & M₂) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation. All internal flip-flops (including the output register) will be reset when the RESET time goes low (V_{DD}).

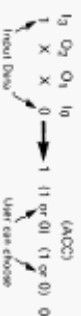
I/O Options

Each I/O pin on each ROM can be uniquely chosen to be either an input or output line by metal option. Also each input or output can either be inverted or direct. When the pin is chosen as an input it may have an on-chip resistor connected to either V_{DD} or V_{SS}.

Instruction Execution

The 4001 responds to the following instructions.

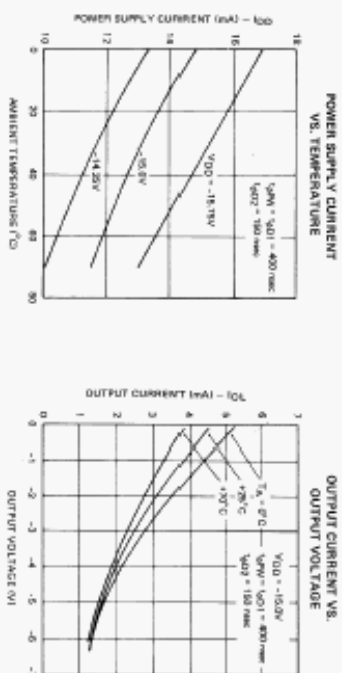
- SRC Instruction** (Send address to ROM and RAM)
When the CPU executes an SRC instruction it will send out 8 bits of data during X₂ and X₃ and will activate the CM-ROM and send CM-RAM line at X₂. Data at X₂ (representing the contents of the first register of the register pair addressed by the SRC instruction) with simultaneous presence of CM-ROM, is interpreted by the 4001 as the chip number of the unit that should later perform an I/O operation. Data at X₃ is ignored.
- WRR - Write ROM Port**
The contents of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed on the same chip. The ACC contents and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O₀). No operation is performed on I/O lines coded as inputs.
- RDR - Read ROM Port**
The data present at the input lines of the previously selected ROM chip is transferred to the accumulator. If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs. When an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed, the transfer is as shown below:



Timing Consideration

In the ROM mode of operation the 4001 will receive an 8 bit address during A₁ and A₂ times of the instruction cycle and a chip number, together with CM-ROM, during A₃ time. When CM-ROM is present, only the chip whose metal option code matches the chip number code sent during A₃ is allowed to send data out during the following two cycles, M₁ and M₂. The activity of the 4001 in the ROM mode ends at M₂.

Typical D.C. Characteristics

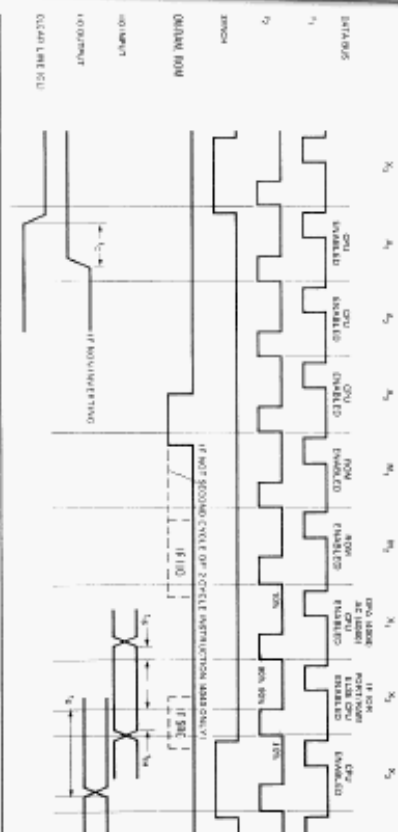


A.C. Characteristics

 $T_A = 0^\circ\text{C to } 70^\circ\text{C}, V_{SS} = V_{DD} = 15\text{V} \pm 5\%$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CY}	Clock Period	1.35		2.0	μs	
t_{set}	Clock Rise Time		50		ns	
t_{fall}	Clock Fall Time		50		ns	
t_{setw}	Clock Width	380		480	ns	
t_{setw}	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
t_{setw}	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_{w}	Data In, CM, SYNC Write Time	350		100	ns	
$t_{\text{h}}[1,2]$	Data In, CM, SYNC Hold Time	40		20	ns	
$t_{\text{set}}[2]$	Set Time (Reference)	0			ns	
t_{ACC}	Data Out Access Time					
	Data Lines					$C_{\text{OUT}} = 500\text{pF}$ Data Lines
	CM-RAM					530 ns
	CM-RAM					530 ns
	CM-RAM					160pF CM-RAM
	CM-RAM					50pF CM-RAM
t_{OH}	Data Out Hold Time	50		150	ns	$C_{\text{OUT}} = 20\text{pF}$
t_{IS}	I/O Input Set Time	50			ns	
t_{IH}	I/O Input Hold Time	100			ns	
t_{O}	I/O Output Delay			1500	ns	$C_{\text{OUT}} = 100\text{pF}$
$t_{\text{O}}[4]$	I/O Output Lines Delay on Clear			1500	ns	$C_{\text{OUT}} = 100\text{pF}$

- Notes: 1. t_{H} measured with $V_{\text{OH}} = 15\text{V}$.
 2. t_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
 3. All MCS-40 components which may transmit instruction or data to 4001/4002 at ϕ_2 and ϕ_3 always enter a 1500 ns wait time after the 4001/4002 takes over the data bus at ϕ_1 and ϕ_2 times. Therefore the 150 ns requirement is always treated since each component cannot drive 100A of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/15A.
 4. CL on the 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.



Programming Instructions

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 330ASR teletype produces.

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of about punches.
2. Included in the tape before the leader, and enclosed by another leader, should be the customer's complete telex or fax number and if more than one pattern is being transmitted, the ROM pattern number.
3. The first ROM pattern, program field B, data device type number or ROM number. The field should be framed by an "I" and "I".

14001-

This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

"CHS"

The valid value digits for the 4001 are 0-15

"DOS" = "C155"

Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

"I01, I02, I03...I15"

where I01, I02...I15 are the option numbers associated with one I/O line. Hence, for a 4001 there will be four bracketed collections of I/O options. Each I/O pin has a series of 10 possible connections. These connections are consecutively numbered from 1-10. It is these numbers that should be in parentheses for each I/O pin.

Example:

"1" indicates no connection
 "1, 1, 1" indicates only #1
 "12, 5, 7" indicates connections #2, 5 and 7.

I/O options should be placed on the tape sequentially for the 4001 from I/O0-I/O316. Always avoid illegal combinations.

*NOTE: Cards may also be submitted.

B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily used on the teletype for diagnosis or error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.
4. Within the ROM pattern, words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit - "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

In the place of a standard BPNF word, a "B" or "F" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words (1 ≤ n ≤ 1023). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

intel®

MCS®
CUSTOM ROM
ORDER FORM

4001
ROM

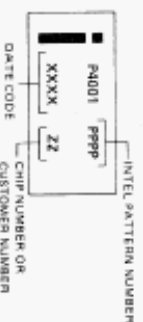
CUSTOMER _____	
P.O. NUMBER _____	DATE _____
For Intel use only	
S# _____	PPPP _____
STD _____	ZZ _____
DD _____	DD _____
APP _____	DATE _____

All custom 4001 ROM orders must be submitted on this form. Programming information should be sent in the form of computer punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel.

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4001), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).

CUSTOMER NUMBER _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____

(Must be specified—any number from 0 through 15—DD).

B. I/O OPTION - Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES - DESIRED OPTION CONNECTIONS REQUIRED

1. Non-inverting output - 1 and 3 are connected.
2. Inverting output - 1 and 4 are connected.
3. Non-inverting input (the inputs must be only 5 is connected).
4. Inverting input (inputs must be V_{SS} - 2, 6, 7, and 9 are connected).

5. Non-inverting input (input must be V_{DD} - 2, 7, 8, and 10 are connected).

6. If inputs and outputs are mixed on the same port, the pins used at the outputs must have the alternate values (8, 9, 10, 11, 12, 13, 14, 15) connected. This is necessary for the particular customer pattern, the chip number, and the date code. If the two pins are connected to the same output, the connection would be made as follows:

Inputs - 2 and 8 are connected Outputs - 1, 3, 8, and 9 are connected

If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

C. 4001 CUSTOM ROM PATTERN -

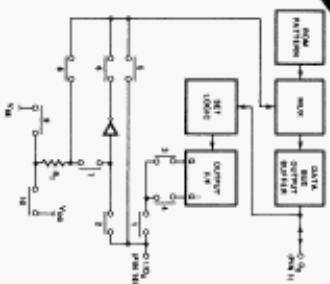
Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the character should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that:

NCP = BPNP PPPP = 0000 0000

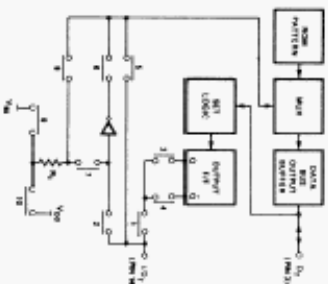
4001 I/O Options

SAMPLE

I/O₀ (PIN 16)

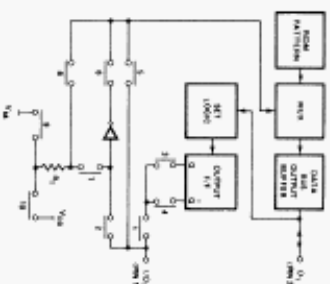
CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC) _____

- a. For T_{11} , computed a one-way ANOVA for factor and stages should be $F_{(10, 10)} = 1.04$, $p = 0.43$, $V_{\text{adj}} = 0.99$.

I/O₂ (PIN 14)

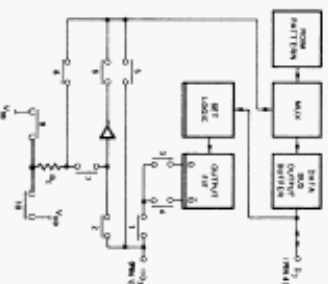
CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)

- a. For $T_{\text{L}} = 100^\circ\text{C}$, compare the results of the I.D. with the supply voltages given at the $V_{\text{DD}} = +10\text{V}$, $\beta_{\text{N}} = 100$, $\beta_{\text{P}} = 10$.

I/O₁ (PIN 15)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC) _____

4. For T_{eff} calculation on the Li^+ ion the band energies should be $V_{\text{COI}} = -12 \text{ eV}$, $V_{\text{OII}} = 4.5 \text{ eV}$.
 5. If electron-impact excitation is used, $T_{\text{eff}} = 4.5$ with maximum total TTA.

I/O₃ (PIN13)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)

- b. For $T_{1/2}$ averaged data in the 1:0 series the property values were 16 for $V_{00} = 1$ (20), 9% $V_{00} = 5.5$ (1.5).