APPENDIX C
MCS-4 CUSTOM ROM ORDER FORM

4001 Metal Masked ROM

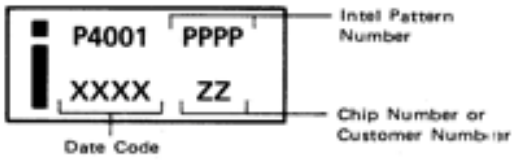
All custom ROM orders must be submitted on forms provided by Intel. Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a print-out of the truth table must accompany the order. Refer to Intel's Data Catalog for complete pattern specifications. Alternatively, the accompanying truth table may be used. Additional forms are available from Intel.

	For Intel use only	
CUSTOMER _____	S# _____	PPPP _____
P.O. NUMBER _____	STD _____	ZZ _____
	APP _____	DD _____
DATE _____	DATE _____	I/O _____

INTEL STANDARD MARKING

The marking as shown at right must contain the Intel logo, the product type (P4001), the four digit Intel pattern number (PPPP), a date code (XXXX), and the two digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ).

Optional Customer Number (Maximum 6 characters or spaces) _____



MASK OPTION SPECIFICATIONS

A. CHIP NUMBER _____ (Must be specified – any number from 0 through 15 – DD)

B. I/O OPTION – Specify the connection numbers for each I/O pin (next page). Examples of some of the possible I/O options are shown below:

EXAMPLES – DESIRED OPTION/CONNECTIONS REQUIRED

1. Non-inverting output – 1 and 3 are connected.
2. Inverting output – 1 and 4 are connected.
3. Non-inverting input (no input resistor) – only 5 is connected.
4. Inverting input (input resistor to V_{SS}) – 2, 6, 7, and 9 are connected.
5. Non-inverting input (input resistor to V_{DD}) – 2, 7, 8, and 10 are connected.
6. If inputs and outputs are mixed on the same port, the pins used as the outputs must have the internal resistor connected to either V_{DD} or V_{SS} (8 and 9 or 8 and 10 must be connected). This is necessary for testing purposes. For example, if there are two inverting inputs (with no input resistor) and 2 non-inverting outputs the connection would be made as follows:

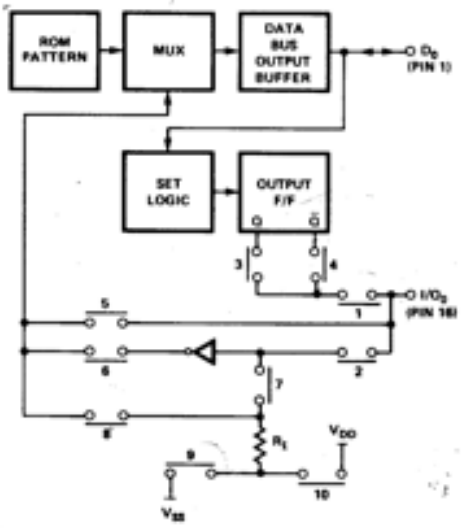
   Inputs – 2 and 6 are connected
   Outputs – 1, 3, 8 and 9 are connected or
   1, 3, 8 and 10 are connected

   If the pins on a port are all inputs or all outputs the internal resistors do not have to be connected.

C. 4001 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a print-out of the truth table must accompany the order. Refer to Intel's Data Catalog for complete pattern specifications. Alternatively, the accompanying truth table may be used. Based on this particular customer pattern, the characters should be written as a "P" for a high level output = n-logic "0" (negative logic "0") or an "N" for a low level output = n-logic "1" (negative logic "1").

Note that NOP = BPPPP PPPPF = 0000 0000

4001 I/O Options

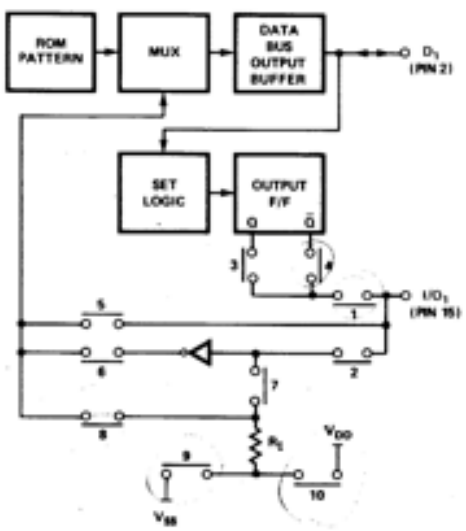


I/O_0 (PIN 16)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

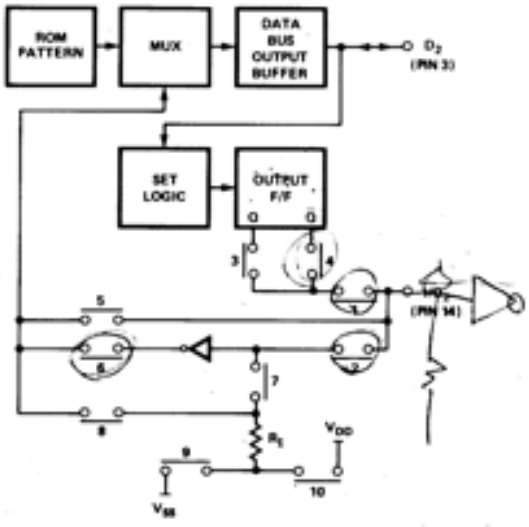


I/O_1 (PIN 15)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

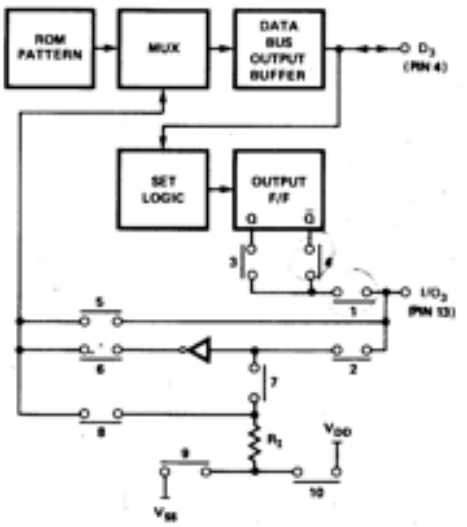


I/O_2 (PIN 14)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).



I/O_3 (PIN 13)

CONNECTIONS DESIRED (LIST NUMBERS & CIRCLE CONNECTIONS ON SCHEMATIC)_____

a. For T^2L compatibility on the I/O lines the supply voltages should be $V_{DD} = -10V \pm 5\%$, $V_{SS} = +5V \pm 5\%$

b. If non-inverting input option is used, $V_{IL} = -6.5$ Volts maximum (not TTL).

4001 CUSTOM ROM TRUTH TABLE

Customer _____

P.O. No. _____

Chip No. _____

Date _____

The customer truth pattern should be placed in the blue screen area. The white section above the screen area will be used by Intel to verify the customer pattern.

Based on the particular customer pattern, the characters should be written as a "P" for a high level output = n-logic "0" (negative logic "0") or an "N" for a low level output = n-logic "1" (negative logic "1").

Word Number	INSTRUCTION OPR $D_3D_2D_1D_0$	INSTRUCTION OPA $D_3D_2D_1D_0$	Word Number	INSTRUCTION OPR $D_3D_2D_1D_0$	INSTRUCTION OPA $D_3D_2D_1D_0$	Word Number	INSTRUCTION OPR $D_3D_2D_1D_0$	INSTRUCTION OPA $D_3D_2D_1D_0$	Word Number	INSTRUCTION OPR $D_3D_2D_1D_0$	INSTRUCTION OPA $D_3D_2D_1D_0$
0			32			64			96		
1			33			65			97		
2			34			66			98		
3			35			67			99		
4			36			68			100		
5			37			69			101		
6			38			70			102		
7			39			71			103		
8			40			72			104		
9			41			73			105		
10			42			74			106		
11			43			75			107		
12			44			76			108		
13			45			77			109		
14			46			78			110		
15			47			79			111		
16			48			80			112		
17			49			81			113		
18			50			82			114		
19			51			83			115		
20			52			84			116		
21			53			85			117		
22			54			86			118		
23			55			87			119		
24			56			88			120		
25			57			89			121		
26			58			90			122		
27			59			91			123		
28			60			92			124		
29			61			93			125		
30			62			94			126		
31			63			95			127		

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4001 CUSTOM ROM TRUTH TABLE

Customer _____

P.O. No. _____

Chip No. _____

Date _____

The customer truth pattern should be placed in the blue screen area. The white section above the screen area will be used by Intel to verify the customer pattern.

Based on the particular customer pattern, the characters should be written as a "P" for a high level output = n-logic "0" (negative logic "0") or an "N" for a low level output = n-logic "1" (negative logic "1").

Word Number	INSTRUCTION OPR	OPA	Word Number	INSTRUCTION OPR	OPA	Word Number	INSTRUCTION OPR	OPA	Word Number	INSTRUCTION OPR	OPA
	$D_3D_2D_1D_0$	$D_3D_2D_1D_0$		$D_3D_2D_1D_0$	$D_3D_2D_1D_0$		$D_3D_2D_1D_0$	$D_3D_2D_1D_0$		$D_3D_2D_1D_0$	$D_3D_2D_1D_0$
128			160			192			224		
129			161			193			225		
130			162			194			226		
131			163			195			227		
132			164			196			228		
133			165			197			229		
134			166			198			230		
135			167			199			231		
136			168			200			232		
137			169			201			233		
138			170			202			234		
139			171			203			235		
140			172			204			236		
141			173			205			237		
142			174			206			238		
143			175			207			239		
144			176			208			240		
145			177			209			241		
146			178			210			242		
147			179			211			243		
148			180			212			244		
149			181			213			245		
150			182			214			246		
151			183			215			247		
152			184			216			248		
153			185			217			249		
154			186			218			250		
155			187			219			251		
156			188			220			252		
157			189			221			253		
158			190			222			254		
159			191			223			255		

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