- Microprogrammable General Purpose Computer Set
- 4-Bit Parallel CPU With 45 Instructions
- Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching
- Binary and Decimal Arithmetic Modes
- Addition of Two 8-Digit Numbers in 850 Microseconds
- 2-Phase Dynamic Operation
- 10.8 Microsecond Instruction Cycle
- CPU Directly Compatible With MCS-4 ROMs and RAMs
- Easy Expansion–One CPU can Directly Drive up to 32,768 Bits of ROM and up to 512D Bits of RAM
- Unlimited Number of Output Lines
- Packaged in 16-Pin Dual In-Line Configuration

The MCS-4 is a microprogrammable computer set designed for applications such as test systems, peripherals, terminals, billing machines, industrial systems, numerical and process control. The 4004 CPU, 4003 SR, and 4002 RAM are standard building blocks. The 4001 ROM contains the resident microprogram and is implemented using a metal mask according to customer specifications.

MCS-4 systems interface easily with switches, keyboards, displays, teletypewriters, printers, readers, A-D converters and other popular peripherals.

A system built with the MCS-4 micro computer set can have up to 4K x 8 bit ROM words, 1280 x 4 bit RAM characters and 128 I/O lines without requiring any interface logic. By adding a few simple parts the MCS-4 can have up to 4K RAM and ROM packages in any combination, and 192 I/O lines. The minimum system configuration consists of one CPU and one 256 x 8 bit ROM.

The MCS-4 has a very powerful instruction set that allows both binary and decimal arithmetic. It includes conditional branching, jump to subroutine, and provides for the efficient use of ROM locks up tables by indirect fetch.

The Intel MCS-4 micro computer set (4001/2/3/4) is fabricated with Silicon Gate Technology. This low threshold, ion implanted process is the same production of higher performance MOS circuits and provides a higher functional density on a monolithic chip than conventional MOS technologies.

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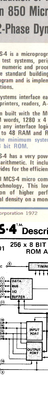
MCS-4™ Description

4001 256 x 8 BIT MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT



The 4001 is a 2048-bit metal mask programmable ROM providing custom microprogramming capability for the MCS-4 micro computer set. It is organized as 256 x 8 bit words.

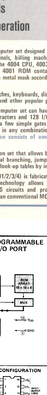
Address and data are transferred in and out by time multiplexing on 4 data bus lines. Timing is internally generated using two clock signals, ϕ_1 and ϕ_2, and a SYNC signal supplied by the 4004. Addresses are received from the CPU on three time periods following SYNC, and select 1 out of 256 words and 1 out of 16 ROM's. For that purpose, ROM's are identified as 40, 1, 2, through 15, by metal option. A Command Line (CM) is also provided and its scope is to select a ROM bank (group of 16 ROM's).

During the two time periods (M_1 & M_2) following the addressing time, information is transferred from the ROM to the data bus lines.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O interface lines. Each chip is the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction. An external signal (CL) will asynchronously clear the output register during normal operation. All internal flip flops (including the output register) will be reset when the RESET line goes low (negative voltage).

Each I/O pin can be uniquely chosen as either an input or output port by metal option. Direct or inverted input or output is optional. An on-chip resistor at the input pins, connected to the voltage V_{DD}, is also optional. (See ordering information on page 12).

4002 320 BIT RAM AND 4 BIT OUTPUT PORT



The 4002 performs two functions. It is a RAM of 80 words x 320 bits arranged in 4 registers of 20 characters each (16 words of main memory characters and 4 status characters). As a variable set of communication with peripheral devices, it is provided with 4 output lines and associated control logic to perform output operations.

In the RAM mode, the operation is as follows: When the CPU executes an SRC instruction (see Instruction Set on page 5) it will send out the contents of the designated index register pair (registers X_2 and X_3) as an address to the RAM, and will activate one CM-RAM line at X_2 for the previously (Note 1) selected RAM bank (see Rom Instruction Cycle on page 5).

The data at X_2 and X_3 is interpreted as shown below:

X_2	X_3
D_2 D_3 D_0 D_1	D_2 D_3 D_0 D_1
Chip ID (through 2)	Register (through 3)	Main Memory Character ID (through 15)

The status character locations (0 through 3) are selected by the CPU operation of one of the four RAM status characters. For chip selection, the 4002 is available in two metal options, 4002 1 and 4002 2. An externally applied chip select may be hard wired to either V_{SS} or V_{DD} it also available for chip selection. All chip selection is asynchronous.

Chip ID	4002 Option	P_0	D_2	D_3	ID X_2
0	4002-1	V_{DD}	0	0	0
1	4002-1	V_{DD}	0	0	1
2	4002-1	GND	1	0	0
3	4002-2	V_{DD}	1	0	1

Timing is internally generated by two clock signals, ϕ_1 and ϕ_2, and a sync signal provided by the 4004. Internal refresh circuitry maintains data levels in the RAM.

All communications with the outside world is through the data bus. The I/O port permits data out from the system. When the external RESET signal goes low, the memory and all static flip-flops (including the output register) will be cleared. To fully clear the output register the RESET signal must be maintained for at least 32 memory cycles (32 x 8 clock periods).

MCS-4™ Description

4003 10 BIT SERIAL-IN/PARALLEL-OUT, SERIAL-OUT SHIFT REGISTER (SR)

The 4003 is a 10 bit static shift register with serial-in, parallel-out and serial out data. Its function is to increase the number of output lines to interface with I/O devices such as keyboards, displays, printer, teletypewriters, switches, readers, A-D converters, etc.

Data is loaded serially and is available in parallel on 10 output lines which are accessed through enable logic. When enabled (E = low), the shift register contents is read out; when not enabled (E = high), the parallel-out lines are at V_{DD}. The serial out line is not affected by the enable logic.

Data is also available serially permitting an indefinite number of similar devices to be cascaded together to provide shift register length multiples of 10.

The data shifting is controlled by the CP signal. An internal power-on-clear circuit will clear the shift register (D_1 = V_{DD}) between the application of the supply voltage and the first CP signal.

4004 4 BIT CENTRAL PROCESSOR UNIT (CPU) WITH 45 INSTRUCTIONS

The 4004 is a central processor unit (CPU) designed to work in combination with other members of the MCS-4 (4001, 4002, 4003) micro-programmable computer applications.

A typical machine cycle starts with the CPU sending a sync-chronization signal (SYNC) to the ROM's and RAM's. Next, 12 bits of ROM address are sent to the data bus using three clock cycles (8: 76 MHz). The address is then incremented by one and stored in the program counter. The selected ROM sends back 8 bits of instruction or data during the following 2 clock cycles. This information is stored in two registers: OPR and OPA. The next three clock cycles are used to execute the instruction. (See Rom Instruction Cycle on page 5).

The ROM bank is controlled by a command ROM control signal (CM-ROM) and up to four RAM banks are controlled by four command RAM control signals (CM-RAM$_0$, CM-RAM$_1$, CM-RAM$_2$, CM-RAM$_3$). Bank switching is accomplished by the execution of the DCL instruction (see Note 1 on page).

An input test signal (TEST) is used in conjunction with the jump on condition (JCN) instruction. When the TEST input signal is used to clear all registers and flip-flops. To fully clear all registers, the RESET signal must be applied for at least 8 instruction cycles (8 x 8 clock periods). After RESET the program will start from "0" step and CM-RAM$_0$ will be selected. The interconnection of the 4004 consists of:

(a) 16 machine instructions (5 of which are double length).
(b) 14 accumulator group instructions.
(c) 16 input/output & RAM instructions.

MCS-4™ Operation

The detailed functional specifications describing the operation of the system, the instruction set, the activity of the CPU for each instruction and some programming and hardware design hints are published separately and are available upon request. Following is a brief outline of the system operation.

The MCS-4 uses a 10.8 μsec instruction cycle. The CPU (4004) generates a synchronizing signal (SYNC), indicating the start of an instruction cycle, and sends it to the ROM's (4001) and RAM's (4002).

Basic instruction execution requires 8 or 16 cycles of a 750 KHz clock. In a typical sequence, the CPU sends 12 bits of address to the ROM's in the first three cycles (A_1, A_2, A_3). The selected ROM chip sends back 8 bits of instruction in the next two cycles (M_1, M_2). The instruction is then interpreted and executed in the final three cycles (X_1, X_2, X_3). (See Figure 2.)

The CPU, RAM's and ROM's can be controlled by an external RESET line. While RESET is activated the contents of the registers and flip-flops are cleared. After RESET, the CPU will start from address 0 and CM-RAM$_0$ is selected.

The MCS-4 can have up to 4K x 8 bit ROM words, 1280 x 4 bit RAM characters and 128 I/O lines, without requiring any interface logic. By adding a few simple parts, the MCS-4 can have up to 4B RAM and ROM packages in any combination and 192 I/O lines.

The 4001, 4002, and 4004 are interconnected by a 4-line data bus (D_0, D_1, D_2, D_3), used for all information flow between the chips except for control signals sent by the CPU on 5 additional lines. The interconnection of the MCS-4 system is shown in Figure 1. An expanded configuration is shown.

4001: Figure 2 shows the activity on the data bus during each clock period, and how a basic instruction cycle is subdivided.

Each data bus output buffer has three possible states "1", "0", and floating. At any given time only one output buffer is allowed to drive a data line, therefore, all the other buffers must be in a floating condition. However, more than one input buffer per data line can receive data at the same time.

The MCS-4 has a very powerful Instruction Set that allows both binary and decimal arithmetic. It includes conditional branching, jump to subroutine and provides for the efficient use of ROM look up tables by indirect fetching. Typically, two 8-digit numbers can be added in 850 μsec. The complete Instruction Set is shown on pages 5 and 6.

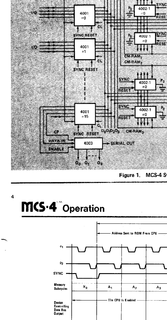
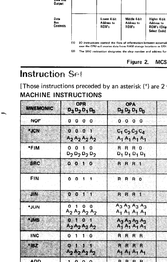


Figure 1. MCS-4 System Interconnection

MCS-4™ Operation


INSTRUCTION CYCLE
Address Sent to ROM Pins CP1
Instruction Received in OPR and Decoded
Data Sent to Accumulator or Other Destination
SYNC
D0-D3
CP1
CP2
ROM Pins
OPR
OPA
Data Bus
Accumulator
Carry
Instruction Decoder
Instruction Register
Data Bus Buffers
Address Register
Stack Register
Data Bus Buffers
Data Bus Buffers
Data Bus Buffers

DAD	1 0 0 1	9	1 0 0 1		Deposit accumulator.
TCS	1 1 0 0	C	1 0 0 0		Transfer carry subtract and clear carry.
STC	1 1 0 1	D	1 0 1 0		Set carry.
DAA	1 1 1 0	E	1 0 1 1		Decimal adjust accumulator.
KBP	1 1 1 1	F	1 1 0 0		Keyboard process the contents of the accumulator from a one out of four code to a binary code.
DCL	1 1 1 1	F	1 1 0 1		Designate command line. (See note 1 on page 3.)

NOTES: (1) This condition code is assigned as follows:
C_4 = 1 Insert jump condition
C_4 = 0 Non insert jump condition
C_3 = 1 Jump if accumulator is zero
C_3 = 0 Jump if accumulator is ≠ 0
C_2 = 1 Jump if carry/link is a 1
C_2 = 0 Jump if carry/link is a 0

(2) RAM is the address of 1 of 8 index register pairs in the CPU.

(3) RAMR is the address of 1 of 16 index registers.

(4) Each RAM chip has 4 registers, each with twenty 4 bit characters subdivided into 16 main memory characters and 4 status characters. Chip number, RAM register and main memory character are addressed by an SRC instruction. For the selected chip and register, however, status character locations are selected by the instruction code (DSA).

6

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +90°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{SS}	+0.5 to −20V
Power Dissipation	1.0 W

*COMMENT
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

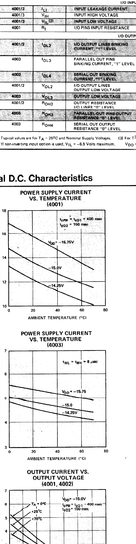
D.C. and Operating Characteristics

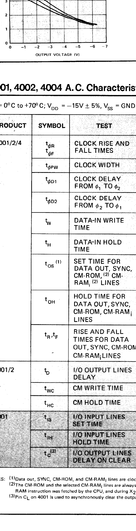
T_A = 0°C to +70°C; V_{DD} = −15V ±5%, V_{SS} = GND; I_{DCY} = 640 nsec; I_{DCY} = 750 nsec, unless otherwise specified
Logic "0" is defined as the more positive voltage (V_{IL}, V_{OL}). Logic "1" is defined as the more negative voltage (V_{IH}, V_{OH})

			LIMIT				
PRODUCT	SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	TEST CONDITION
SUPPLY CURRENT							
4001	I_{DD1}	AVERAGE SUPPLY CURRENT		15	30	mA	T_A = 25°C
4002	I_{DD2}	AVERAGE SUPPLY CURRENT		3.5	7.0	mA	T_A = 25°C
4003	I_{DD3}	AVERAGE SUPPLY CURRENT		5.5	8.5	mA	T_A = 25°C, I_{DCY} = 2 μsec
4004	I_{DD4}	AVERAGE SUPPLY CURRENT		20	40	mA	T_A = 25°C
INPUT CHARACTERISTICS (ALL INPUTS EXCEPT I/O INPUT PINS)							
4001/04	I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = V_{SS}
4001/04	V_{IH}	INPUT HIGH VOLTAGE (SERIAL INPUT PIN)	V_{SS}−1.5		V_{SS}+0.3	V	
4001/04	V_{IL}	INPUT LOW VOLTAGE (SERIAL INPUT PIN)	V_{DD}		V_{SS}+0.5	V	
4001/04	V_{IH}	CLOCK INPUT HIGH VOLTAGE	V_{SS}−2.5		V_{SS}+0.3	V	
4001/04	V_{IL}	CLOCK INPUT HIGH VOLTAGE	V_{DD}		V_{SS}+0.5	V	
OUTPUT CHARACTERISTICS (ALL OUTPUTS EXCEPT I/O OUTPUT PIN)							
4001/04	I_{LO}	DATA BUS OUTPUT LEAKAGE CURRENT			10	μA	V_{OUT} = +15V, Unselected Data Bus
4001/04	V_{OH}	OUTPUT HIGH VOLTAGE	V_{SS}−0.5		V_{SS}	V	Driving 4000 Series loads only
4001/04	I_{OH1}	DATA BUS OUTPUT CURRENT "1" LEVEL	−5	−8		mA	V_{OUT} = +2.5V
4001/04	I_{OH2}	CM-ROM DRIVING CURRENT "1" LEVEL	0.5	1		mA	V_{OUT} = 0V
4004	I_{OL4}	CM-RAM LINES SINKING CURRENT "0" LEVEL	2.5	4		mA	V_{OUT} = +5V
4001/04	V_{OL1}	DATA LINES, CM LINES OUTPUT LOW VOLTAGE	V_{SS}	V_{SS}	V_{SS}+0.5	V	I_{OUT} = 500 μA
4001/04	R_{DS1}	OUTPUT SINK CHANNEL DATA LINES "0" LEVEL		150	250	Ω	V_{OUT} = +0.5V
4004	R_{DS4}	CM-ROM OUTPUT RESISTANCE "0" LEVEL		200	400	Ω	V_{OUT} = +0.5V
4004	R_{DS4}	CM-RAM OUTPUT RESISTANCE "0" LEVEL		1.1	1.8	kΩ	V_{OUT} = +5V
I/O INPUT CHARACTERISTICS							
4001/2	I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = V_{SS}
4001/2	V_{IH}	INPUT HIGH VOLTAGE	V_{SS}−1.5		V_{SS}+0.3	V	
4001/2	V_{IL} [2]	INPUT LOW VOLTAGE	V_{DD}		V_{SS}−6.5	V	V_{OUT} = −5V
4001	R_I	I/O PINS INPUT RESISTANCE	10	15	25	kΩ	Internal input resistor is optional
I/O OUTPUT CHARACTERISTICS							
4001	I_{OL1}	I/O OUTPUT LINE SINKING CURRENT "0" LEVEL	2.5	5		mA	V_{OUT} = +0.5V (for TTL compatibility a 5.2K ±1.10% resistor necessary on I/O output pin)
4002	I_{OL1}	PARALLEL OUT PINS SINKING CURRENT "0" LEVEL	0.8	1.2		mA	V_{OUT} = +0.5V (for TTL compatibility a 5.2K ±1.10% resistor necessary on I/O output pin)
4002	I_{OL4}	SERIAL OUT SINKING CURRENT "0" LEVEL	3.0	5.0		mA	V_{OUT} = +5V
4001/2	V_{OL1}	I/O OUTPUT LINES OUTPUT LOW VOLTAGE	V_{SS}	V_{SS}	V_{SS}+0.5	V	I_{OUT} = 500μA
4002	V_{OL4}	SERIAL OUT OUTPUT LOW VOLTAGE	V_{SS}	V_{SS}	V_{SS}+0.5	V	I_{OUT} = 500μA
4001/2	R_{DS1}	OUTPUT RESISTANCE "0" LEVEL		150	250	Ω	V_{OUT} = +0.5V
4002	R_{DS4}	PARALLEL OUT PINS OUTPUT RESISTANCE "0" LEVEL		400	750	Ω	V_{OUT} = +0.5V
4002	R_{DS4}	SERIAL OUT OUTPUT RESISTANCE "0" LEVEL		880	1300	Ω	V_{OUT} = +5V

(1) Typical values are for T_A = 25°C and Nominal Supply Voltages. (2) For TTL compatibility on the I/O lines the supply voltages should be
(3) If non-inverting input option is used, V_{IL} = −6.5 Volts maximum. V_{DD} = −19V ± 5%. V_{SS} = +5V ± 5%

Typical D.C. Characteristics





8

4001, 4002, 4004 A. C. Characteristics

T_A = 0°C to +70°C; V_{DD} = −15V ± 5%, V_{SS} = GND

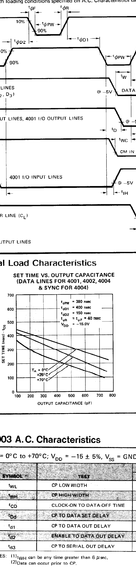
PRODUCT	SYMBOL	TEST	LIMIT MIN.	LIMIT MAX.	UNIT	CONDITIONS
4001/2/4	t_{SR} t_{SF}	CLOCK RISE AND FALL TIMES	10	50	nsec	
	t_{SPW}	CLOCK WIDTH	380	480	nsec	
	t_{SD1}	DELAY CLOCK FROM ϕ_1 TO ϕ_2	400	550	nsec	
	t_{SD2}	DELAY CLOCK FROM ϕ_2 TO ϕ_1	150	300	nsec	
	t_{W}	DATA-IN WRITE TIME	350		nsec	
	t_{H}	DATA-IN HOLD TIME	40		nsec	
	t_{DS} (1)	SET TIME FOR DATA OUT, SYNC, CM-ROM, (2) CM-RAM, (3) LINES	0		nsec	C_{OUT} = 500 pF for data lines 500 pF for SYNC 150 pF for CM-ROM 50 pF for CM-RAM
	t_{DH}	HOLD TIME FOR DATA OUT, SYNC, CM-ROM, CM-RAM, LINES	50		nsec	C_{OUT} = 20 pF
	t_R, t_F	RISE AND FALL TIMES FOR DATA OUT, SYNC, CM-ROM, CM-RAM, LINES		500	nsec	C_{OUT} = 500 pF for data lines 500 pF for SYNC 150 pF for CM-ROM 50 pF for CM-RAM
4001/2	t_D	I/O OUTPUT LINES DELAY		600	nsec	C_{OUT} = 20 pF
	t_{WC}	CM WRITE TIME	350		nsec	
	t_{HC}	CM HOLD TIME	10		nsec	
4001	t_{S}	I/O INPUT LINES SET TIME	50		nsec	
	t_{HI}	I/O INPUT LINES HOLD TIME	100		nsec	
	t_{DI} (2)	I/O INPUT LINES DELAY ON CLEAR		200	nsec	C_{OUT} = 20 pF

NOTES: (1) Data out, SYNC, CM-ROM, and CM-RAM lines are clocked out with the trailing edge of the ϕ_2 clock.
(2) The CM-ROM and the selected CM-RAM lines are always activated during ϕ_2 time. They are also activated during M_2 time if an I/O and RAM instruction was fetched by the CPU, and during X_2 time if an SRC instruction was fetched by the CPU.
(3) The C_{L2} on 4001 is used to asynchronously clear the output flip-flops associated with the I/O lines.

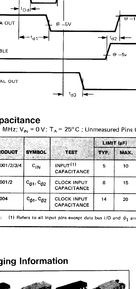
9

4001, 4002, 4004 Timing Diagram

Outputs with loading conditions specified on A.C. Characteristics table.



Typical Load Characteristics



10

4003 A.C. Characteristics

T_A = 0°C to +70°C; V_{DD} = −15 ± 5%, V_{SS} = GND

		LIMIT			
SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
t_{PCL}	CP LOW WIDTH	6		10,000	μsec	
t_{PCH}	CP HIGH WIDTH	6		Note 1[1]	μsec	
t_{CD}	CLOCK ON TO DATA OUT TIME	3		7	μsec	
t_{CS}	CP TO DATA SET DELAY	Note 1[2]		250	nsec	
t_{DS}	CP TO DATA OUT DELAY	250		1,750	nsec	
t_{CL}	ENABLE TO DATA OUT DELAY			350	nsec	C_{OUT} = 20 pF
t_{CP}	CP TO SERIAL OUT DELAY	200		1,250	nsec	C_{OUT} = 20 pF

NOTES: (1) Max can be any time greater than 6 μsec.
(2) Max can occur prior to CP.

4003 Timing Diagram

Capacitance

f = 1 MHz; V_{IN} = 0V; T_A = 25°C ; Unmeasured Pins Grounded.

PRODUCT	SYMBOL	TEST	LIMIT (pF) TYP.	LIMIT (pF) MAX.
4001/2/3/4	C_{IN}	INPUT[1] CAPACITANCE	5	10
4001/2	C_{B1}, C_{B2}	CLOCK INPUT CAPACITANCE	8	15
4004	C_{B1}, C_{B2}	CLOCK INPUT CAPACITANCE	14	20

NOTE: (1) Refers to all input pins except data bus I/O and ϕ_1 and ϕ_2.

11

Packaging Information

Ordering Information

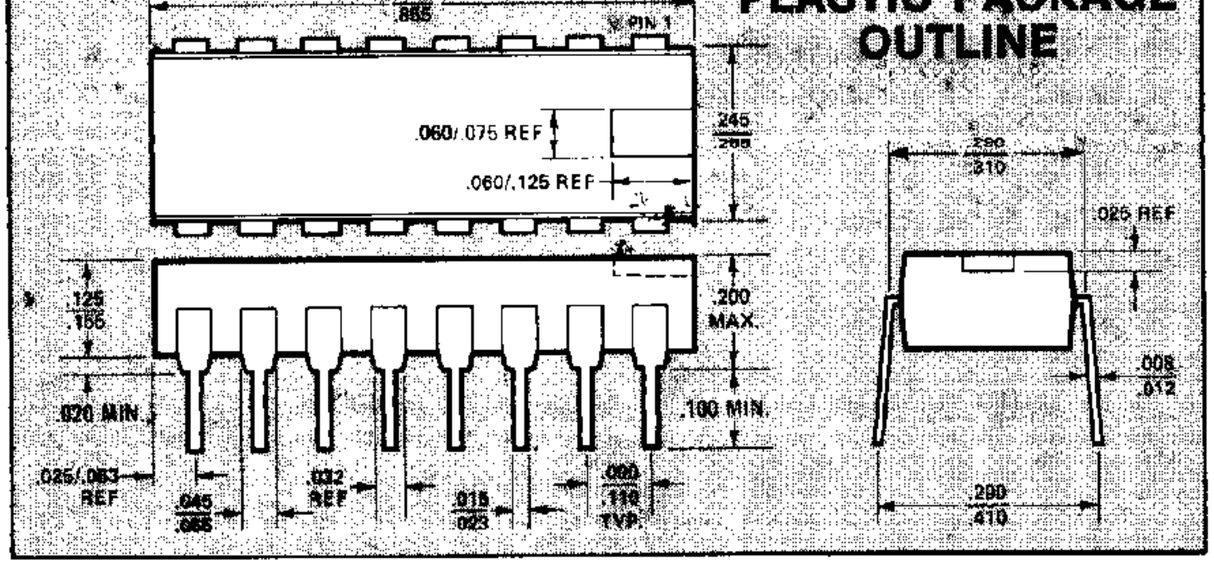
(1) The 4004 (CPU) is available in ceramic only and should be ordered as (CR04).

(2) The 4001 (ROM), 4002 (RAM) and 4003 (SR) are presently available off the shelf in plastic only. These devices can be ordered in ceramic on special request. Standard devices should be ordered as follows:
4001 Plastic Package
P4001 Mask Version #11 - Plastic Package
P4002C1 (Mask Option #2) - Plastic Package
P4003 Plastic Package

(3) **Mask Programmable Options**
The customer can specify the pull-down and I/O options (input/output sensing and non-inverting inputs or outputs and on-chip resistor connected to either V_{DD} or V_{SS}) must be specified at an a truth table for each 4001 ordered. Blank custom truth tables are available on request.

(4) MCS-4 Software: Xin Using the **4001-0005 ROM**
Xin is a cross assembler capable of evaluating one MCS-4 parts, Using the microprogram stored in the 4001-0005, all of the 46 instructions of the MCS-4 instruction set are executed. Xin runs on the IBM 360/67 under the Time Sharing Option (TSO). To order, specify the indicated part numbers.

(5) **SIM-01: Prototyping System**
An interface board in which 1701 or 1702 electrically pro-



grammable and erasable ROM's simulate the 4001 mask programmable ROM's provides a design tool for developing a system. This board contains one 4004, four 4002's and has provision for up to four 1701's or 1702's. The board should be ordered as SIM4-01 (the type and number of PROM's should also be indicated).

(6) **SIM4-02: Prototyping System**
This board is an expanded version of the SIM4-01. It contains one 4004, four 4002's, and has provision for an additional twelve 4002's and sixteen 1701's or 1702's. The board should be ordered as SIM4-02 (the type and number of PROM's and RAM's should also be indicated).

(7) **MP7-02 ROM Programmer**
This is the programmer board for 1601/1701 or 1602/1702. The three 1602 control ROM's used with the SIM4 cards for an automatic programming system are specified by pattern numbers A0540, A0541, A0542. All items should be ordered individually.

(8) **PROM Program A0700: Sample Decimal Addition Program**
The SIM4-01 or SIM4-02 systems (interfaced with TTY) can be checked out using this special program in a 1701 or 1702. When ordering PROM's, specify one of the devices programmed to Intel tape number A0700.

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