# 256 x 8 MASK PROGRAMMABLE ROM AND 4 BIT I/O PORT

- Direct Interface to MCS-40" I/O Port Low-Power TTL
- 16 Pin Dual In-Line Package Compatible
- Standard Operating 0° to 70°C Temperature Range of

27

š ¢1, ¢2/Neg

 Also Available With -40° to +85°C Operating Range

> RESET/Neg SYNC/Neg

Reset input. A negative level System synchronization signal

(V<sub>DD</sub>) on this pin will clear ingenerated by processor. which determine device timing Non-overlapped clock signals

The input buffers are not ternal flip-flops and buffers.

communication with peripheral devices it is provided with 4 I/O pins and associated control logic to perform input and output operations. The 4001 is a PMOS device, compatible with all other MCS-40" devices. The 4001 performs two basic and distinct functions. As a ROM it stores 256 x 8 words of program or data tables; as a vehicle of

7

CL/Neg.

Clear input for I/O lines. A negcleared by this signal.

CTHE MALE CTHE MALE CHARGE r E ::::: ALTA DALTA DACADA NON NON

PIN CONFIGURATION

BLOCK DIAGRAM

5 Ė

ě

CM-ROM/Neg.

Chip enable generated by the a TK pull-up to V<sub>SS</sub>. be driven by a TTL output and ative level on this pin will clear the I/O buffers. This pin may

processor.

13-16

I/Og-I/Og/Neg. A single I/O port consisting of

be V<sub>88</sub> - 15,0V ±5%,

Main supply voltage value. Must

4 bidirectional and solectable

Functional Description

words and 1 out of 16 ROM's. For that purpose, each ROM is identified as #0, 1, 2, through 15, by metal option. A Command ROM Line (CM-ROM) is also provided and it is used to select a ROM bank (group of 16 ROM's). three time periods following SYNC, and select 1 out of 256 plied by the CPU, Addresses are received from the CPU on using two clock signals,  $\phi_1$  and  $\phi_2$ , and a SYNC signal supplexing on 4 data bus lines. Timing is internally generated Address and data are transferred in and out by time multi

& Mpl following the addressing time, information is transferred from the ROM to the data bus lines. During the two time periods of the instruction cycle (M<sub>1</sub>

chronously clear the output register during normal operation.

All internal flip flops (including the output register) will Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O. execute the instruction. An external signal ICL1 will asymfor an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and external lines. Each chip has the capability to identify itself A second mode of operation of the ROM is as an Input/

be reset when the RESET line goes law (Vpo).

Description of Function dress and data communication Bidirectional data bus, All ad-Most positive supply voltage ROM is handled by these lines. between the processor and connected to either V<sub>DD</sub> or V<sub>SS</sub>. pin is chosen as an input it may have an on-chip resistor either an input or output line by metal option. Also each input or output can either be inverted or direct. When the I/O Options Each I/O pin on each ROM can be uniquely chosen to be

Pin No.

Designation/ Type of Logic

Do .D<sub>3</sub>/Neg.

Pin Description

## Instruction Execution

The 4001 responds to the following instructions

# SRC Instruction | Send address to ROM and RAM)

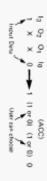
later perform an I/O operation. Data at X3 is ignored. (representing the contents of the first register of the out 8 bits of data during  $X_2$  and  $X_3$  and will activate the CM-ROM and one CM-RAM line at  $X_2$ . Data at  $X_2$ When the CPU executes an SRC instruction it will the 4001 as the chip number of the unit that should register pair addressed by the SRC instruction) with simultaneous presence of CM-ROM, is interpreted by

### WRR - Write ROM Port

WRR is executed on the same drip. The ADC content and carry/link are unaffected. (The LSB bit of the accumulator appears on I/O<sub>B</sub>.) No operation is performed on IJfQ lines coded as inputs. The data is available on the output pins until a new ROM output port of the previously selected ROM chip. The content of the accumulator is transferred to the

## RDR - Read ROM Port

or "1" transferred to the accumulator for those I/O pins If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "O" coded as outputs, when an RDR instruction is executed selected ROM chip is transferred to the accumulator. For example, given a port with the I/O lines coded The data present at the input lines of the previously



the transfer is as shown below:

with 2 inputs and 2 outputs, when RDR is executed,

## Timing Consideration

to send data out during the following two cycles:  $M_1$  and  $M_2$ . The activity of the 4001 in the ROM mode ends at  $M_2$ . code matches the chip number code sent during A3 is allowed bit address during A1 and A2 times of the instruction cycle When CM-ROM is present, only the dhip whose metal option and a chip number, together with CM-ROM, during Ag time. In the ROW mode of operation the 4001 will receive an 8

from 0 - 15. The 4001 can have a chip number via the metal option

latched on the output flip-flops associated with the I/O lines. was WRR, the data present on the data bus at X2.92 will be its I/O pins to the data bus at X2. If the instruction received after receiving RDR will transfer the information present at In the I/O mode of operation, the selected 4001 (by SRC)

### Ordering Information

specified: When ordering a 4001, the following information must be

- Chip number
- All the metal options for each I/O pin.
- 3. ROM pattern to be stored in each of the 256

from lintel. A copy of this table is shown and blank copy can be found following the detailed 4001 characteristics. A blank customer truth table is available upon request

EXAMPLES - DESIRED OPTION/CONNECTIONS RE-

- Non-inverting output (negative logic output) 1 and 3 are connected.
- Non-inverting input (no input resistor negative logic 2 Inverting output (positive logic output) — 1 and 4 are input) - only 5 is connected. connected,
- 4. Inverting input (input resistor to V<sub>55</sub> positive logic input) - 2, 6, 7, and 9 are connected.
- Non-inverting input linput resistor to V<sub>00</sub> negative If inputs and outputs are mixed on the same port, the logic input) - 2, 7, 8, and 10 are connected.
- must be connected!. This is necessary for testing pur-poses. For example, if there are two inverting inputs (with no input rejustor) and 2 non-inverting outputs the connected to either VDD or VSS (8 and 9 or 8 and 10 pins used as the outputs must have the internal resistor

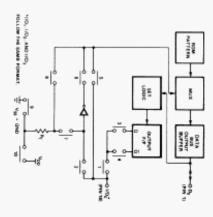
connection would be made as follows: Inputs - 2 and 6 are connected

1, 3, 8 and 10 are connected Outputs - 1, 3, 8 and 9 are connected or

If the pins on a port are all inputs or all outputs, the internal resistors do not have to be connected.

options should be selected. it should be noted that all internal logic and processing is performed in negative logic, i.e., "I" equals Vop and "D" equals VSS. For positive logic conversion, the inverted

all outputs to insure the logic "0" state (VQL). VSS = 5V ± 5%. An external 12K resistor should be used on TTL competibility is obtained by Vpp = -10V ±5% and



# 4001 Available Metal Option for Each I/O Pin.

# Absolute Maximum Ratings\*

"COMMENT.

"COMMENT".

"COMMENT TO Extend under "Abstock Maureure Refregat".

They cause permission identify motiva disease. This is a limited using order to the disease along order to the process of the disease at make or stary offer conductors about a fixed with calculation of the disease at make or stary offer conductors about a fixed with calculation in the disease at make or stary of the appendication is not express.

8

# D.C. and Operating Characteristics

 $T_A = 0^{\circ}C$  to  $70^{\circ}C$ ;  $V_{SS} = V_{DO} = 15V \pm 5\%$ ;  $I_{SPM} = I_{ADD} = 400$  nacc;  $I_{SDD} = 150$  nacc; Logic "0" is defined as the more positive voltage  $\{V_{H_1}, V_{O_1}\}$ ; Unless Otherwise Specified.

### SUPPLY CURRENT

			Limit			
Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
001	Average Supply Current		16	30	πA	T <sub>A</sub> = 25°C
INPUT CH	INPUT CHARACTERISTICS - ALL INPUTS EXCEPT I/O PINS					
Ē.	Input Laskage Current			10	Αŭ	VIL = Vpp
V <sub>IH</sub>	Input High Voltage (Except Clocks)	V <sub>\$5</sub> -1.5		V55+.3	<	
V <sub>II</sub> L	Input Low Voltage (Except Clocks)	Vop		$V_{88}-5.5$	<	
VIHC	Input High Voltage Glocks	V <sub>58</sub> -1.5		V <sub>SS</sub> +.3	<	
VILC.	Input Low Voltage Clocks	You		V <sub>55</sub> -13.4 V	٧	
OUTPUT	OUTPUT CHARACTERISTICS - ALL OUTPUTS EXCEPT I/O PINS	SNIc				

	R <sub>1</sub> [1]	3	D	٧I٢	ř	Ϋ́L	V <sub>IH</sub>	<u>-</u>	I/O IMPO	Вон	V <sub>O</sub> L	lor.	МОН	δ
	Input Resistance, if Used	and the second s	loos Pasistanes if I had	CL Input Law Voltage	Input Low Voltage, Non-inverting Input	Input Low Voltage, Inverting Input	Input High Voltage	Input Leakage Current	I/O INPUT CHARACTERISTICS	Output Resistance, Data Line "O" Level	Output Low Voltage, Date Bus, CM, SYNC	Data Lines Sinking Current	Output High Voltage	Data Bus Output Leakage Current
	5	č	5	Vpo	VDO	Ypo	V <sub>88</sub> -1.5				Vss-12	89	V855V	
	26	ä	ė							150		3	V <sub>SS</sub>	
	6	1	Ř	V <sub>85</sub> -4.2	V <sub>88</sub> -6.5	Vss-4.2	V85+.3	10		250	V <sub>35</sub> -6.5			5
	ă	200	Š	<	<	<	<	μA		::	<	mΑ	<	ž
V <sub>IN</sub> = V <sub>SS</sub> -3V	R1 tied to Vpp;	V <sub>IN</sub> = V <sub>88</sub> -3V	B that to V							V <sub>OUT</sub> = V <sub>SS</sub> −.5V	I <sub>OL</sub> = 0.5mA	V <sub>0</sub> UT = V <sub>88</sub>	Capacitive Load	Vout = -12V

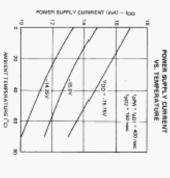
c	5
:	ŝ
٥.	15
ì	왚
Į.	RACT
	SINE
5	TICS
ı	
- 1	

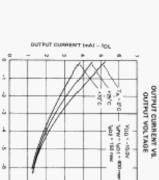
PF VIN = VSS	10				
	;			Input Capecitance	ClN
	15	9.5		Data Bus Capacitance	g <sub>0</sub>
pF VIN = V88	15	00		Clock Capacitance	ç,
				TANCE	CAPACIT
<	¥55-6.5		V <sub>55</sub> -12	I/O Output Low Voltage	V <sub>OL</sub> 1/0 0
mA V <sub>OUT</sub> = V <sub>55</sub> -4.85V		ω	0.8	I/O Output "1" Sink Current	loL(2)
mA V <sub>OUT</sub> = V <sub>SS</sub> 5V		en	2.5	I/O Output "1" Sink Current	lor
kΩ V <sub>OUT</sub> = V <sub>S8</sub> 5V	2	1.2		I/O Output "O" Resistance	ROH
V 10UT = 0			V855V	Output High Voltage	МОМ

Note: 1. R<sub>1</sub> is large signal equivalent resistance to IV<sub>SS</sub>-12f V. 2. For TTL compatibility, use 12kD externel resistor to V<sub>DD</sub>.

# Typical D.C. Characteristics

4001



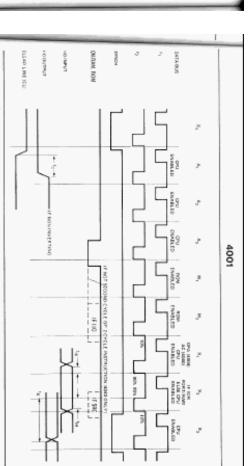


A.C. Characteristics TA = 0°C to 70°C, V<sub>50</sub> = V<sub>D0</sub> = 15V ±5%

			Į,			
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
A31	Clock Period	1.35		2,0	,450c	
ngu	Clock Rise Time			g	TK.	
3¢1	Clock Fall Times			g	3	
Welch	Clock Width	380		480	200	
10¢1	Clock Delay \$1 to \$2	400		550	75	
tøp2	Clock Delay \$2 to \$1	150			2	
Mg	Data-In, CM, SYNC Write Time	360	100		ns.	
(FLI) <sup>H3</sup>	Data-In, CM, SYNC Hold Time	đ	20		7,5	
t <sub>08</sub> [2]	Set Time (Reference)	0			25	
tAOC	Data-Out Access Time					Cour -
	Data Lines			930	ns	500pF Data Lines
	SYNC			930	ns.	500pF SYNC
	CM-ROM			930	ns.	160pF CM-ROM
	CN-RAM			900	ns.	SOpF CM-RAM
ť	Data-Out Hold Time	50	150		ns	Cour = 20pF
tis	I/O Input Set-Time	50			ņ	
HII	I/O Input Hold-Time	100			ns	
ō	I/O Output Delay			1500	ns.	C <sub>DUT</sub> = 100pF
	I/O Outstand Lines Delaw on Class			ienn	200	C

Tage to both surfaces. GM-History of control of the dy training order which clocks these times out. Tog it
the arms output access time returned to the leading edge of the next eye tick private.
 All MCS-80 components which may transmit instruction or data to 4004/4040 at Noy and Xy always enter a floot state
unit the 4004/4040 states over the data bound Xy and Xy arms. Therefore the tip expurience at leaveys insured since each
component contributes 10aA of testage current and 10pF of capacitance which guarantees that the data but cannot change
feater stant (V)a.
 CL on the 4001 is used to saynchronously clear the output IIIp-lings associated with the I/D lines.

8.94



Flaure 1. Timing Disgram

DUTPUT VOLTAGE OVE

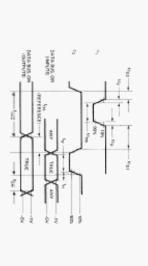


Figure 2. Timing Detail

## Programming Instructions

delays, programs should be specified in the following format. To insure optimum handling of ROM programs and avoid

### Paper Tape Format\*

model 33ASR reletype produces: A 1" wide paper tape using 8 bit ASCII code, such as a

### A. Preamble

- Preceding the first word field and following the last word field, there should be a leader/trailer sist of rubout punches. length of at least 25 characters. This should con-
- Included in the tape before the leader, and precoded by another leader, should be the cus-ROM pattern number. more than one pattern is being transmitted, the tomer's complete telex or two number and it
- davios type number or ROM number. The field should be framed by an "I" and "-" The first ROM pattern preamble field is the

mation encoded in decimal (two digits), and enclosed by "C" and "S", as in This should be followed by the chip select infor

00 N S78

The valid select digits for the 4001 are 0-15

"C155" - "C155"

portby-port basis with the connections to be made separated by commas, and enclosed in Finally, the I/O options would be specified on a

"(n1, n2, n3 . . .)".

be in parentheses for each I/O pin. tions. These connections are consecutively num-bened from 1-10. It is these numbers that should ciated with one I/O line. Hence, for a 4001 there Each I/O pin has a series of 10 possible connecwill be four bracketed collections of I/O options. where (n1, n2 . . .) are the option numbers also

"[ )" indicates no connection "[2,5,7]" indicates connections "(11)" indicates only #1

avoid illegal combinations I/O options should be placed on the tape sequen-tially for the 4001 from I/OO-I/O3(4), Always

#2, 5 and 7.

\*NOTE: Cards may also be submirted

ROM Code

The format requirements are as follows

- All word fields are to be punched in consecutive the N x 8 ROM organization ander, starting with word field 0 (all addresses low). There must be exactly N word fields for
- level output (V<sub>SS</sub> or logic 0 for MCS40 CPUs) and a Niresults in a low level output (V<sub>DD</sub> or logic Each word field must begin with the start charac If for MCS-40 CPUs). and F. Within the word field, a Presults in a high must be exactly 8 data characters between the B ter B and end with the stop character F, There

Example of 256 x 8 format (N=256)



- of error checking. It may be helpful to insert the may be easily listed on the teletype for purposes B's or F's may be inserted. Carriage return and Between word fields, comments not contains word fields. evord number (as a comment) at least every four these carriage returns, etc., are inserted, the tape least between every four word fields). When line feed characters should be inserted (as a "comment") just before each word field (or at
- Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a user on the Verification Listing tape. for testing. The values will be specified to the lested by Intel. The bit value will be fixed to allow allows the optimum default bit values to be sedicate a single bit - "Don't Care" setting. This "0" and "1" setting respectively, an "X" will in-

Venuesi. which might conceivably have different assigned be repeats of word 9 (except for Don't Care bits position 10, then words 10, 11, 12, and 13 will More that if a repeat count of 4 is given in word the last BPNF word encountered is to be word may be used. This indicates that the data in In the place of a standard BPNF word, a "B"nF" repeated for the next n words (1 \le n \le 1023).

by the remaining word count in a repeat count remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed To indicate that an entire block (such as the

> XXXX ZZ P4001 pppp INTEL PATTERN NUMBER

E P

## MCS® CUSTOM ROM ORDER FORM

ROM

APP		STD	S#
DATE	00	27	Por Intel use only INDIP

DATE\_ P.O. NUMBER CUSTOMER.

punched cards or punched paper tage per the formats designated on this order form. Additional forms are available from Intel All eustion 4001 RCM orders must be submitted on this form. Programming information should be sent in the form of computer

### MARKING

The marking as shown at the right must contain the lineal logo, the product type (P4001), the 4-digit lineal pattern humber (P9PP), of date code (XXXX), and the 2-digit chip number IDD. An optional customer identification number may be substituted for the chip number (ZZ), Optional Customer Number (Ingermum 6 characters or spaces).

CUSTOMER NUMBER

DATE CODE CUSTOMER NUMBER

## MASK OPTION SPECIFICATIONS

0 through 15-- DDI. (Must be specified—any number from A. CHIP NUMBER.

page). Examples of some of the pos-sible I/O options are shown below: B. I/O OPTION - Specify the connection numbers for each I/O pin (next

NECTIONS REQUIRED EXAMPLES - DESIRED OPTIONICON

- 1. Non-inverting output 1 and 3 are gannected.
- inverting output = 1 and 4 are connected.
- Non-inverting input into input ratio tool only 5 a connected.
- Inverting input limput resister to VggI
   2, 6, 7, and 9 are connected

- Non-inverting input (input resistor to Vogs) 2, 7, 8, and 10 are con
- 6. If impolt and originat are missed on the same port, are area used at the outpoils must have the internal re-sistent connected on either Vogo or Vogo 88 area 90 or 8 and 10 must be uponected. This is included to Votil. ing purposes. For example, if there are two inverting inputs (with no input resister) and two non-inverting outputs, the connection would be made as follows:

Inputs - 2 and 6 are connected Outputs - 1, 3, 8, and 9 are con-

If the pine on a port are all inputs or all outputs, the internal resisters do not have to be connected. 1, 3, 8, and 10 are connected

C. 4001 CUSTOM ROM PATTERN acters should be written as a "P" for perticular outtomer pattern, the chan case, a printout of the truth table must cards or punched paper tapa. In either Programming information should be output = V<sub>DD</sub> (negative logic "1"). logic "0") or an "N" for a low level a high level output " V<sub>SS</sub> (negative sent in the form of computer punched accompany the order. Based on the

Note that:

NOP = BPPPP PPPPF = 0000 0000

