

## A Single supply level shifting circuit

A recurring problem when working with single supply devices such as the A/D converter used on the PMod board is driving them with zero referenced inputs which swing between positive and negative voltage levels. This note analyzes an op-amp circuit that can be used to shift a zero volt referenced input to a reference equal to one-half the supply voltage.

The resistors included in the workstation boxes have an accuracy of  $\pm 5\%$ . This means there will be a small amount of level shift and gain error. In a more “real” situation one might to use more accurate resistors or an integrated circuit designed specifically for this application.

The output impedance of any signal source used with this circuit will also have an effect.

### A.1 Analysis

The op-amp in Figure 3 is assumed to be powered using the same supply voltage,  $v_s$  as the devices that follow it.

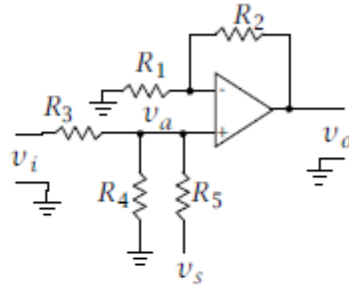


Figure 3: Single supply op-amp level shifting circuit.

Summing the currents flowing into the positive input's node gives

$$\frac{v_i - v_a}{R_3} + \frac{v_s - v_a}{R_5} = \frac{v_a}{R_4}$$
$$\frac{v_i}{R_3} + \frac{v_s}{R_5} = v_a \left( \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5} \right)$$

$$v_a = \left( \frac{v_t}{R_3} + \frac{v_s}{R_5} \right) \frac{R_3 R_4 R_5}{R_3 R_4 + R_3 R_5 + R_4 R_5}$$

The voltage between the plus and input nodes is assumed to be zero. Giving

$$v_o = v_a \frac{R_1 + R_2}{R_1}$$

$$v_o = \left( \frac{v_t}{R_3} + \frac{v_s}{R_5} \right) \frac{R_3 R_4 R_5 (R_1 + R_2)}{R_1 (R_3 R_4 + R_3 R_5 + R_4 R_5)}$$

The gain to  $v_s$  is

$$g_s = \frac{R_3 R_4 (R_1 + R_2)}{R_1 (R_3 R_4 + R_3 R_5 + R_4 R_5)}$$

The gain to  $v_t$  is

$$g_t = g_s \frac{R_5}{R_3}.$$

The equation for  $g_s$  gives the relation

$$g_s R_1 (R_3 R_4 + R_3 R_5 + R_4 R_5) = R_3 R_4 (R_1 + R_2).$$

The goal in this note is to center the output level at  $v_s/2$  which gives

$$\frac{(R_3 R_4 + R_3 R_5 + R_4 R_5)}{R_3 R_4} = \frac{2(R_1 + R_2)}{R_1}.$$

$$1 + \frac{R_5}{R_4} + \frac{R_5}{R_3} = 2 \left( 1 + \frac{R_2}{R_1} \right)$$

The values of  $R_3$  and  $R_5$  are related by the desired signal gain  $g_t$ .

$$\frac{R_5}{R_4} + 2g_t = 1 + \frac{2R_2}{R_1}$$

If  $R_4 = R_5$  then

$$g_t = \frac{R_2}{R_1}.$$

## A.2 A design procedure

Choose a signal gain  $g_t$  and a value for  $R_3$ . Then

$$R_4 = R_5 = 2g_t R_3.$$

The  $R_1$  and  $R_2$  values are related as

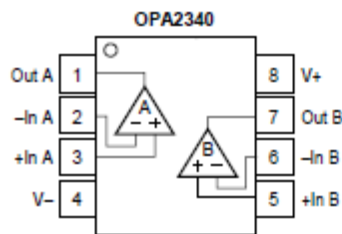
$$R_2 = g_t R_1.$$

Typically one keeps the  $R_n \geq 10k$ ,  $n = 1, 2, 3, 4, 5$ .

### A.3 Choice of op-amp device

Almost all of the manufacturers making integrated circuit op-amp devices sell low voltage, rail-to-rail devices. Many of these will work over unity gain bandwidths of 5 MHz and higher.

EECS currently using the Burr-Brown (TI) 8-pin OPA2340 dual op-amp. One of the reasons this was chosen was because it was still available at DigiKey in 8-pin DIP package. Though hole components such as the 8-pin DIP package are slowing vanishing.

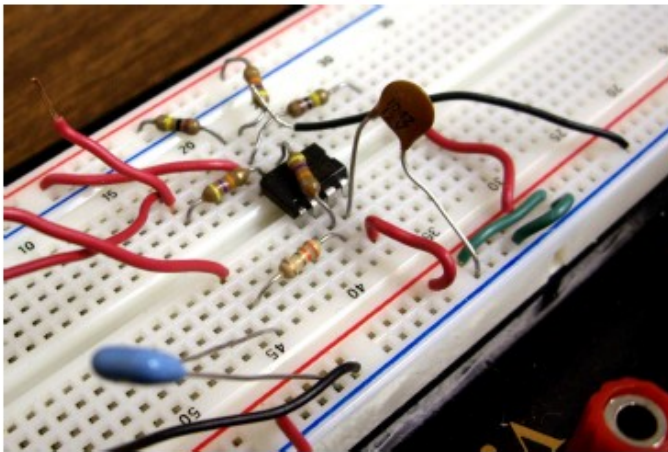


Supply voltage	2.7V to 5.5V
Unity gain bandwidth	5.5 MHz

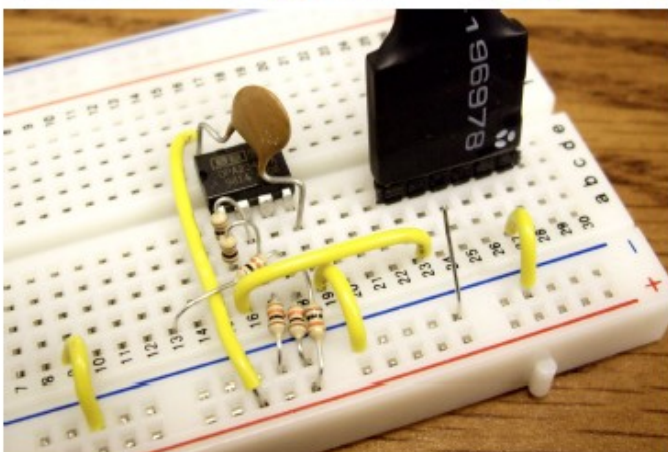
Figure from the Burr Brown OPA340 data sheet.

It is strongly recommended that a bypass capacitor on the order of  $0.1 \mu\text{F}$  be placed across  $V_{cc}$  and ground as close to the chip as feasible. Using the white plug boards it is easy to mount the capacitor bridging the chip and straddling its sides. This is done to enhance stability (i.e., to prevent it from oscillating) and to perhaps improve a noise performance.

### A.4 White board construction



This is an example of how NOT to build one channel of level shifting. Notice the disc bypass capacitor is not bypassing the chip but a piece of wire. TOTALLY in the wrong place. This unit was claimed to be “noisy”.



This is an example of a good implementation of one channel of level shifting. Notice the disc bypass capacitor is bridging the op-amp chip. The single wire sticking up was used to connect a scope probe ground.