Application of Filter Sharpening to Cascaded Integrator-Comb Decimation Filters

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***Abstract*—A new architecture for the implementation of high-order decimation filters is described. It combines the cascaded integrator-comb (CIC) multirate filter structure with filter sharpening techniques to improve the filter's passband response. This allows the first-stage CIC decimation filter to be followed by a fixed-coefficient second-stage filter, rather than a programmable filter, thereby achieving a significant hardware reduction over existing approaches. Furthermore, the use of fixed-coefficient filters in place of programmable-coefficient filters improves the overall throughput rate. The resulting architecture is well suited for single-chip VLSI implementation with very high data-sample rates. Applications include all-digital subband tuning for wideband communication links and signal analysis.**

I. Introduction

IN MANY communication and signal processing systems, it is necessary to isolate a very narrowband signal from a very wideband signal. For example, in a wideband satellite communication link, there might be several different signals combined into a single wideband channel for down link to a ground receiver(s). The ground-based receiver must then be able to isolate the signal of interest and remove all the other signals within the channel. Such narrowband signal isolation is sometimes referred to as subband tuning. As these types of systems become more complex, and their data rates increase, it becomes increasingly desirable to implement as much of the system as possible with digital circuits. Eliminating the need for expensive analog components having characteristics that vary widely over time and with environmental conditions reduces the overall system cost while also improving manufacturability and reliability. Furthermore, a wide range of digital signal processing (DSP) techniques can be drawn upon to greatly enhance system performance and more efficiently use the data transmission bandwidth. Recent advances in integrated circuit (IC) fabrication technology, particularly CMOS, coupled with advanced DSP algorithms and architectures are making possible single-chip all-digital solutions to complex communication and signal processing subsystems such as subband tuners.

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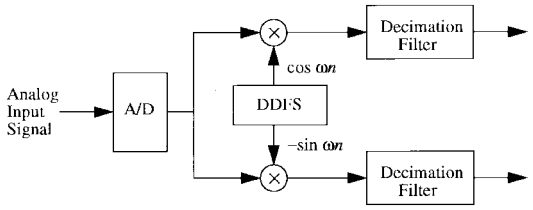


Fig. 1. Block diagram of an all-digital subband tuner.

One possible approach to narrowband signal isolation in an all-digital system is to first digitally translate the signal of interest down to baseband using a quadrature direct digital frequency synthesizer (DDFS) and two multipliers. This produces a complex signal having in-phase (I) and quadrature (Q) components with the signal of interest centered around DC. The signal of interest can then be isolated by two digital lowpass filters and decimated to lower the output sample rate. A block diagram of such a system is shown in Fig. 1. Ideally, both the DDFS output frequency (i.e., the center frequency of the band being tuned down to baseband) and the decimation ratio (i.e., the bandwidth of the desired signal) would be *programmable* to maximize the overall system's flexibility. For such a programmable system, the digital decimation filter is the *key* component required to provide an efficient single-chip solution for the overall system.

This paper presents architectures for the system's digital decimation filters that are suitable for efficient single-chip VLSI implementation for high data rates. We will briefly discuss a cascaded integrator-comb (CIC) decimation filter architecture proposed by Hogenauer [1] and then propose a modified CIC architecture that provides significantly improved performance over the traditional CIC approach at very little extra cost. We will then discuss an example with specifications suitable for use in a wideband satellite communication system. We will also compare the proposed architecture with the traditional CIC architecture [2] and with a recirculating halfband filter architecture recently proposed by Samueli and Lin [3].

II. Cascaded Integrator-Comb Filter

The CIC filter architecture is based on a class of FIR prefiltering techniques for multirate applications proposed by Hogenauer [1]. A CIC decimation filter consists of two main sections: an integrator section, which is a cascade of L

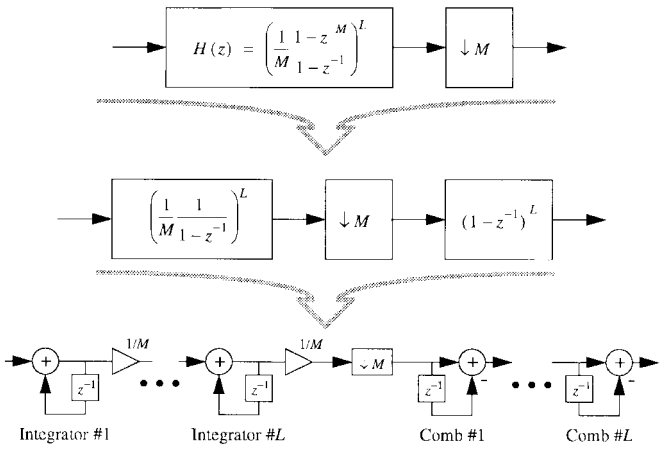


Fig. 2. Block diagram of a CIC decimation filter.

integrators with the transfer function

$$H_I(z) = \left(\frac{1}{M}\,\frac{1}{1-z^{-1}}\right)^L \tag{1}$$

and a comb section, which is a cascade of L combs with the transfer function

$$H_C(z) = (1-z^{-1})^L. \tag{2}$$

The integrator and comb sections are separated by a decimator with a decimation factor M, as shown in Fig. 2. Because of this filter's simplicity and its efficient structure, it is very suitable for VLSI implementation at high data rates. Additionally, the comb section operates at the lower data rate, resulting in smaller chip area and lower power dissipation. The CIC decimation filter can be viewed as a single high-sample-rate filter that precedes the decimator having the transfer function

$$H(z) = \left(\frac{1}{M}\,\frac{1-z^{-M}}{1-z^{-1}}\right)^L = \left(\frac{1}{M}\sum_{k=0}^{M-1} z^{-k}\right)^L. \tag{3}$$

This filter, which is obtained by simply moving the comb section through the decimator, is a cascade of L copies of an Mth-order FIR filter whose coefficients specify a rectangular time-domain window. The scaling factor $1/M$ compensates for the filter's intrinsic DC gain. The frequency response of the CIC filter can be expressed as

$$H(e^{j\omega}) = \left\{\frac{\sin\dfrac{\omega M}{2}}{M\sin\dfrac{\omega}{2}}e^{-j\omega[(M-1)/2]}\right\}^L \tag{4}$$

which clearly describes a linear-phase filter with a lowpass $\sin Mx/\sin x$ characteristic. The frequency response has nulls at integer multiples of $(1/M)F_s$, where F_s is the high-rate sampling frequency, and thus, the frequency bands that are aliased into the desired baseband signal by the decimation operation are centered around nulls. This provides "natural" alias-rejection. Fig. 3 shows the frequency response for a single-stage ($L = 1$) CIC filter with a decimation ratio of $M = 8$ (normalized with respect to the high sampling rate $F_s = 1$).

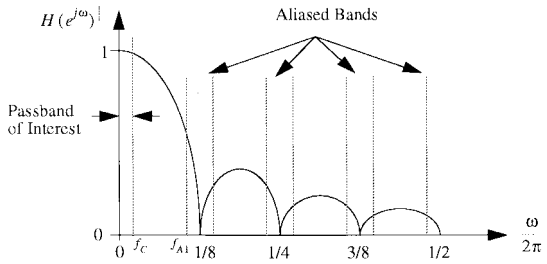


Fig. 3. Single-stage CIC frequency response for $M = 8$.

The CIC filter has a very wide transition band, and the passband of interest (0 to f_C in Fig. 3) is typically only a small portion of the resulting bandwidth after the M-fold decimation. In order to isolate this small band and remove the frequencies in the wide transition band (where most of the aliasing due to the decimation occurs), the CIC filter is usually followed by a second decimating lowpass filter stage. Its decimation ratio is usually significantly smaller than that of the CIC stage (typically 16 or less). The decimation factor of this second stage will determine the frequency at which the worst-case aliasing will occur (f_{A1} in Fig. 3) and will also determine the edge frequency of the passband of interest (f_C in Fig. 3), where the worst-case passband distortion will occur. For the case of a second filtering stage with a decimation ratio of 8, the edge of the passband of interest (normalized with respect to the high sampling rate $F_s = 1$) would be at $f_C = (\pi/8M)(1/2\pi) = (1/16M)$, where M is the decimation ratio of the CIC stage. Similarly, the worst-case aliasing would occur at the edge of the first aliased band at $f_{A1} = (1/M - 1/16M) = 15/16M$. The worst-case passband deviation and alias rejection for a cascade of L CIC stages followed by a lowpass filter with a decimation ratio of 8, as a function of the CIC decimation ratio M, is shown in Fig. 4 for values of L from 1 to 6. For example, a cascade of four stages (i.e., $L = 4$) has a worst-case passband deviation of approximately 0.22 dB ($M = 10$ case) and a worst-case alias rejection of approximately 80.7 dB ($M = 2$ case). As M increases beyond 10, the passband deviation and alias rejection remain fairly constant. Fig. 4 was obtained by direct evaluation of (4).

It can be seen clearly from Fig. 3 that the CIC filter introduces a droop in the passband of interest. Fig. 4 shows that this droop is dependent on the CIC decimation ratio M. For an overall system with a fixed decimation ratio, this is not a problem because the decimating lowpass filter following the CIC filter can be designed to compensate for the known amount of passband droop, and it can be implemented efficiently as a fixed-coefficient FIR filter. However, for a system requiring programmable decimation ratios, the second stage decimating lowpass filter must be a *programmable* filter to allow for the variation of the droop. For narrowband systems or applications where the decimation ratio of the CIC is guaranteed to be very large, this programmable filter

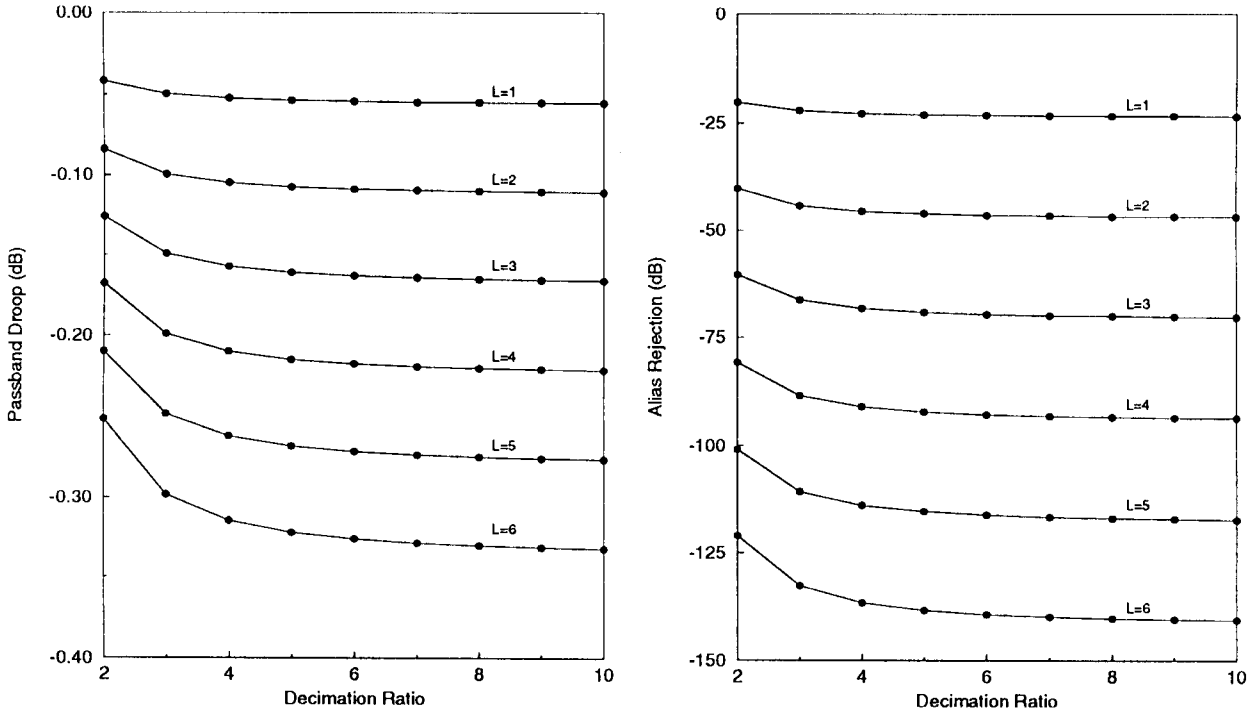


Fig. 4. Worst-case passband droop and alias rejection for a cascade of L CIC filters followed by a lowpass filter with decimation ratio of 8.

can be implemented with a series of computations using a single multiplier and accumulator because the data rate at the output of the CIC decimation filter is guaranteed to be very low. However, for wideband systems or systems required to accommodate both small and large overall decimation factors, a significant amount of hardware resources must be devoted to the implementation of this second filter stage.

In practice, the useful information in the CIC filter's output signal will not occupy its entire output bandwidth $(F_s/2M)$ because the filters in the second stage (following the CIC) will have some nonzero-width transition bands. These filter transition bands are typically on the order of 10–20% of their input bandwidth $(F_{s\_in}/2)$, depending on the specific application. For a second stage filter with a 20% transition band, only 80% of the CIC filter's output would be within the second stage filter's passband; the other 20% would be within its transition band. If the second-stage filter has a decimation ratio of 8, the edge of the CIC filter's passband would be at the frequency $f_C = 1/20M$ (i.e., 80% of $1/16M$, normalized with respect to the high sampling rate $F_s = 1$), where M is the CIC filter's decimation ratio. Similarly, the edge of the first aliased band (where worst-case aliasing occurs) would be at the normalized frequency $f_{A1} = (1/M - 1/20M) = 19/20M$. The worst-case passband droop and alias rejection for a cascade of L CIC stages followed by a lowpass filter with a decimation ratio of 8 and a 20% transition band, as a function of the CIC decimation ratio M, is shown in Fig. 5 for values of L from 1 to 6. Fig. 5 was obtained by direct evaluation of (4). For the case of a cascade of four stages (i.e., $L = 4$), the worst-case passband droop is approximately 0.14 dB ($M = 10$), and the worst-case alias rejection is approximately 88.4 dB ($M = 2$) as compared with 0.22 and 80.7 dB reported above for the case of 100% utilization of the CIC filter's output bandwidth. As M increases beyond 10, the passband droop and alias rejection remain approximately constant.

III. Sharpened CIC Filter

The limitations of the CIC-based architecture for programmable decimating digital filters are due to the need for a *programmable* second-stage filter to compensate for the variable droop in the passband of the CIC filter response. The proposed new architecture overcomes these limitations by significantly reducing this passband droop. This makes it possible to design a fixed-coefficient second stage filter to extract the passband of interest and further reduce the output sample rate. This reduces the chip area required for the overall system while also increasing the system's maximum data throughput rate.

The new CIC architecture is based on a technique for sharpening the response of a filter proposed by Kaiser and Hamming [4]. This technique attempts to improve both the passband and stopband of a symmetric nonrecursive filter by using multiple copies of the same filter. In the simplest case, the sharpened filter $H_{new}(z)$ can be related to the original filter $H(z)$ by the following equation: $H_{new}(z) = H^2(z)[3 - 2H(z)]$. A block diagram of a sharpened filter is shown in Fig. 6. The implementation of the sharpened filter requires three copies of the original filter, a scaling multiplier of value 3, a trivial multiplier of value -2, an adder, and a delay line to equalize the group delay through the two channels in the first part of the structure. If the original filter $H(z)$ is chosen to be a single-stage CIC filter, the resulting sharpened filter will have significantly reduced passband droop and improved alias rejection. Fig. 7 shows a plot of the frequency response of a single-stage CIC filter with $M = 8$ and that of a sharpened

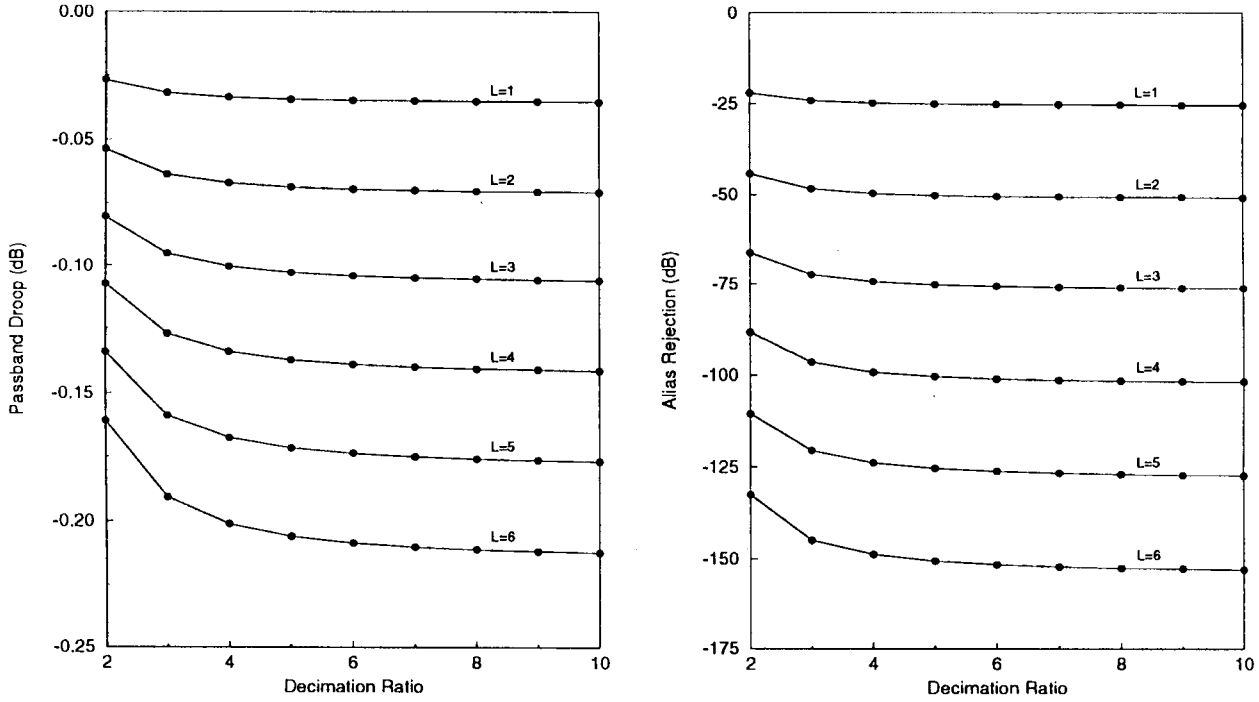


Fig. 5. Worst-case passband droop and alias rejection for a cascade of L CIC filters followed by a lowpass filter with decimation ratio of 8 and a 20% transition band.

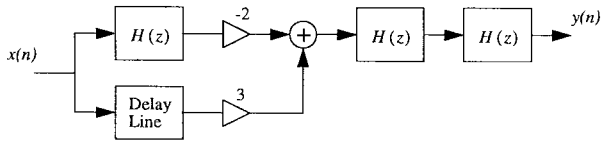


Fig. 6. Block diagram of a sharpened filter.

CIC filter using a single-stage CIC filter as the $H(z)$ building block. The elimination of droop within the passband of interest can be seen clearly.

Using (4), the frequency response of the sharpened CIC filter with an $H(z)$ building block consisting of an L-stage CIC filter can be expressed as

$$|H(e^{j\omega})| = \left| \left[3\left(\frac{\sin\frac{\omega M}{2}}{M\sin\frac{\omega}{2}} \right)^{2L} \right] - \left[2\left(\frac{\sin\frac{\omega M}{2}}{M\sin\frac{\omega}{2}} \right)^{3L} \right] \right|. \tag{5}$$

Since all of the $H(z)$ building blocks used in the sharpened CIC filter are linear-phase filters, the overall filter will have linear phase. As discussed previously, if the filter stage following the sharpened CIC filter (which is needed to extract the passband of interest) has a decimation ratio of 8, the edge frequency of the passband of interest (worst-case passband distortion) will be at the normalized frequency $f_C = 1/16M$, and the edge of the first aliased band (worst-case alias rejection) will be at the normalized frequency $f_{A1} = 15/16M$, where M is the decimation factor of the CIC filter. Fig. 8, which was obtained by direct evaluation of (5), shows a plot of the worst-case passband distortion and worst-case alias rejection as a function of the decimation ratio M for the sharpened CIC filter using an L-stage CIC for the $H(z)$ building blocks for

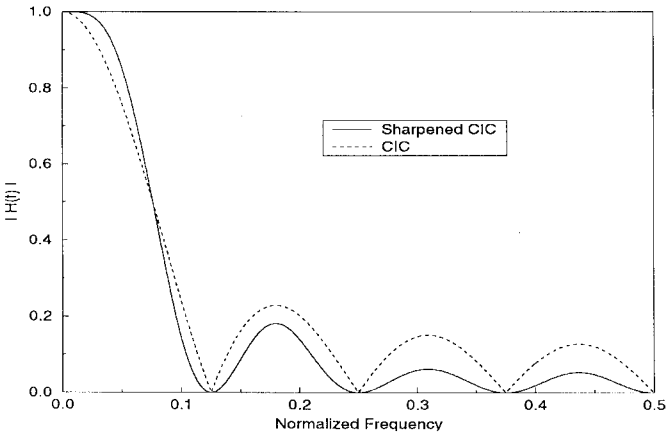


Fig. 7. Example of CIC filter sharpening ($M = 8$).

values of L from 1 to 4. For example, if a two-stage CIC is chosen for the $H(z)$ building blocks (i.e., $L = 2$), the sharpened CIC filter will have a worst-case passband distortion of 0.004 dB ($M = 10$ case) and a worst-case alias rejection of 71.2 dB ($M = 2$ case). As M increases beyond 10, the passband distortion and alias rejection remain approximately constant. When compared with the results for the standard CIC filter (Fig. 4), it can be seen that the passband distortion has been reduced by more than an order of magnitude and even by as much as a factor of 40 for the $L = 1$ and $L = 2$ cases.

Again, the results improve for the case where the decimate-by-eight filter following the sharpened CIC filter has a 20% transition band (i.e., only 80% of the CIC filter's output is within the second-stage filter's passband). Under this assumption, the edge of the passband of interest would be at $f_C = 1/20M$, and the edge of the first aliased band would

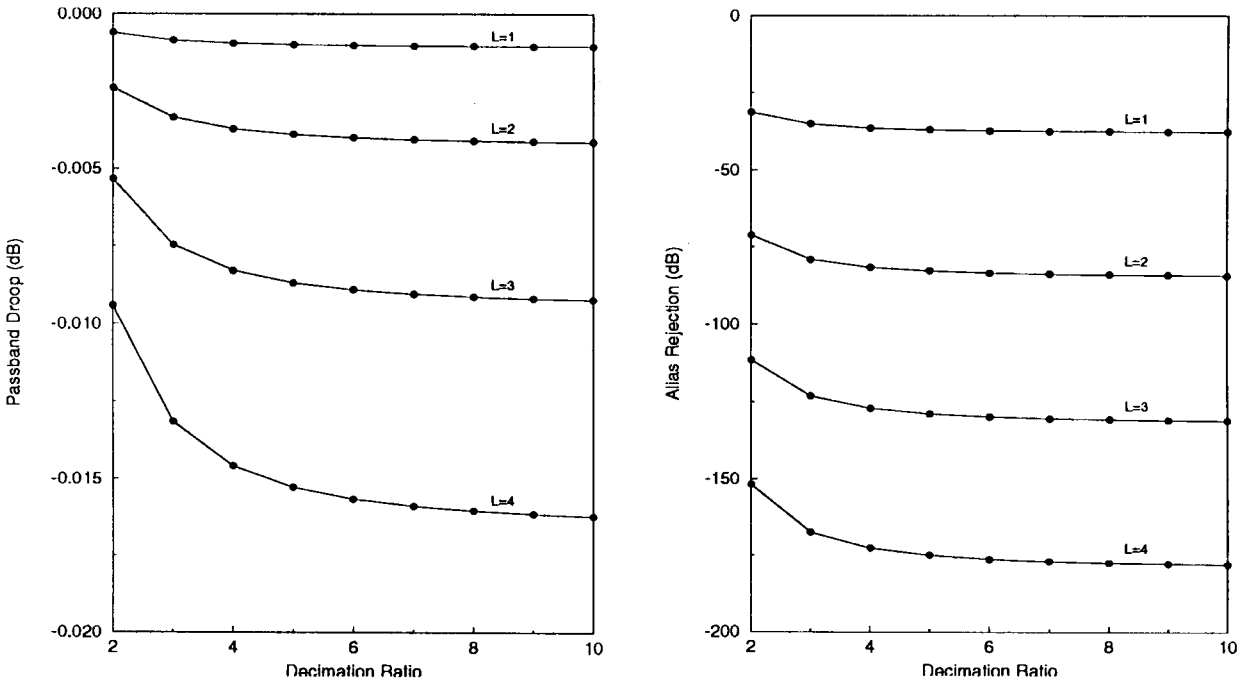


Fig. 8. Worst-case passband droop and alias rejection for the sharpened CIC filter followed by a lowpass filter with decimation factor of 8.

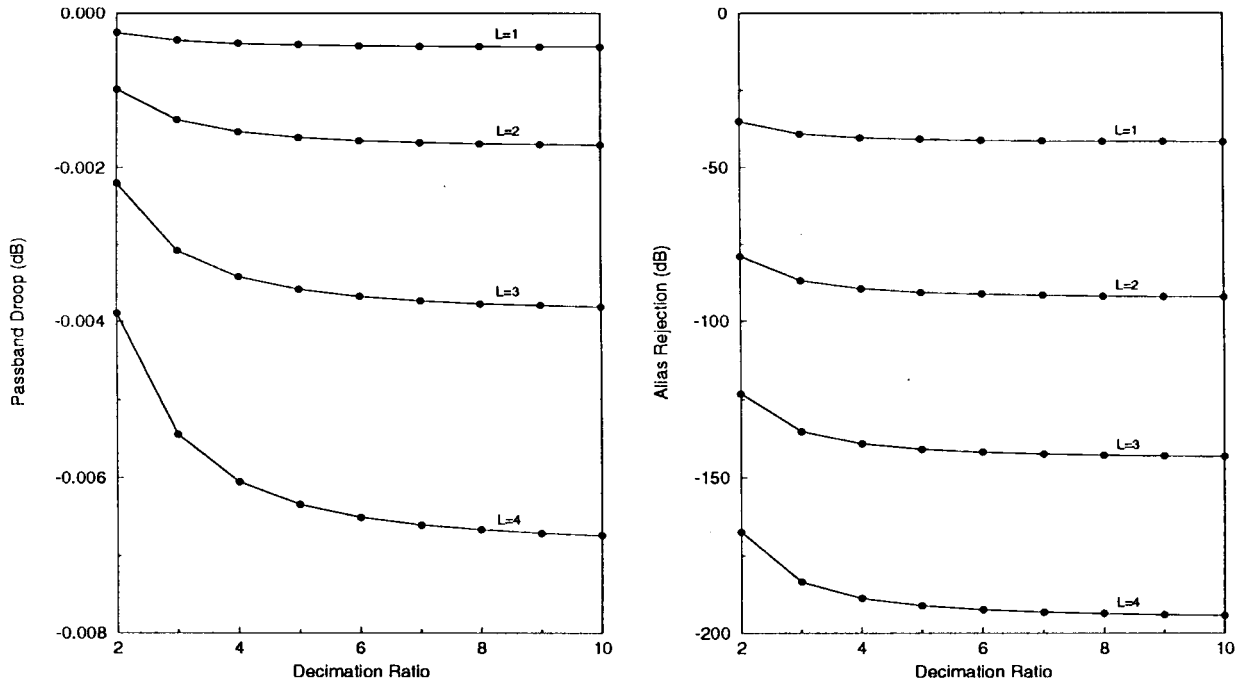


Fig. 9. Worst-case passband droop and alias rejection for the sharpened CIC filter followed by a lowpass filter with decimation factor of 8 and a 20% transition band.

be at $f_{A1} = 19/20M$ (this is where the worst-case aliasing occurs). The worst-case passband distortion and alias rejection for the sharpened CIC filter using an L-stage CIC for the $H(z)$ building blocks followed by a second stage filter with a decimation ratio of 8 and a 20% transition band, as a function of the decimation ratio M, for values of L from 1 to 4, are shown in Fig. 9. For the case of a two-stage CIC used as the $H(z)$ building block (i.e., $L = 2$), the worst-case passband distortion is 0.002 dB ($M = 10$), and the worst-case alias rejection is 78.9 dB ($M = 2$), as compared with 0.004 and 71.2 dB reported above for the case of 100% utilization of the CIC filter's output bandwidth.

IV. Sharpened CIC Decimation Filter Example

A programmable decimating digital filter using the sharpened CIC architecture with specifications suitable for wideband satellite communication systems has been designed as

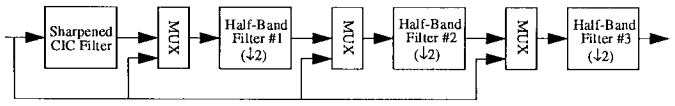


Fig. 10. Block diagram of a decimating digital filter using the sharpened CIC filter followed by three fixed-coefficient half-band filters.

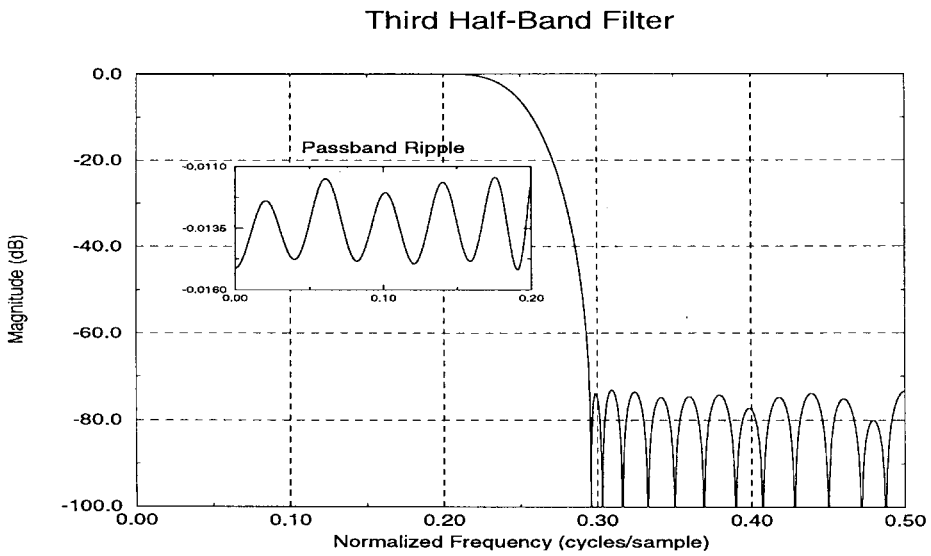
the cascade of a sharpened CIC filter and a fixed-coefficient lowpass filter with a decimation ratio of 8. The target specifications for the design are a single-chip solution with greater than 70-dB alias rejection and less than 0.01 dB passband deviation over programmable power-of-two decimation factors from 2 to 8192 that can operate at input data sample rates up to 200 MHz. In order to allow for programmable decimation ratios of 2^1, 2^2, and 2^3, the second-stage lowpass filter is implemented as a cascade of three fixed-coefficient halfband filters with a multiplexer at the input of each filter that selects either the input data or the data from the preceding filter. Thus, for a decimation ratio of 2^1, only the third halfband filter is used for a decimation ratio of 2^2, the second and third halfband filters are used, and for a decimation ratio of 2^3, all three halfband filters are used. For decimation ratios larger than 2^3 (i.e., 2^4 to 2^{13}), the sharpened CIC filter is programmed for a decimation factor of 2^{M-3}, and the three halfband filters perform the final 2^3 decimation. Fig. 10 shows a block diagram of this system. It should be noted that in this system, the sharpened CIC filter would only need to implement power-of-two decimation ratios from 2^1 to 2^{10}.

The three halfband filters in Fig. 10 were designed to have 20% transition bands (i.e., 80% output bandwidth utilization). Because the second halfband filter is always followed by the third halfband filter and, similarly, the first halfband filter is always followed by the second and third halfband filters, the transition band specifications of the first and second halfband filters can be relaxed, providing significant hardware reductions. Therefore, the third halfband filter will have the most stringent specifications, and its implementation will require the most hardware. The third halfband filter (of Fig. 10) was designed as a 47-tap FIR filter using canonical signed digit (CSD) coefficients to reduce the number of nonzero digits [5]. For a 20% transition band (i.e., 80% output bandwidth utilization), the filter has a passband edge frequency at 0.2 and a stopband edge frequency at 0.3 (normalized relative to its input sample rate $F_{s-in3} = 1$). After the filter's output is decimated by 2, the attenuated frequencies in the stopband (from 0.3 to 0.5 relative to $F_{s-in3} = 1$) will be aliased back into the passband (from 0.0 to 0.2 relative to $F_{s-in3} = 1$). When normalized relative to the output sample rate ($F_{s-out3} = 1$), the useful output from the filter will occupy the frequencies from 0.0 to 0.4 (80% of the output bandwidth). The frequencies from 0.4 to 0.5 (relative to $F_{s-out3} = 1$) will consist of information in the filter's transition band (from 0.2 to 0.3 relative to $F_{s-in3} = 1$). The filter achieves a minimum stopband attenuation of 73.1 dB (over the band from 0.3 to 0.5 relative to $F_{s-in3} = 1$) with a worst-case peak-to-peak passband ripple of 0.004 dB (over the band from 0.0 to 0.2 relative to $F_{s-in3} = 1$). Fig. 11 shows its frequency response and impulse response coefficients. Since it is a halfband filter, all the odd coefficients except the center one are zero. In addition, since it is a linear-phase filter, the coefficients are symmetric. Thus, only 13 fixed-coefficient multipliers are required to implement this filter. Furthermore, polyphase decomposition can be used to reduce the number of multiplications required per unit time (MPU) by a factor of two. Similar filters have been designed to operate at data rates in excess of 200 MHz in 1.0-μm CMOS technology [6].

Since the second halfband filter is always followed by the third halfband filter and its output is decimated by a factor of two, its required passband and stopband edges are at 0.1 and 0.4, respectively (normalized relative to its input frequency $F_{s-in2} = 1$). Frequencies in the band from 0.2 to 0.3 (normalized relative to its input frequency $F_{s-in2} = 1$) will be attenuated by the third halfband filter. It was designed as a 15-tap FIR filter with CSD coefficients requiring only four fixed-coefficient multipliers (the center tap coefficient being implemented as a simple one-bit shift), and it achieves a minimum stopband attenuation of 75 dB with a peak-to-peak passband ripple less than 0.0008 dB. Its frequency response and impulse response coefficients are given in Fig. 12.

The transition band requirements for the first halfband filter can be further relaxed. The required passband and stopband edges are 0.05 and 0.45, respectively (normalized relative to the filter's input sample rate $F_{s-in1} = 1$). The filter was designed as an 11-tap FIR filter using CSD coefficients [7], and it achieves a minimum stopband attenuation of 76.9 dB with a peak-to-peak passband ripple less than 0.0015 dB. Fig. 13 shows its frequency response and impulse response coefficients. Only three fixed-coefficient multipliers are required to implement this filter (again, the center tap coefficient is implemented as a simple one-bit shift). Thus, the overall second-stage decimate-by-eight filter can be implemented using only 20 fixed-coefficient multipliers.

Since the sharpened CIC filter will be followed by a decimate-by-eight second filter stage with a 20% transition band, Fig. 9 can be used to determine the required number of CIC filters for the $H(z)$ building blocks. From Fig. 9, it can be seen that a two-stage CIC filter $H(z)$ building block (i.e., $L = 2$) will meet the alias rejection requirement of 70 dB. The sharpened CIC (SCIC) filter will actually achieve a worst-case alias rejection of 78.9 dB. It should be noted that the overall performance of the system could be improved (up to 78.9 dB alias rejection) without changing the SCIC filter by designing the three halfband filters to achieve a higher stopband attenuation. Fig. 14 shows a block diagram of the SCIC filter using a two-stage CIC as the $H(z)$ building block. As with the CIC filter discussed previously, the decimator can be moved through the comb filter parts of the CIC filter building blocks. Since the SCIC filter only needs to accommodate power-of-two decimation ratios, the scaling multiplier at the input can be implemented as a simple programmable shifter. Thus, the complete SCIC filter requires only one multiplier (a scaling multiplier of value 3) and that multiplier operates at the reduced sample rate. It should be noted that the number of CIC stages cascaded to form the $H(z)$ building blocks must be a multiple of two. This is because the group delay of a single CIC filter is $(M-1)/2$ samples, and

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h(0)  = h(46) = -3.204346E-04 = - 2^-12 - 2^-14 - 2^-16
h(1)  = h(45) =  0.0
h(2)  = h(44) =  8.239746E-04 =   2^-10 - 2^-13 - 2^-15
h(3)  = h(43) =  0.0
h(4)  = h(42) =  1.770020E-03 = - 2^-9  + 2^-13 + 2^-14
h(5)  = h(41) =  0.0
h(6)  = h(40) =  3.356934E-03 =   2^-8  - 2^-11 - 2^-14
h(7)  = h(39) =  0.0
h(8)  = h(38) = -5.813599E-03 = - 2^-7  + 2^-9  + 2^-14 - 2^-16
h(9)  = h(37) =  0.0
h(10) = h(36) =  9.506226E-03 =   2^-7  + 2^-9  - 2^-12 - 2^-16
h(11) = h(35) =  0.0
h(12) = h(34) = -1.490784E-02 = - 2^-6  + 2^-11 + 2^-12 - 2^-16
h(13) = h(33) =  0.0
h(14) = h(32) =  2.282715E-02 =   2^-6  + 2^-7  - 2^-11 - 2^-13
h(15) = h(31) =  0.0
h(16) = h(30) = -3.500366E-02 = - 2^-5  - 2^-8  + 2^-13 + 2^-15
h(17) = h(29) =  0.0
h(18) = h(28) =  5.572510E-02 =   2^-4  - 2^-7  + 2^-10 + 2^-14
h(19) = h(27) =  0.0
h(20) = h(26) = -1.010742E-01 = - 2^-4  - 2^-5  - 2^-7  + 2^-11
h(21) = h(25) =  0.0
h(22) = h(24) =  3.161621E-01 =   2^-2  + 2^-4  + 2^-8  - 2^-12
    h(23)     =  4.992371E-01 =   2^-1  - 2^-10 + 2^-12 - 2^-15
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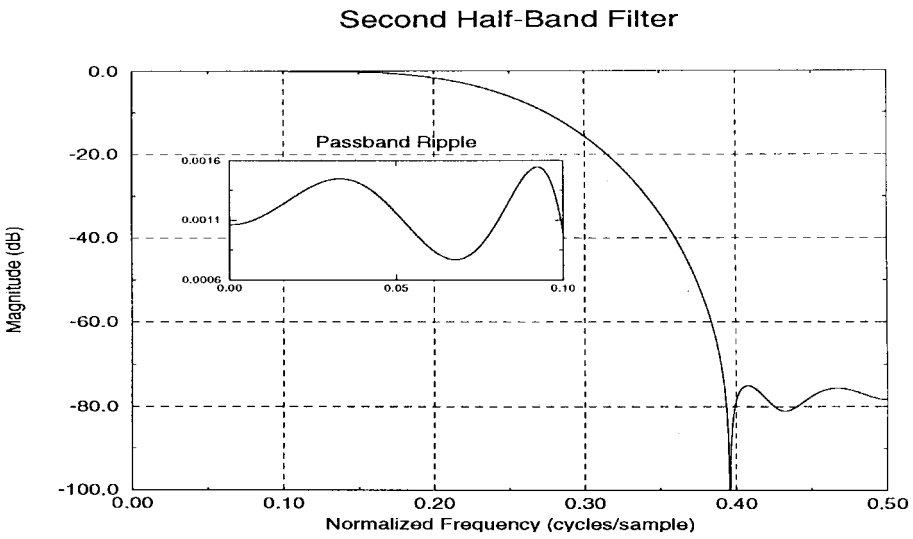
Fig. 11. Frequency response and impulse response coefficients for the third halfband filter.

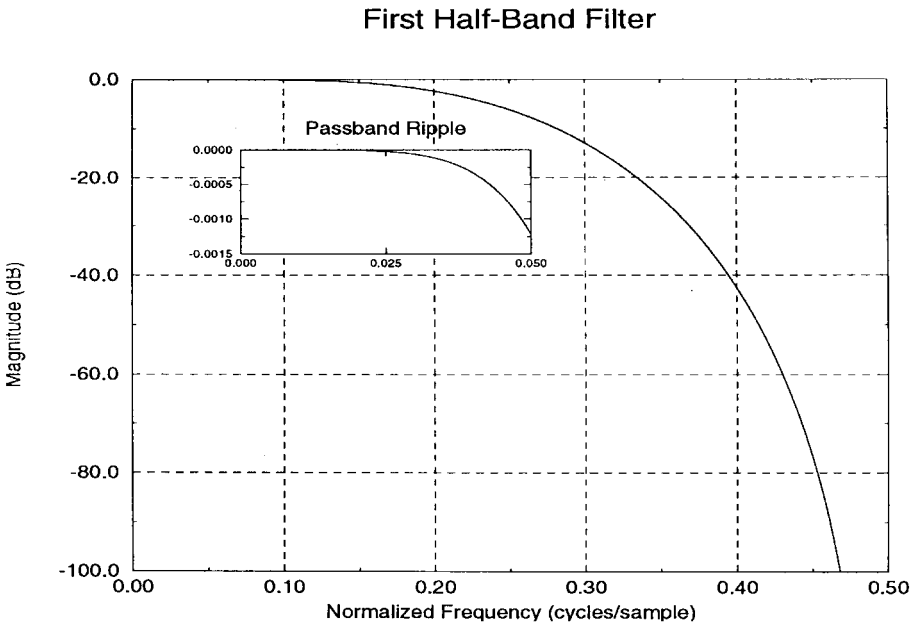
in order to be able to move the decimator through the delay equalizer (see Fig. 6), the delay must be a multiple of M. Thus, the $H(z)$ building blocks must be made up of an even number of cascaded CIC stages, with an additional z^{-1} being inserted at the input to make the total delay z^{-M}. This SCIC filter will achieve a worst-case alias rejection of 78.9 dB with a worst-case passband distortion less than 0.002 dB. It requires six integrator and six comb sections, whereas only four of each would be required in the traditional approach. However, the hardware savings of the fixed-coefficient second-stage filter more than compensate for the two additional multiplierless CIC stages (recall that a programmable-coefficient second-stage filter would be required in the traditional approach).

The overall decimating digital filter (consisting of the sharpened CIC and the three halfband filters) will achieve a worst-case passband distortion less than 0.01 dB and a worst-case alias rejection greater than 73 dB for programmable decimation ratios from 2 to 8192. Furthermore, the range of possible decimation factors could easily be extended since the decimation ratio of the SCIC filter stage (currently 2^1 to 2^{10}) is implemented as a simple programmable counter. In addiiton, the alias rejection could be improved up to 78.9 dB by modifying the halfband filters at the cost of slightly more hardware. Table I gives simulation results for the sharpened CIC filter followed by the three halfband filters, showing the worst-case distortion *after* decimation for each of the programmable decimation ratios. Recall that the decimation ratios 2^1, 2^2, and 2^3 do not use the sharpened CIC filter (only the halfband filters). Fig. 15 shows the simulated worst-case passband *after* decimation for the $M = 16$ case, where the sharpened CIC is programmed for a decimation factor of 2, and the three halfband filters provide an additional decimation factor of 8. We are currently in the process of designing a single-chip implementation of this programmable decimation filter that will provide 16-b input and output data and will operate at input data sample rates in excess of 200 MHz. We anticipate that the decimation filter will require a core area of 30 mm^2 using 0.8-μm CMOS technology. The filter will



$h(0) = h(14) = -2.441406\text{E-}03 = -2^{-9} - 2^{-11}$
$h(1) = h(13) = 0.0$
$h(2) = h(12) = 1.690674\text{E-}02 = 2^{-6} + 2^{-10} + 2^{-12} + 2^{-14}$
$h(3) = h(11) = 0.0$
$h(4) = h(10) = -6.762695\text{E-}02 = -2^{-4} - 2^{-8} - 2^{-10} - 2^{-12}$
$h(5) = h(9) = 0.0$
$h(6) = h(8) = 3.032227\text{E-}01 = 2^{-2} + 2^{-4} - 2^{-7} - 2^{-9} + 2^{-11}$
$h(7) = 0.5 = 2^{-1}$

Fig. 12. Frequency response and impulse response coefficients for the second half-band filter.



$h(0) = h(10) = 5.8593750\text{E-}03 = 2^{-8} + 2^{-9}$
$h(1) = h(9) = 0.0$
$h(2) = h(8) = -4.8828125\text{E-}02 = -2^{-5} - 2^{-6} - 2^{-9}$
$h(3) = h(7) = 0.0$
$h(4) = h(6) = 2.9296875\text{E-}01 = 2^{-2} + 2^{-5} + 2^{-7} + 2^{-8}$
$h(5) = 0.5 = 2^{-1}$

Fig. 13. Frequency response and impulse response coefficients for the first halfband filter.

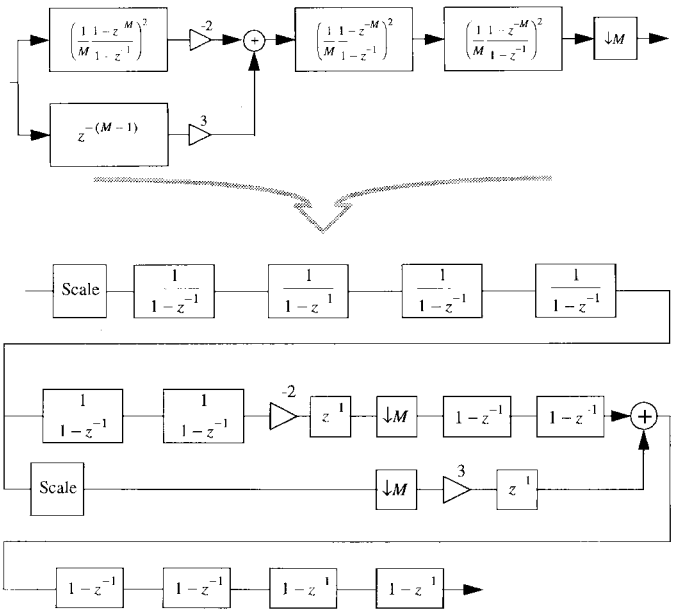


Fig. 14. Block diagram of a sharpened CIC filter using a two-stage CIC filter as the $H(z)$ building block.

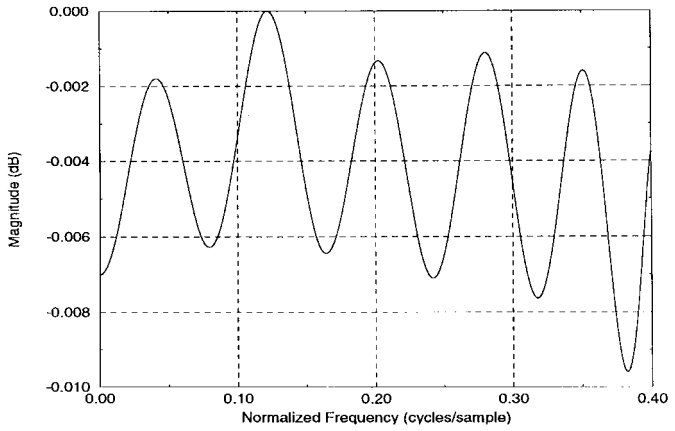


Fig. 15. Simulated passband after decimation for the complete decimation filter (sharpened CIC and three halfband filters) for the case of $M = 16$.

achieve greater than 73 dB alias rejection with less than 0.01-dB passband distortion over programmable decimation ratios from 2 to 8192.

V. Comparison with Other Approaches

Recently, a high-performance decimating digital filter has been implemented using a recirculating halfband filter architecture [3]. This single-chip realization of a high-order decimation/interpolation filter consists of a polyphase implementation of a halfband filter, where the output data can be recirculated to the filter's input. By "cascading" the halfband filter in this manner, various decimation/interpolation ratios can be realized. Since the sample rate at the output of each decimation "stage" (or at the input of each interpolation stage) of the filter is reduced by two, only half of the filter's resources are utilized at any given time. One way to more efficiently use the hardware would be to operate the filter at twice the data rate. However, a more useful way to efficiently utilize the hardware for subband tuning applications is to feed the output back to the input at the reduced sample rate. Thus, by continually feeding back the output of the filter, the overall utilization will approach 100%. Fig. 16 shows a block diagram of this architecture.

This programmable high-order decimation/interpolation filter was implemented in 1.0-μm CMOS technology. The IC contained 200 000 transistors and occupied a chip area of 87.36 mm^2 [8]. The chip can be programmed for any power-of-two conversion ratio up to 16 384 (2^1–2^{14}) and can accommodate throughput rates up to 100 MHz. Thus, this single decimation chip can isolate a 3-kHz narrowband signal out of a 50-MHz

TABLE I
Simulated Worst-Case Passband Distortion After Decimation Versus Decimation Factor

Decimation Factor	Worst-case passband distortion (dB)
2	0.00748664
4	0.00469985
8	0.00308263
16	0.00958937
32	0.00604246
64	0.00488694
128	0.00472363
256	0.00438328
512	0.00419868
1024	0.00411545
2048	0.00407759
4096	0.00405978
8192	0.00405779

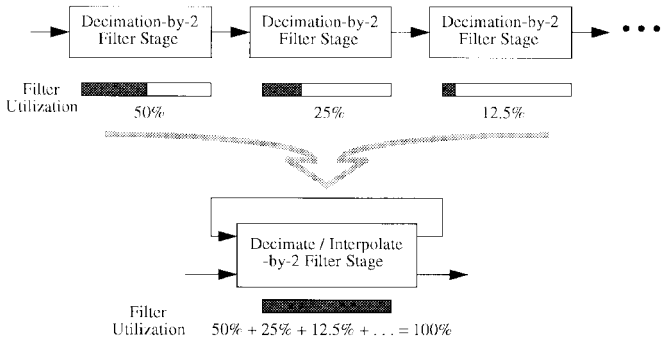


Fig. 16. Recirculating multistage decimation/interpolation filter architecture.

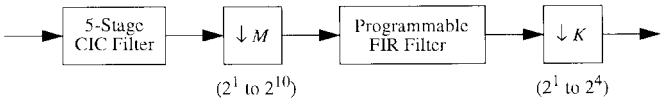


Fig. 17. Block diagram of Harris Semiconductor decimating digital filter IC.

wideband RF signal sampled at 100 MHz and at the same time convert the signal down to a 6.1 kHz sample rate. The overall filter has a worst-case alias rejection of 64.4 dB and a worst-case passband distortion of 0.008 dB. The halfband filter core is implemented as a 43-tap FIR filter with a 20% transition band using canonical signed digit (CSD) coefficients to reduce the number of nonzero digits and polyphase decomposition to reduce the number of multiplications required per unit time (MPU) by a factor of two. Because this is a fixed-coefficient filter (i.e., it has a fixed transfer function), it can be implemented efficiently with a minimal amount of hardware.

Although the implementation of this chip's halfband filter core is very efficient, the impact of this efficiency is diluted since over 75% of the chip area is devoted to circuitry implementing the registers of the 14 halfband filter stages. That is, even though only one set of multipliers and adders is used to implement all of the filters, each of the 14 stages (required to implement a conversion ratio of $2^{14} = 16\,384$) must have its own set of registers to store intermediate results. Thus, for large decimation/interpolation ratios, the chip does not take advantage of the large conversion ratio (i.e., it does not eliminate the storage of intermediate values that are never used). This IC cannot fully exploit this basic property of multirate systems because its architecture is based on a halfband filter core. Furthermore, the design of the IC is complicated by the need to generate and distribute 14 different clock signals to control the flow of data within the filter. In addition, this architecture cannot easily be extended to larger decimation factors. Each additional factor of two requires another set of registers to store intermediate values and the generation and distribution of another clock signal.

The decimating digital filter IC currently available from Harris Semiconductor [9] is an example of a CIC-based decimating digital filter. The chip consists of a five-stage decimating CIC filter with programmable decimation ratios from 2^1 to 2^{10} followed by a programmable FIR filter with programmable decimation ratios from 2^1 to 2^4. Thus, overall decimation ratios up to 2^{14} (16 384) can be achieved. The chip can implement any decimation ratio (it is not limited to power-of-two conversions). Fig. 17 shows a block diagram of this decimating digital filter IC. The Harris Semiconductor documentation [9] claims that the CIC filter can obtain an alias rejection of up to 96 dB. However, the results in Fig. 4 show that the alias rejection is dependent on the decimation ratio in the CIC stage and the decimation ratio in the following programmable FIR filter stage. In general, the IC can only obtain this level of performance for overall decimation ratios of at least 16, and it is, therefore, most useful for applications that do not require small decimation factors. Furthermore, the maximum input data sample rate of the IC is only 33 MHz, making it unsuitable for wideband applications. This limitation is primarily due to the programmable FIR filter that is implemented using a single multiplier and accumulator. In order to avoid the severe passband droop of the CIC filter for small overall decimation factors, most of the decimation must be performed in the programmable FIR filter stage, which further limits the maximum data throughput. For example, an overall decimation ratio of 10 could be achieved through a decimation ratio of two in the CIC filter stage and a decimation ratio of five in the programmable FIR filter stage. Since the second-stage filter decimates by a factor of five, the worst-case droop in the CIC filter's passband will occur at the frequency $f_C = 1/10M$ (normalized relative to the CIC filter's input sample rate $F_s = 1$), and the worst-case aliasing will occur at the frequency $f_{A1} = 9/10M$ (normalized relative to the CIC filter's input sample rate $F_s = 1$). Using (4) with $M = 2$ (CIC decimation factor) and $L = 5$ (number of CIC stages) for these frequencies gives a passband droop of 0.54 dB and an alias rejection of 80.6 dB. The passband droop could be compensated for in the programmable FIR filter, but the alias rejection cannot be improved in the second stage. Furthermore, the input data rate would be severely limited because the programmable FIR filter stage (implemented with a single multiplier and accumulator) would have to operate at half the input data rate (CIC decimation ratio $= 2$). Thus, the maximum input data rate would be 2×33 MHz$/N$, where N is the length of the second filter stage. The throughput could be improved by programming the CIC filter stage for a decimation ratio of five and the programmable FIR filter stage for a decimation ratio of two. Thus, the programmable FIR filter stage would operate at one fifth the input sample rate. However, since the second stage filter now only decimates by a factor of two, the worst-case droop in the CIC filter's passband would occur at the frequency $f_C = 1/4M$ (normalized relative to the CIC filter's input sample rate $F_s = 1$) and the worst-case aliasing would occur at the frequency $f_{A1} = 3/4M$ (normalized relative to the CIC filter's input sample rate $F_s = 1$). Using (4) with $M = 5$ and $L = 5$, the passband droop is 4.38 dB, and the alias rejection is 50.7 dB. Again, the passband droop can be compensated for in the second-stage programmable FIR filter, but the alias rejection cannot be improved. Because of these problems, this IC is most suitable for applications with a large first-stage decimation factor.

The CIC filter architecture, when combined with a programmable FIR filter using a single hardware multiplier/accumulator, provides a very efficient single-chip implementation of a programmable decimation filter. However, for small overall decimation factors, the chip's maximum data throughput rate is severely limited by the single multiplier in the programmable FIR filter. The use of a dedicated programmable FIR filter to improve the data throughput would significantly increase the amount of chip area required, making a single-chip solution expensive or even impossible.

VI. Conclusions

The proposed sharpened CIC programmable decimating filter architecture enables a very high-performance single-chip solution for an all-digital subband tuner for use in wideband communication links. It retains the small-size advantages of the traditional multiplierless CIC approach but overcomes the performance limitations associated with that approach by allowing the second-stage filter to be implemented as a fixed-coefficient filter rather than a programmable filter, thereby providing a flexible, programmable single-chip system capable of very-high data throughput rates.

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