FACULTY OF SCIENCE
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Master's Thesis

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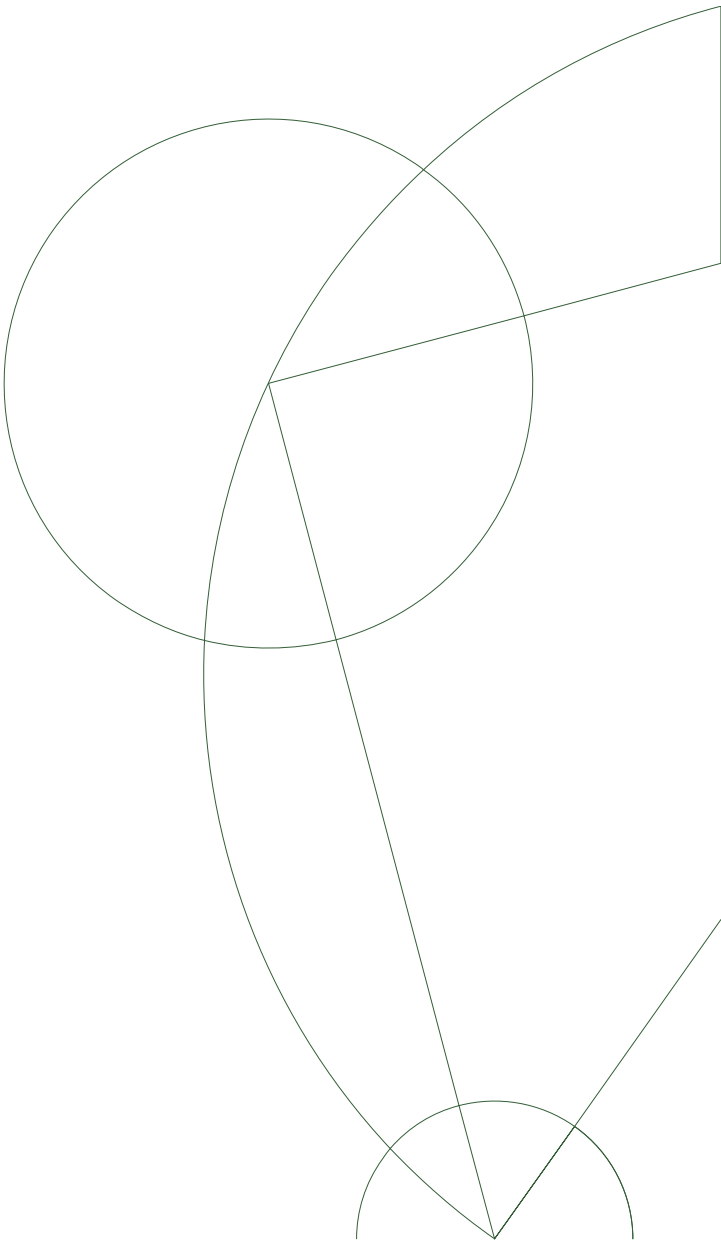
Towards formal verification of FDR4

Department of Computer Science



Professor Brian Vinter

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Abstract

Bla bla bla bla

Contents

Todo list

Chapter 1

Introduction

When we create programs, we wish to verify that it is also correct. There are several ways to do this, one commenly used is `testing` which require that the programmer creates several different scenarios and its expected output, or that the programmer programs a test-generator to create the scenarios and expected output. This, however, is not adequate for (word for important systens). Therefore it is of high interest to create a verification of the system or program.
Talk about how verification was first created and how it became to be used for concurrent systems. Then write about how it works and then write about the different systems and formal languages that is used for it.

In this thesis we look at model checking, that is, verifying that a specific property will always hold for a piece of code.

Formal verification is the process of checking whether a program satisfies specific properties. Different methods have evolved, all having different advantages and disadvantages. FDR is sometimes referred to as a model checker however is it actually a refinement checker.

Matematicians tend to reject proofs by exhaustive checking of all cases as being less satisfying than deductive proofs, and with good reason. First, they are not applicable for proving theorems about integers and real numbers, which are infinite domains so that the number of interpretations is infinite and they cannot be exhaustively checked. Second, they offer no insight into why a theorem is true. But computer scientists have more practical concerns. If they can check all computations of a program and show that they all satisfy a correctness property, we will be willing to forego elegance and be more than satisfied that our program has been proven correct. (from "A primer on model checking af Ben-Ari [7]

1.1 Motivation

Intels-division bug
Toyota bremse-fejl
Adriane 5 haeldning
Terac-25

1.2 Learning goals

This is where the learning goals go.

Chapter 2

Related work

The concepts of formal verification was first expressed in 1954 when Martin Davis created the first computer generated mathematical proof that the product of two even numbers is even. First-order theorem provers were applied to verification problems in Pascal, Ada and Java, in the late 1960s. At Stanford, in 1972, Sir Robin Milner had success building the original LCF system for proof checking. His work in automated reasoning have been the foundation for a lot of other theorem provers, like the proof assistant HOL (Higher Order Logic) by Mike Gordon, which was originally developed for reasoning about hardware. The formal proof management system Coq is a descendent of LCF.
Also in 1972, Robert S. Boyer and J. Strother Moore was successful in building a machine-based prover, called Nqthm which became the basis for ACL2 which is a programming language and a theorem prover. Theorem provers have proved very valuable over the time, but one problem with them was, that if they found a problem in a theorem, they could not tell why it could not prove the theorem. It was not possible to create a counter example or any other explanation as to why it was not possible to prove this theorem.

In 1967, when Robert W. Floyd was published with the paper *Assigning meaning to programs*[12]. Floyd provided a basis for the formal definitions of the meaning of programs which can be used for proving correctness, equivalence and termination. By using flowcharts, he argued that when a command is reached, all previous commands will have been true as well.
C.A.R Hoare was inspired by Floyd and in 1969 his paper *An axiomtic basis for computer programming*[15] was published. The logic he presented there (later known as *Hoare logic*), was build on Floyd's ideas and proposed the notation *Partial correctness specification*; $\{P\}C\{Q\}$. Here, C is a command and P and Q are conditions on the program variables in C. Hoare showed that whenever C is executed in a state that satisfies the condition P, and if the execution terminates, then the state that C terminates in, will satisfy Q. Hoares logic have been the basis of a lot of different formal languages and have contributed to the continuous work on formal verification.
Since the original Hoares logic was not originially thought as to model concurrent programs, L. Lamport extended Hoare's logic in his paper *The 'Hoare logic' of concurrent programs*[22] in 1980. Here, he discuss why Hoare's logic, as proposed by C.A.R Hoare, does not work for concurrent programs and proposes

a "generalized Hoare's logic" that takes concurrency into account.

In 1978 Hoares paper *Communicating Sequential Processes* was published and with it, CSP was born. It have been widely used in many different types of work and have also been expanded since Hoare initially described it in 1978[1]. The first version of CSP was a simple language but in 1984, Brookes, Hoare and Roscoe published their continued work on CSP with the paper *A Theory of Communicating Sequential Processes*[9], and created the modern process algebra it is today. Only a few minor changes have been made to CSP since then, and they are described in Roscoe's *The Theory and Practice of Concurrency*[30].
A number of tools have been created in order to analyse, verify and understand systems written in CSP. Since CSP was mostly a blackboard language and difficult to use on larger scale, different types of machine-readble CSP syntaxes have been created over the years in order to make it easier to use CSP on a larger scale. Most of todays CSP tools use a version of machine-readble CSP called CSP_Mwhich was created by Scattergood[31]. Scattergood created a combination of the standard CSP and a functional programming language which created a better baseline for tools to work with CSP.
Here is a subset of the different CSP tools:

- One of the most known CSP tool is the Failure-Divergence Refinement (FDR), build by Formal Systems (Europe) Ltd., which is currently at version 4.2.3[34]. FDR is a refinement checker and the newer version of FDR is able to run in parallel as well as do state compression in order to avoid a very large state space. FDR only work on finite-state processes.
- ProBE (Process Behaviour Explorer)[25] is a tool to animate CSP in order to explore the state space of CSP processes. It can handle infinite state and is based on the same CSP_Mversion as FDR is. ProBE was also been created by Formal Systems (Europe) Ltd that created FDR and ProBE is integrated into the current version of FDR.
- At Adelaide University, The Adelaide Refinement Checker (ARC)[26] was created. It is a automatic verification tool for CSP that uses Ordered Binary Decision Diagrams (OBDDs) to represent the internal representation of data structures. This lessen the state explosion problem that other model checker tools have had.
- The ProB project[13][24] was originally created as an animation and model checker tool for the B-Method[2] but it also supports other languages like Z and CSP_M. Newer versions of ProB can do refinement checking of CSP_Mscripts but does not have the full functionality that FDR does.
- J. Sun, Y.Liu, J.Dong et al. presented the Process Analysis Toolkit (PAT) in their 2009 paper[33]. PAT is a CSP analysis tool that can perform Linear Temporal Logic (LTL) model checking, refinement checking and simulation of CSP processes.
- CSP-Prover[19] is a theorem prover which works on CSP and based on the theorem prover Isabelle. It is an entirely different way to check programs than model checking. It attempts to prove some general results based on specific theory. It is better at proving general results where model checkers are better at proving combinatorial problems.

The programming language Occam[32], which was first released in 1983, is a concurrent programming language that builds on the CSP process algebra. Occam was continuouly in development during the years and the Kent Retargetable occam Compiler (KRoC) team at Kent University created the Occam-π[35] variant of the Occam programming language. It is a version that extends the ideas of CSP in the original Occam language but adding mobility features from pi-calculus. In the paper *The symbiosis of concurrency and verification: teaching and case studies*[27] Pedersen and Welch uses Occam-π along with CSP$_M$in order to reason about the logic behind CSP$_M$and FDR. By using an executable language like Occam-π which is based on the concurrency model of CSP it becomes easier to understand the logic of CSP$_M$and thereby verify the program with FDR.

SPIN[21] is a verification tool that uses process interactions to prove correctness for a system. The systems are described in the formal language `PROMELA`(PROcess MEta LAnguage)[16] and the correctness properties are spcified in Linear Temporal Logic (LTL)[28]. In the paper *Reasoning About Infinite Computations*[37], Vardi and Wolper showed that all LTL formulas can be translated into a Büchi automata which SPIN makes use of and thus converting the given LTL into a Büchi automaton. Spin performs verification on concurrent software and does not perform verification on hardware circuits.
Spin was developed at Bell Labs, starting in 1980. Gerard J. Holzmann gives an introduction to the theoretical foundations, the design and structure and examples of applications in the paper *The model checker SPIN*[17]. SPIN, as well as other model checker tools, has been build on the pioneering work on logic model checking by Clarke and Emerson[11], as well as Sifakis and Queille[29]. Vardi and Wolper extended their work with an automata-theoretic approach to automatically verify programs[36].

Another verification tool was developed as a collaboration between the Department of Information Technology at Uppsala University (UPP) in Sweden and the Department of Computer Science at Aalborg University (AAL) in Denmark. Larsen et al. first proposed the ideas for UPPAAL[23] in 1995 and further introduced it in the paper *UPPAAL - a Tool Suite for Automatic Verifcation of Real-Time Systems*[8]. UPPAAL is a verification tool for modelling, simulating and verifying real-time systems. It is based on the theory of timed automata[18][5] and typical systems to gain advantage of UPPAAL are systems where timing aspects are critical that communicate through channels or shared variables. As other model checkers, UPPAAL have a modelling language, wherein the system is specified, and a query language that is used to specify the properties to check against the system. The query language is a subset of CTL (computational tree logic) that work for real-time systems[14] [23]. The model checking is done by checking the state-space by making a reachability analysis. The current version of UPPAAL is called UPPAAL2K and was first released in 1999[6].

In 1981, Edmund M. Clarke and E. Allen Emerson managed to combine temporal logic with the state-space exploration in order to provide the first automated model checking algorithm[11]. It was capable of proving properties of programs as well as producing counter examples. In the mid 1980s it was shown how model checking could be applied to hardware verification. However, it quickly

became clear that model checking on hardware was very limited due to the state-space explosion that occurs especially on hardware.
Randall Bryant from the CMU electrical engineering department invented ordered Binary decision diagrams (OBDDs). Later on, J. Burch, E. Clarke, K. McMillan et al.[10] used OBDDs and created *symbolic model checking* which represents the state space symbolically. The symbolic model checking can verify systems with an extremely large number of states and thus creating a solution to the problems of state space explosion.
Because of the state-space explosion problem and the increasing complexity of digital electronic circuits, there was a need to be able to model the timing and data flow of a ciruit with a certain amount of abstraction. This became Hardware Description Languages (HDL)

The VHSIC Hardware Description Language VHDL was initially ordered by the United States Department of Defence in 1981 to help with the growing problem of hardware life cycles.

VHDL: (VHSIC - Very High Speed Integrated Circuit) HDL Initially sponsored by DoD as a hardware documentation standard in early 80s Transformed to IEEE and ratified it as IEEE standard 1176 in 19887 (Known as VHDL-87) Major modification in 93 (Known as VHDL-93) Continuously revised It is based on the Ada programming language.

Verilog: Introduced by Gateway Design Automation in 1985. Cadence Design Systems got the rights to Verilog-XL, the HDL simulator that would become the de-facto standard og Verilog simulator. Due to a request from the U.S Department of Defence, the development of VHDL came to be.

However, VHDL and Verilog share many of the same limitations: neither is suitable for analog or mixed-signal circuit simulation; neither possesses language constructs to describe recursively-generated logic structures. Specialized HDLs (such as Confluence) were introduced with the explicit goal of fixing specific limitations of Verilog and VHDL, though none were ever intended to replace them. (From WIKI) (From WIKI): Essential to HDL design is the ability to simulate HDL programs. Simulation allows an HDL description of a design (called a model) to pass design verification, an important milestone that validates the design's intended function (specification) against the code implementation in the HDL description. It also permits architectural exploration. The engineer can experiment with design choices by writing multiple variations of a base design, then comparing their behaviour in simulation. Thus, simulation is critical for successful HDL design.

Look at functional verification

Look at Property Specification Language also look at SVA (two property languages that are derived from LTL) (used for Hardware)

HDL include explicit notation for expressing concurrency as well as a notion of time. HDLs are used to write executable specifications for hardware. Because HDLs can be executed it gives the illusion of programming languages even though it is more of a specification language or modelling language. First HDLs in late 60's. C.Gordon Bell and Allan Newells text "Computer Structures" in 1971 - first to give a hdl with lasting effect.

(from http://www.techdesignforums.com/practice/guides/formal-verification-guide/) "Equivalence checking has been used for more than a decade to check that RTL and gate-level descriptions of a design represent the same design"

Take a look at Temporal logic model checking (As it is mentioned in the

formal verification - evolution article) - Clarke et. al. CMU 1981 - Sifakis et. al. Grenoble 1982 and also look at Symbolic model checking McMillan 1991 SMV

WRIGHT[4][3] is an architecture description language which was developed at Carnegie Mellon University. They can auto generate CSP$_M$ code from WRIGHT and from there they can confirm certain properties by using FDR. http://www.cs.cmu.edu/ able/wright/

Both theorem provers and model checkers have been, and are still, widely used for both software and hardware. There is a third form of formal verification that is also being used more often now. This is equivalence checking, which compares two models of a design and produces an outcome that either shows that they are equal or provides a counter-example to show when they disagree. It is beginning to become common practice for hardware designers to use equvalence checking to compare the design of an optimized digital design and an unoptimized digital design. This way it is possible for the designer to check that the optimizations did not change the functionality of the design.

Mark B. Josephs shows in his paper *Gate-level modelling and verification of asyncronous circuits using CSP$_M$ and FDR*[20] how to model circuits using CSP$_M$ and also verify its correctness properties with FDR. By using small examples he shows how to check for receptiveness, how to modle delay-insensitivity, how to model gates, n-way mutual exclusion and alternation in delay-insensitive signalling. All this is written in CSP$_M$ and afterwards verified with FDR.

It would be worth to read more about this! They have done a bit of the same that I am to do in my thesis with auto generating CSP$_M$

Chapter 3

Theory

This is where the theory go. fx. SME and the correlation between that and CSP. CSPm was devised by Bryan Scattergood as a machine-readable dialect of CSP - se the paper *The Semantics and Implementation of Machine-Readable CSP*

" FDR2 is often described as a model checker, but is technically a refinement checker, in that it converts two CSP process expressions into Labelled Transition Systems (LTSs), and then determines whether one of the processes is a refinement of the other within some specified semantic model (traces, failures, or failures/divergence)" (from Wikipedia - se paper *Model-checking CSP - af Roscoe*

3.1 CSP

3.2 FDR

3.3 SME

3.4 SMEIL

Chapter 4

Method

This is the method section that describes what I did, how and why.

The first step in translating from SMEIL to CSP$_M$is to create a small example and do a manual translation. This ensures that we have a suitable example to test the automatic gode generation with, but also gives a good understanding of how the translation should be created and what kind of challenges there will arise from translating from SMEIL to CSP$_M$. The example *Seven segment example* is an example of modelling a digital clock which can show hour, minutes and seconds. It consists of 6 different 7-segment displays, which is a display device for displaying decimal numbers. In one 7-segment displays there are 7 identical segments which can be lit in different combinations in order to show the Arabic numbers 0 to 9. This example tries to model a circuit that receives an input in the form ”seconds after midnight” and from this, calculate and display the correct hours, minutes and seconds on the displays. Since only one digit can be shown on each 7-segment display it also needs to separate the actual number e.g if the hour is 12 it will be shown as 1 and 2 on two separate displays.
The SME example is shown in figure inputs a number from a source process that is incremented with one for each run. It then sends the input out on the output bus where three different calculating processes read from. Each process calculates respectively hours, minutes and seconds and divide the number in order to output two numbers to the output channels. Each calculating process outputs to two different output channels.

Put example code in

The code in `seven_segment_example.csp` is the handmade translation from the SME file. In order to create a proper input range for CSP$_M$we use the range created by the SMEIL simulator. The range is created based on all observed numbers and since the source process in SME does not have an input bus we use this process to created the input channel in CSP$_M$. This way we can generalize how to translate the input ranges from SME to CSP$_M$. The translation in CSP$_M$is equivalent to the SME version where each process calculates either the hours, minutes or seconds and divide the result into two digits, one for each output channel.
What we want to check in this example is that a 7 segment display can only represent 0-9 but 4 bits can represent 0-15. So we are interested in figuring out if this model can result in a result that is over 9, in which case, the model needs to be changed. The assertion used in CSP$_M$is to check if the processes refines

the `SKIP` process i.e if the process terminates.

Chapter 5

Results and tests (Experiment?)

Does it work? why, why not

Chapter 6

Discussion

Chapter 7

Conclusion

7.1 Future work

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7.2 Appendix