1 Related work

The concepts of formal verification began in 1967 , when Robert W. Floyd was published with the paper *Assigning meaning to programs*[9]. Floyd provided a basis for the formal definitions of the meaning of programs which can be used for proving correctness, equivalence and termination. By using flowcharts, he argues that when a command is reached, all previous commands will have been true as well.

apparently it did not - but how far back should I go?

C.A.R Hoare was inspired by Floyd and in 1969 his paper *An axiomtic basis for computer programming*[12] was published. The logic he presented there (later known as *Hoare logic*), was build on Floyd's ideas and proposed the notation *Partial correctness specification*; $\{P\}C\{Q\}$. Here, C is a command and P and Q are conditions on the program variables in C. Hoare showed that whenever C is executed in a state that satisfies the condition P, and if the execution terminates, then the state that C terminates in, will satisfy Q. Hoares logic have been the basis of a lot of different formal languages and have contributed to the continuous work on formal verification.

Since the original Hoares logic was not originially thought as to work with concurrent programs, L. Lamport extended Hoare's logic in his paper *The 'Hoare logic' of concurrent programs*[18] in 1980. Here, he discuss why Hoare's logic, as proposed by C.A.R Hoare, does not work for concurrent programs and proposes a "generalized Hoare's logic" that takes concurrency into account.

Maybe add more here about what uses Hoare logic today

In 1978 Hoares paper *Communicating Sequential Processes* was published and with it CSP. It have been widely used in many different works and have also been expanded since Hoare initially described it in 1978. The first version of CSP was mostly a concurrent programming language but in 1984, Brookes, Hoare and Roscoe published their continued work on CSP with the paper *A Theory of Communicating Sequential Processes*[7], and created the modern process algebra it is today. Only a few minor changes have been made to CSP since then, and they are described in Roscoe's *The Theory and Practice of Concurrency*[25]. Now, several different variations of CSP exists today which all specialize in different areas of formal descriptions.

Figure out if Hoare used this information/update in his work with CSP. I am not sure if CSP work on Hoare logic?

A number of tools have been created in order to analyse, verify and understand systems written in CSP. Since CSP was mostly a blackboard language and difficult to use on larger scale, different types of machine-readble CSP syntaxes have been created over the years in order to make it easier to use CSP on a larger scale. Most of todays CSP tools use a version of machine-readble CSP called CSP_Mwhich was created by Scattergood[26]. Scattergood created a combination of the standard CSP and a functional programming language which created a better baseline for tools to work with CSP. Here is a subset of the different CSP tools:

Citation to Communicating Sequential Processes: The first 25 years

- One of the most known CSP tool is the Failure-Divergence Refinement (FDR), build by Formal Systems (Europe) Ltd., which is currently at version 4.2.3[29]. FDR is a refinement checker which differs from a lot of other CSP tools that are merely model checkers. FDR only work on finite-state processes.
- ProBE (Process Behaviour Explorer)[21] is a tool to animate CSP in order

Is that really how it was - was it a programming language??? :o

to explore the state space of CSP processes. It can handle infinite state and is based on the same CSP_Mversion as FDR is. ProBE was also been created by Formal Systems (Europe) Ltd that created FDR and ProBE is integrated into the current version of FDR.

- At Adelaide University, The Adelaide Refinement Checker (ARC)[22] was created. It is a automatic verification tool for CSP that uses Ordered Binary Decision Diagrams (OBDDs) to represent the internal representation of data structures. This lessen the state explosion problem that other model checker tools have had.

- The ProB project[10][20] was originally created as an animation and model checker tool for the B-Method[1] but it also supports other languages like Z and CSP_M. Newer versions of ProB can do refinement checking of CSP_Mscripts but does not have the full functionality that FDR does.

- J. Sun, Y.Liu, J.Dong et al. presented the Process Analysis Toolkit (PAT) in their 2009 paper[28]. PAT is a CSP analysis tool that can perform Linear Temporal Logic (LTL) model checking, refinement checking and simulation of CSP processes.

- CSP-Prover[16] is a theorem prover which works on CSP and based on the theorem prover Isabelle. It is an entirely different way to check programs than model checking. It attempts to prove some general results based on specific theory. It is better at proving general results where model checkers are better at proving combinatorial problems.

The programming language Occam[27], which was first released in 1983, is a concurrent programming language that builds on the CSP process algebra. Occam was continuouly in development during the years and the Kent Retargetable occam Compiler (KRoC) team at Kent University created the Occam-π[30] variant of the occam programming language. It is a version that extends the idas of CSP in the original occam language but adding mobility features from pi-calculus.

SPIN[17] is a verification tool that uses process interactions to prove correctness for a system. The systems are described in the formal language `PROMELA`(PROcess MEta LAnguage)[13] and the correctness properties are spcified in Linear Temporal Logic (LTL)[23]. In the paper *Reasoning About Infinite Computations*[32], Vardi and Wolper showed that all LTL formulas can be translated into a Büchi automata which SPIN makes use of and thus converting the given LTL into a Büchi automaton. Spin performs verification on concurrent software and does not perform verfication on hardware circuits.
Spin was developed at Bell Labs, starting in 1980. Gerard J. Holzmann gives an introduction to the theoretical foundations, the design and structure and examples of applications in the paper *The model checker SPIN*[14]. SPIN, as well as other model checker tools, has been build on the pioneering work on logic model checking by Clarke and Emerson[8], as well as Sifakis and Queille[24]. Vardi and Wolper extended their work with an automata-theoretic approach to automatically verify programs[31].

Another verification tool was developed as a collaboration between the Department of Information Technology at Uppsala University (UPP) in Sweden and the Department of Computer Science at Aalborg University (AAL) in Denmark. Larsen et al. first proposed the ideas for UPPAAL[19] in 1995 and further introduced it in the paper *UPPAAL - a Tool Suite for Automatic Verifcation of Real-Time Systems*[6]. UPPAAL is a verification tool for modeling, simulating and verifying real-time systems. It is based on the theory of timed automata[15][4] and typical systems to gain advantage of UPPAAL are systems where timing aspects are critical that communicate through channels or shared variables. As other model checkers, UPPAAL have a modelling language, wherein the system is specified, and a query language that is used to specify the properties to check against the system. The query language is a subset of CTL (computational tree logic) that work for real-time systems[11] [19]. The model checking is done by checking the state-space by making a reachability analysis. The current version of UPPAAL is called UPPAAL2K and was first released in 1999[5].

VHDL was initially ordered by the United States Department of Defence in 1981 to help with the growing problem of hardware life cycles.

VHDL: (VHSIC - Very High Speed Integrated Circuit) HDL Initially sponsored by DoD as a hardware documentation standard in early 80s Transformed to IEEE and ratified it as IEEE standard 1176 in 19887 (Known as VHDL-87) Major modification in 93 (Known as VHDL-93) Continuously revised It is based on the Ada programming language.

Verilog: Introduced by Gateway Design Automation in 1985. Cadence Design Systems got the rights to Verilog-XL, the HDL simulator that would become the de-facto standard og Verilog simulator. Due to a request from the U.S Department of Defence, the development of VHDL came to be.

However, VHDL and Verilog share many of the same limitations: neither is suitable for analog or mixed-signal circuit simulation; neither possesses language constructs to describe recursively-generated logic structures. Specialized HDLs (such as Confluence) were introduced with the explicit goal of fixing specific limitations of Verilog and VHDL, though none were ever intended to replace them. (From WIKI) (From WIKI): Essential to HDL design is the ability to simulate HDL programs. Simulation allows an HDL description of a design (called a model) to pass design verification, an important milestone that validates the design's intended function (specification) against the code implementation in the HDL description. It also permits architectural exploration. The engineer can experiment with design choices by writing multiple variations of a base design, then comparing their behavior in simulation. Thus, simulation is critical for successful HDL design.

Look at functional verification

Look at Property Specification Language also look at SVA (two property languages that are derived from LTL) (used for Hardware)

HDL include explicit notation for expressing concurrency as well as a notion of time. HDLs are used to write executable specifications for hardware. Because HDLs can be executed it gives the illusion of programming languages even though it is more of a specification language or modeling language. First HDLs in late 60's. C.Gordon Bell and Allan Newells text "Computer Structures" in 1971 - first to give a hdl with lasting effect.

(from http://www.techdesignforums.com/practice/guides/formal-verification-guide/) "Equivalence checking has been used for more than a decade to check that RTL and gate-level descriptions of a design represent the same design"

Take a look at Temporal logic model checking (As it is mentioned in the formal verification - evolution article) - Clarke et. al. CMU 1981 - Sifakis et. al. Grenoble 1982 and also look at Symbolic model checking McMillan 1991 SMV

WRIGHT[3][2] is an architecture description language which was developed at Carnegie Mellon University. They can auto generate CSP$_M$code from WRIGHT and from there they can confirm certain properties by using FDR. http://www.cs.cmu.edu/ able/wright/

It would be worth to read more about this! They have done a bit of the same that I am to do in my thesis with auto generating CSP$_M$

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