

# Towards Automatic Program Specification Using SME Models

Communicating Process Architectures 2018 – Technische Universität Dresden

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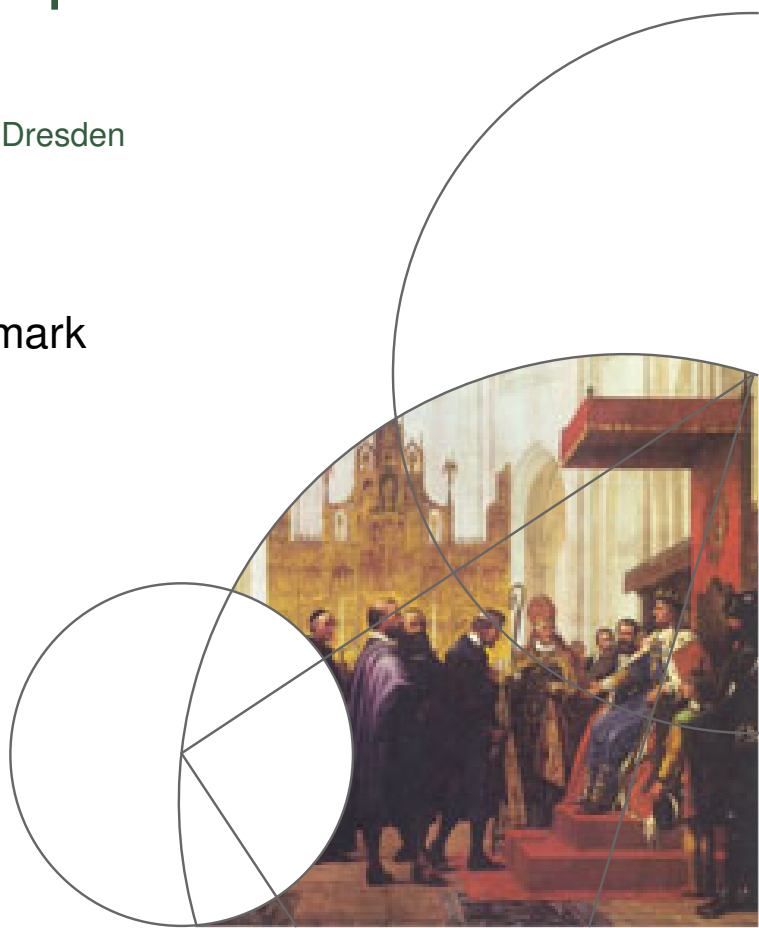

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No people where harmed

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A bug in the system’s weapons control computer caused an inaccurate tracking calculation. Conversion of time since last boot from an integer to a real number was performed using a 24 bit register.

Inaccurate results == missile misses target

# What have we done?

A transpiler which transpiles SMEIL code to $\text{CSP}_M$ in order to verify SME models with FDR4

# SME

The SME model builds on the CSP algebra what more to add?

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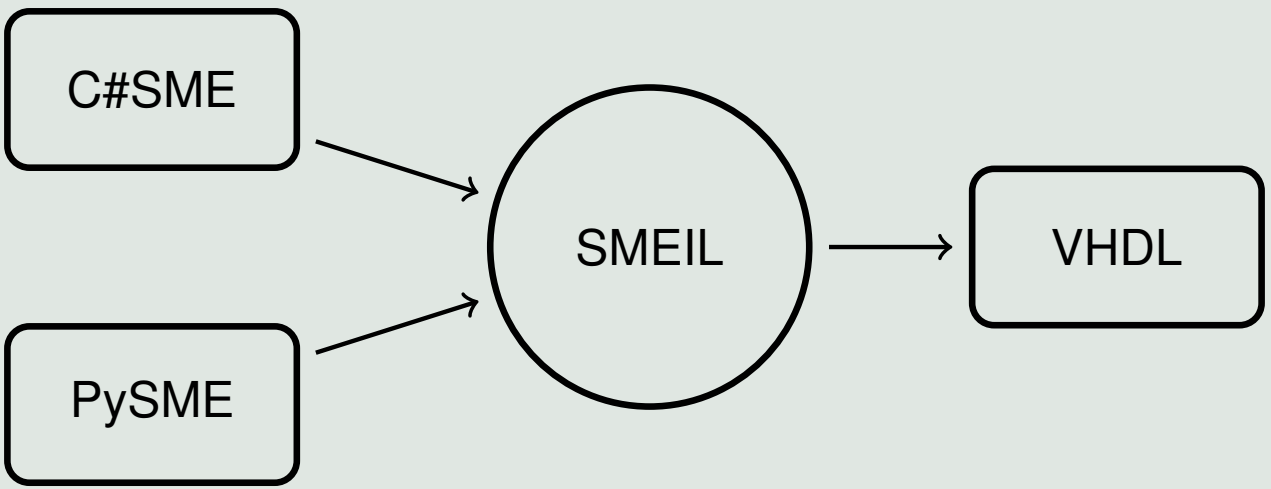


Figure. SMEIL transpiler structure.

# Seven segment display clock

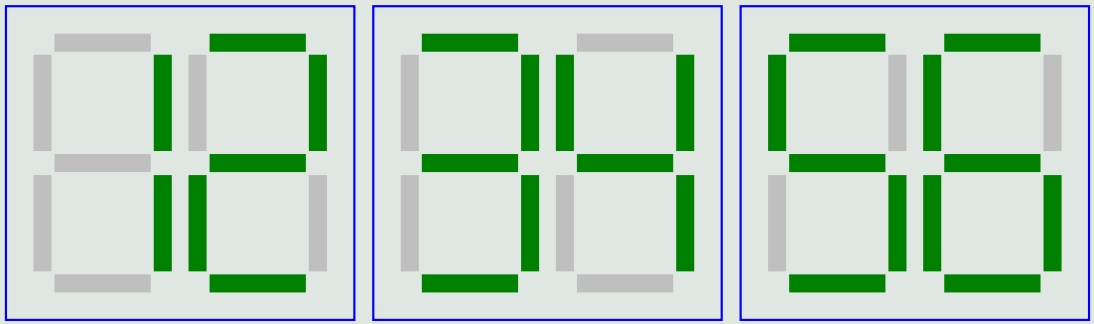

Figure. Digital clock with six seven segment displays, displaying 12:34:56.

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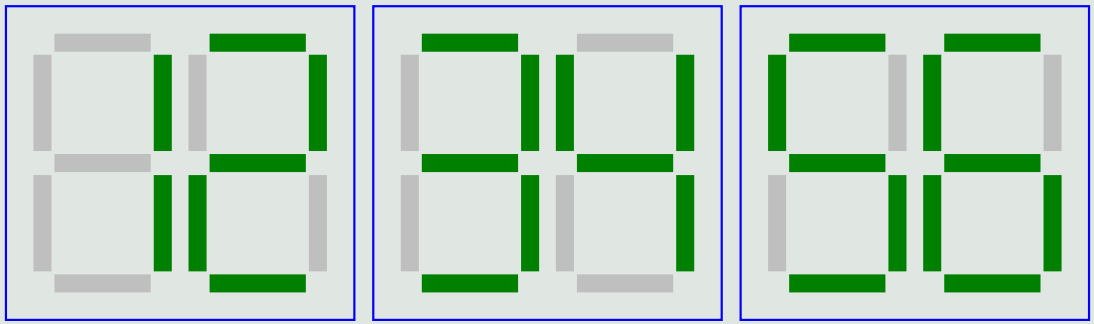

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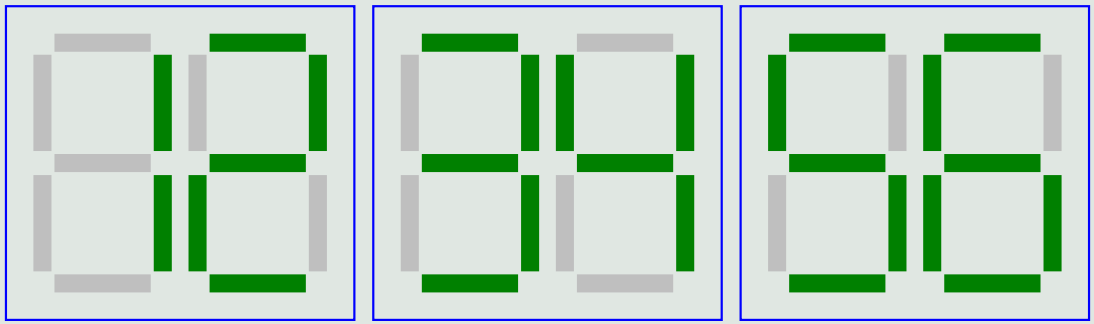

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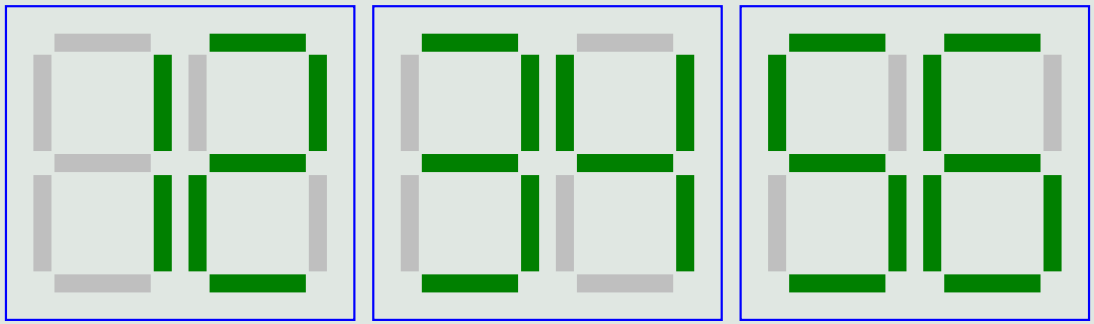

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Two seven segment displays pr. `time` process

# Simple example

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In this case we can restrict the assertions further.
Hours will never be more than 24, etc.

# Simple example

## Seven Segments SMEIL Structure

`SMEIL` code:

# Simple example

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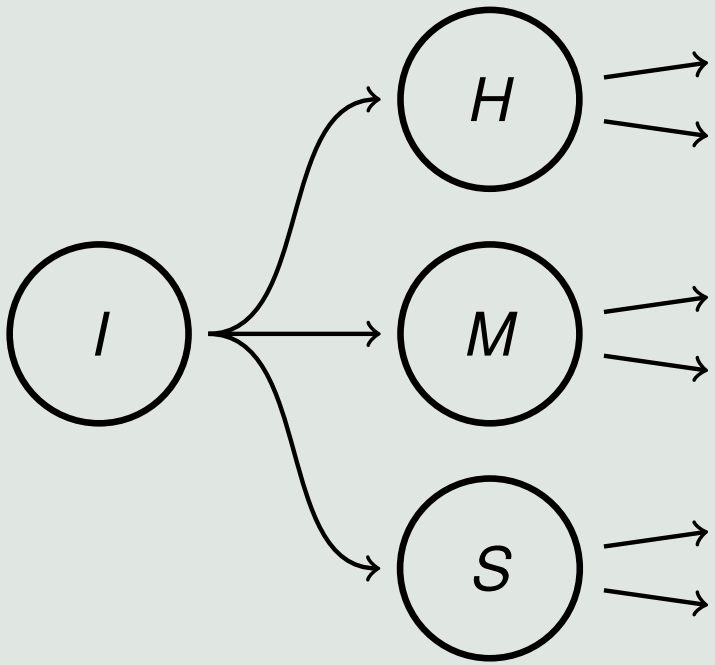


Figure. SMEIL network for a seven segment display clock. Each SMEIL process is represented by a cicle with a letter corresponding to the processes Input, Hours, Minutes and Seconds respectively.

# SMEIL bus to CSP$_M$ channel

Code example

# $CSP_M$ process structure

Code example

# Monitor process

Code example

# Example continued

## $CSP_M$ code

$CSP_M$ code? Do we even need this?

# Results - time to verify in FDR4?

The seven segment example have been run on a Intel(R) Xeon(R) CPU E5-2698 v4 @ 2.20GHz.

The example were run x times and the average was measured. (If I have time)

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and verify values on the $\text{CSP}_M$ channels

and thereby verify the original hardware model

# Future work

## Rest of SMEIL grammar?

+ more?

# Questions?

## Thank you!

Thank you so much for your time.
Feel free to ask anything.