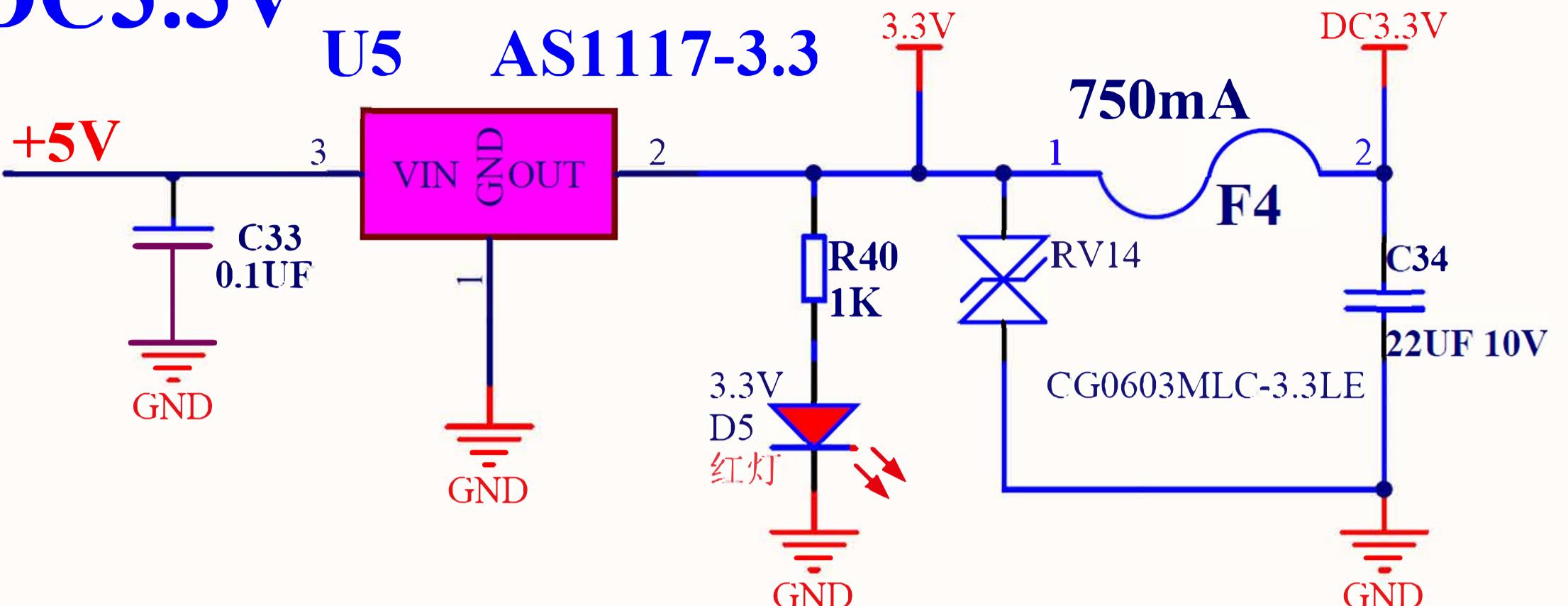
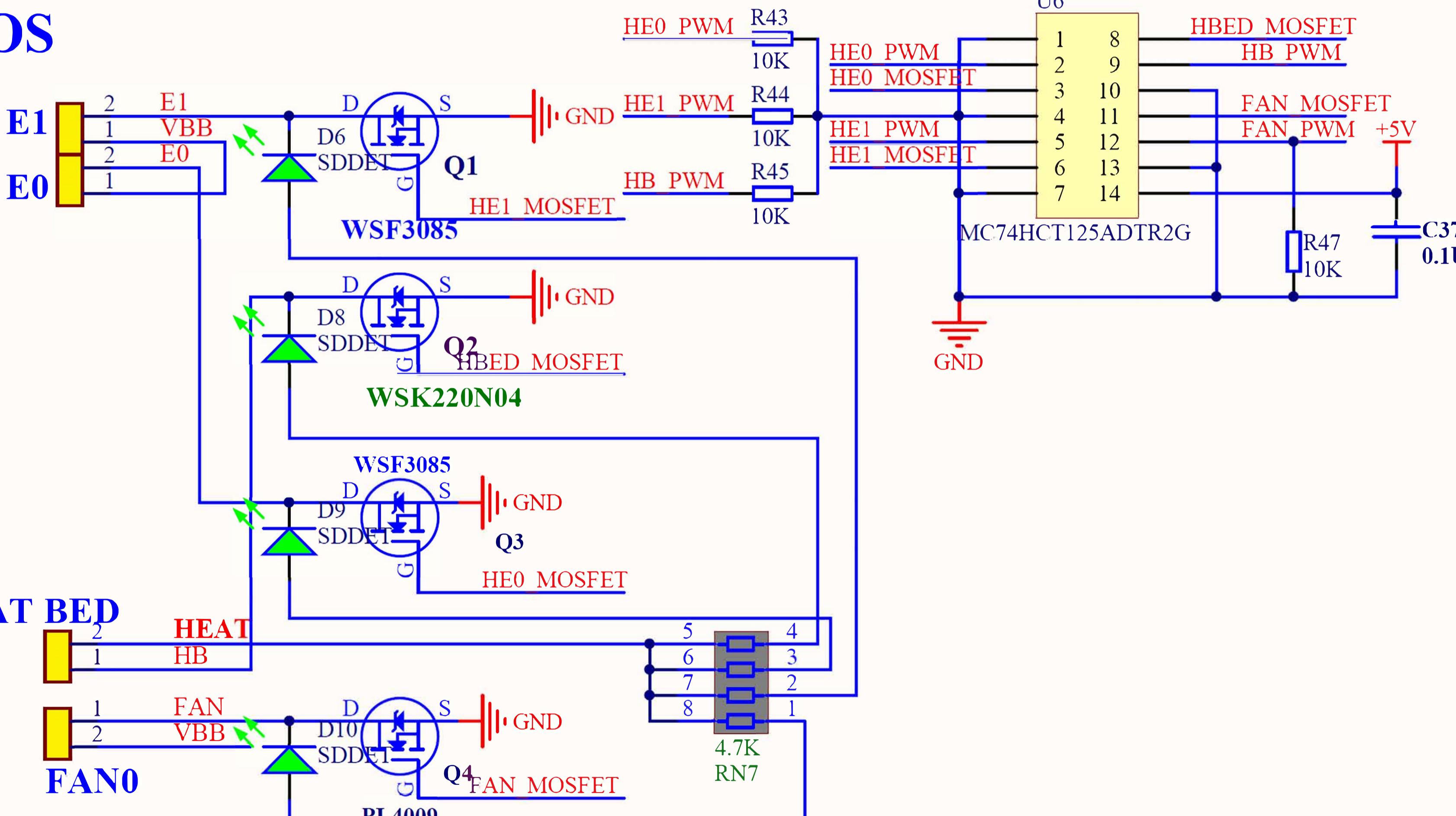


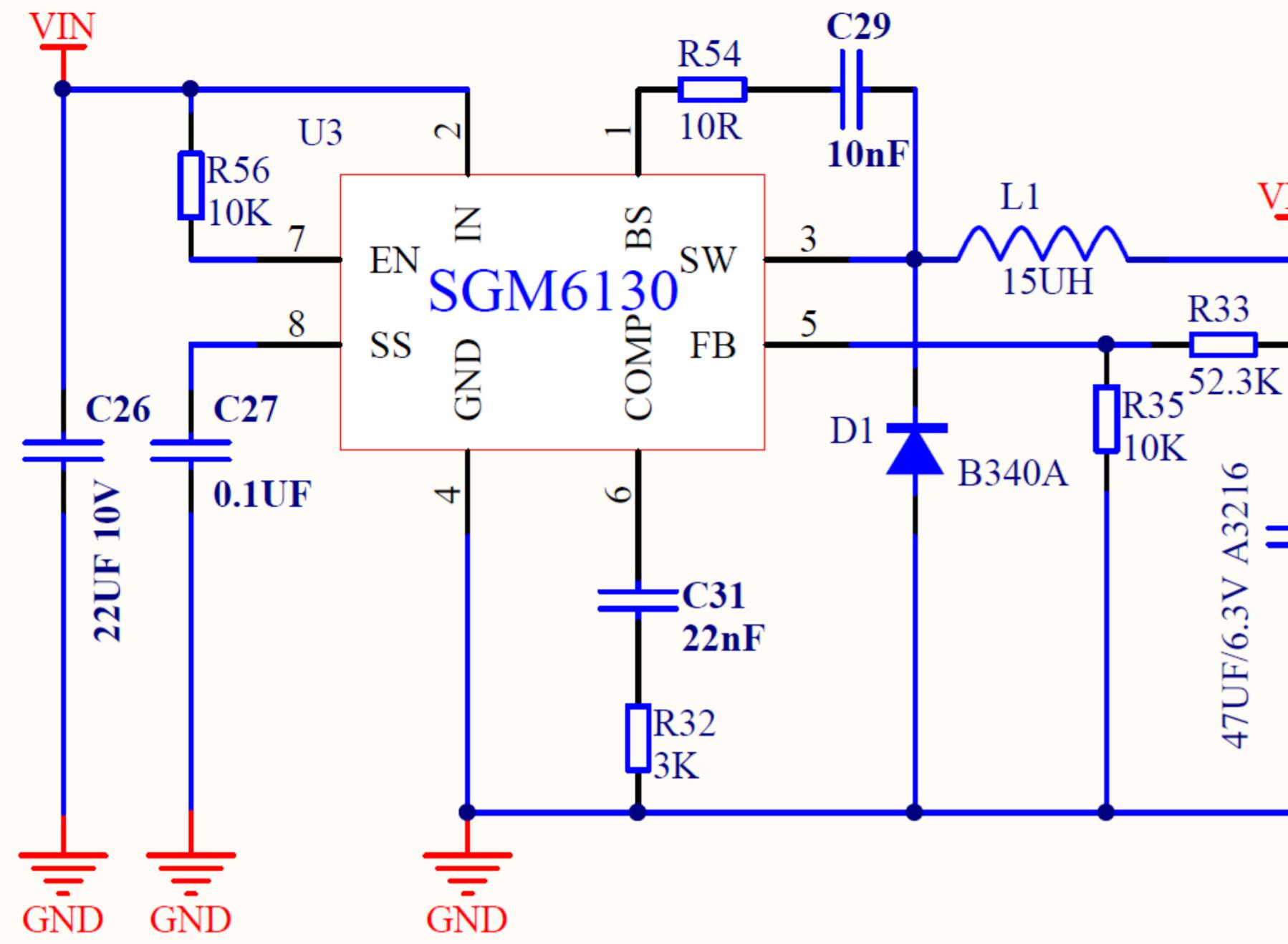
# DCDC3.3V



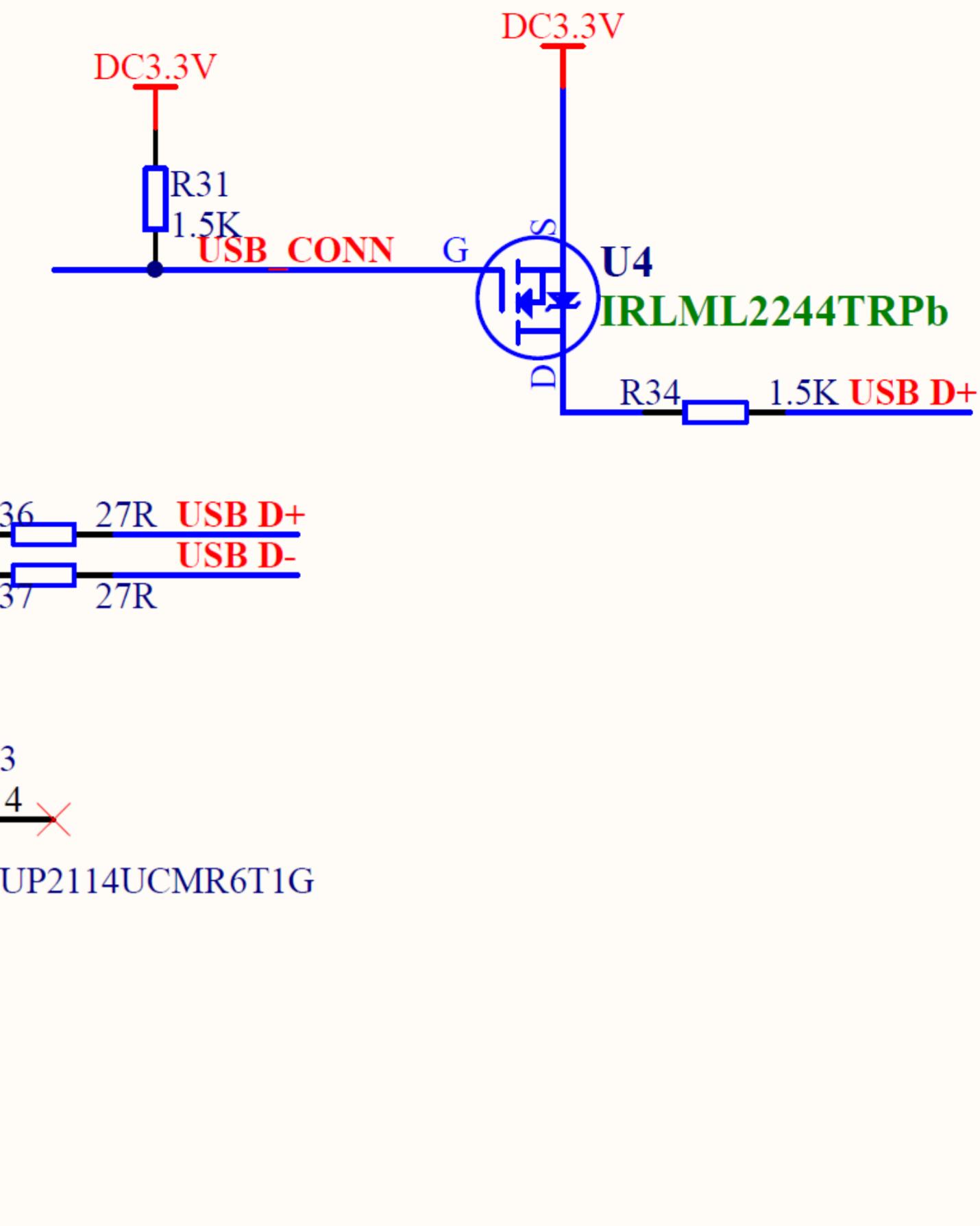
# MOS



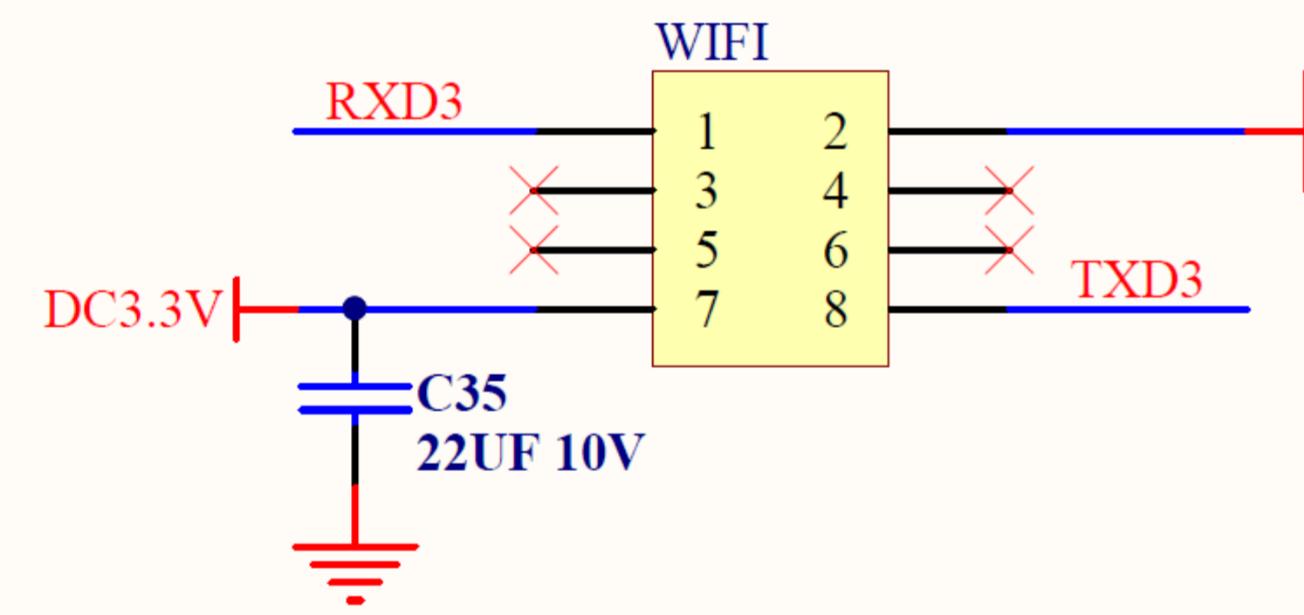
# DCDC5V



USI

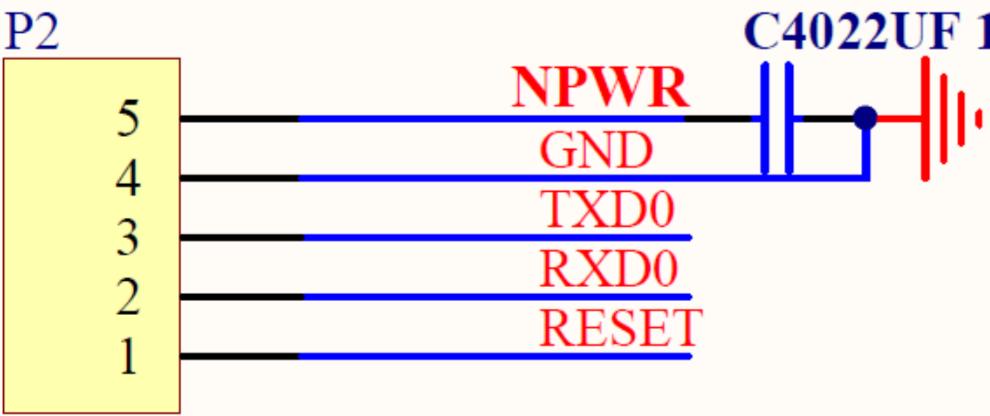


# WIFI

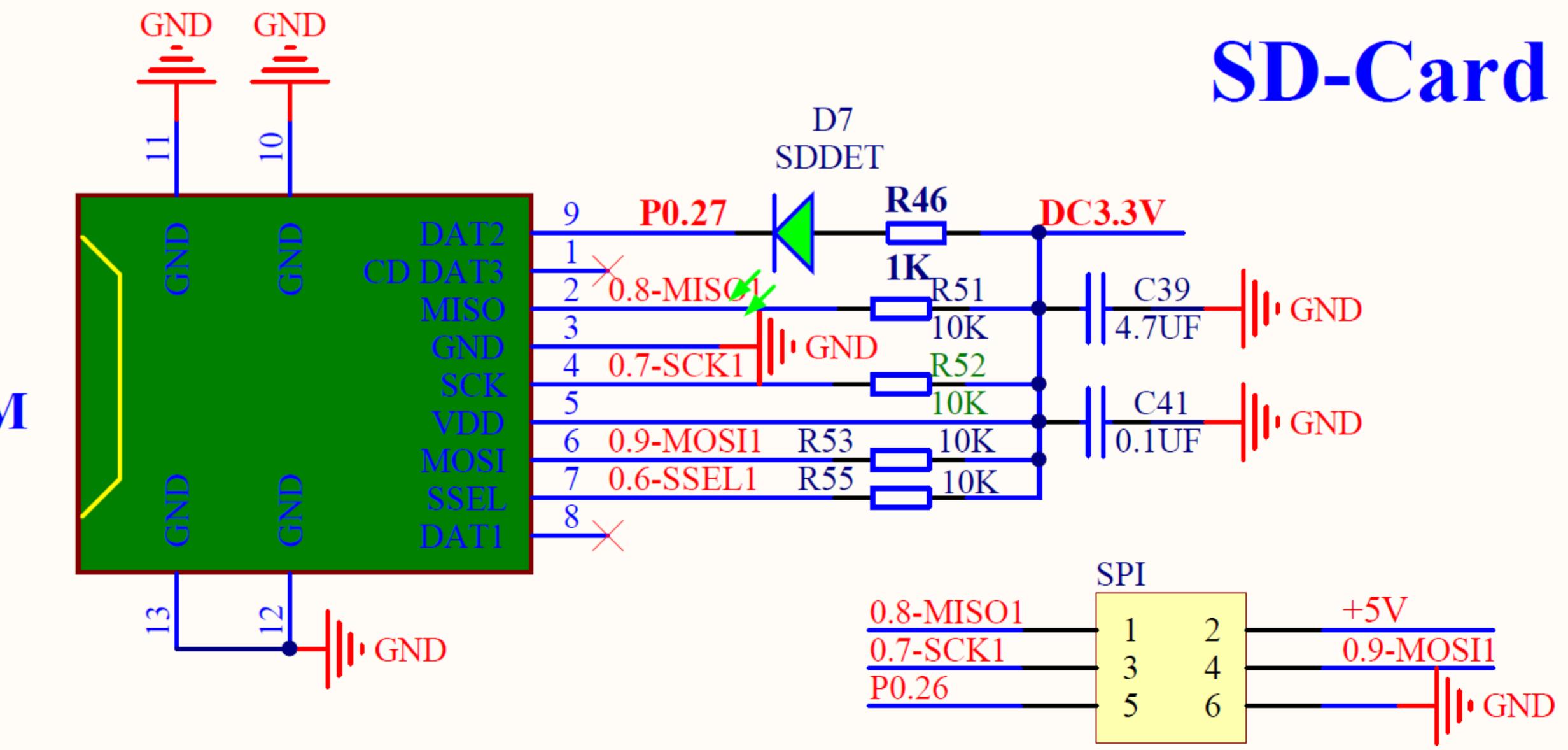


# SD-Card

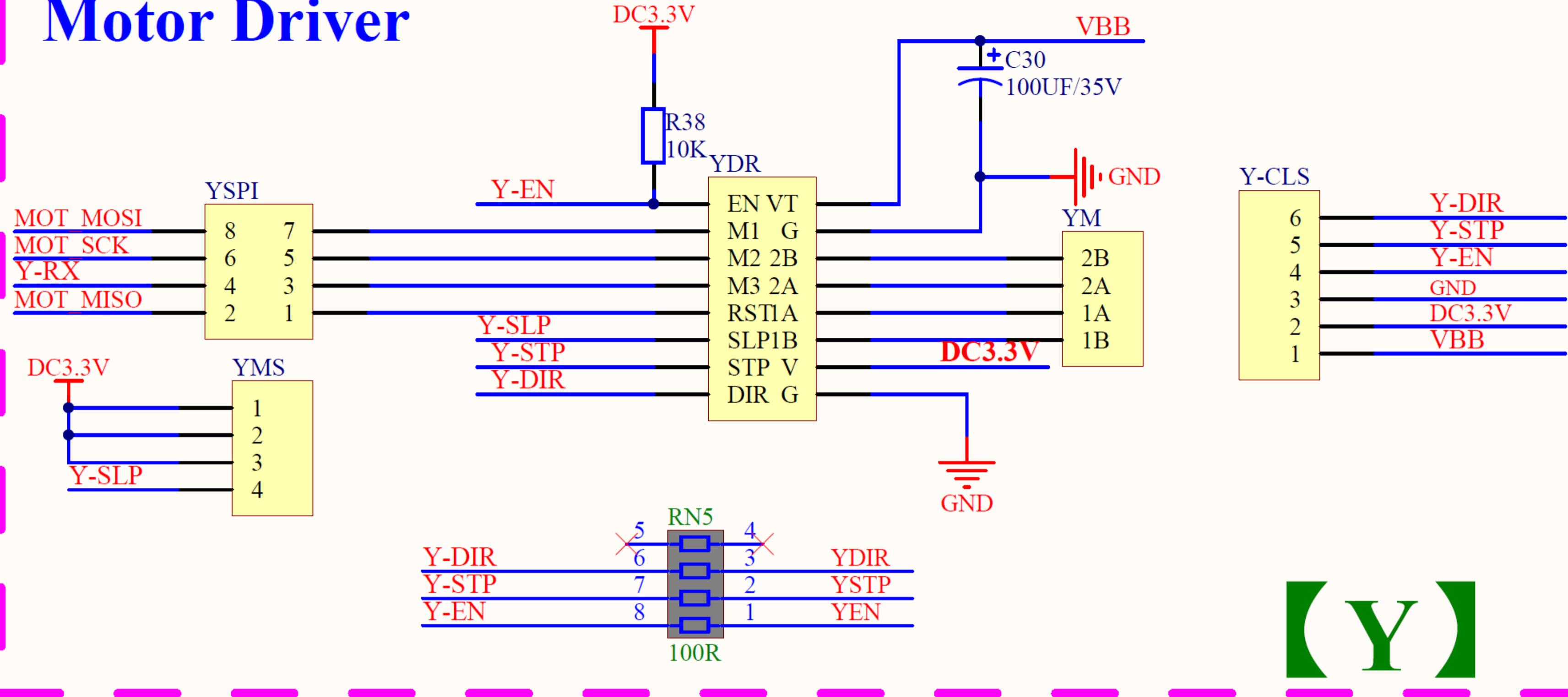
**5V**   **TFT**



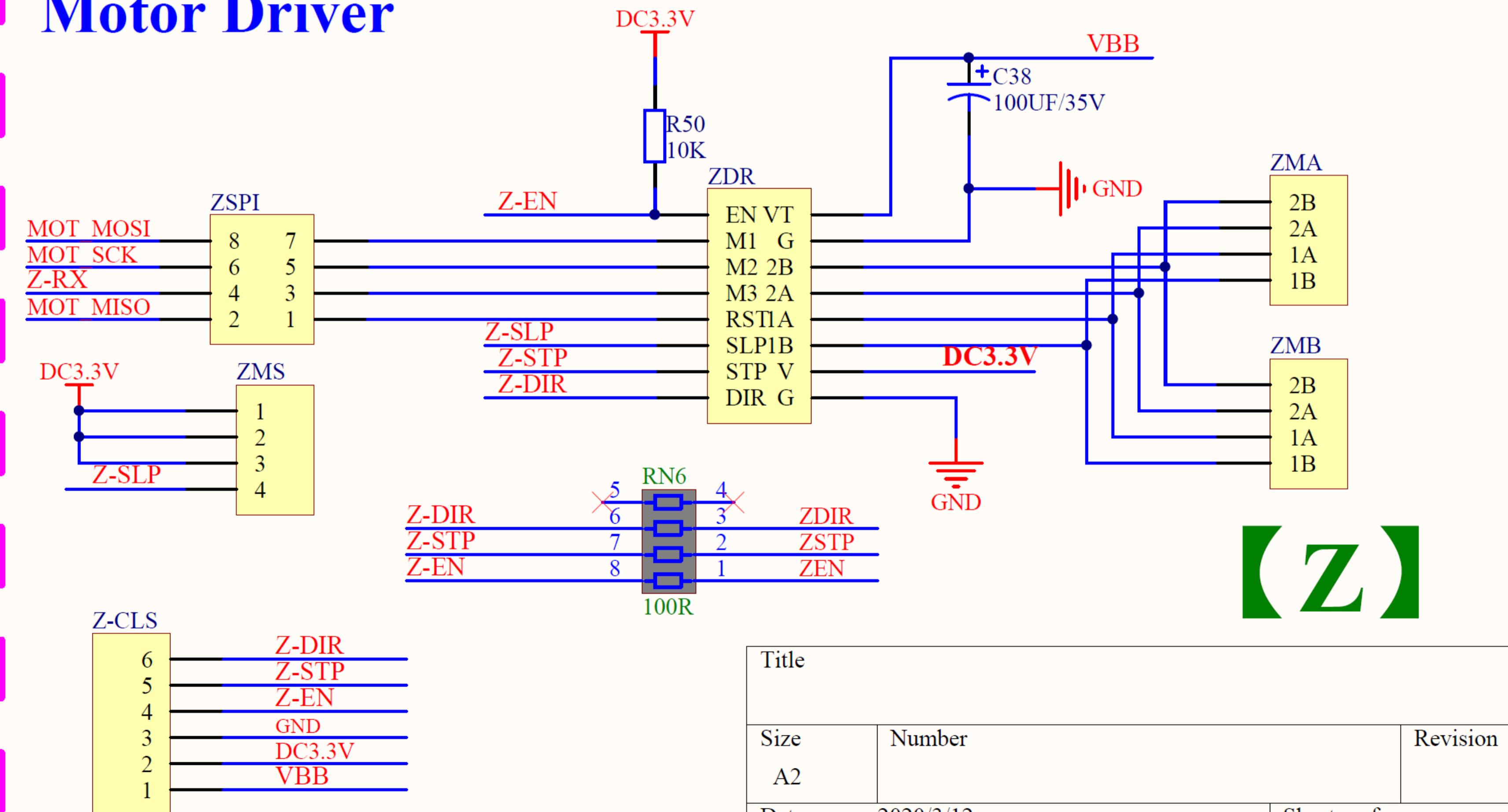
U  
SD



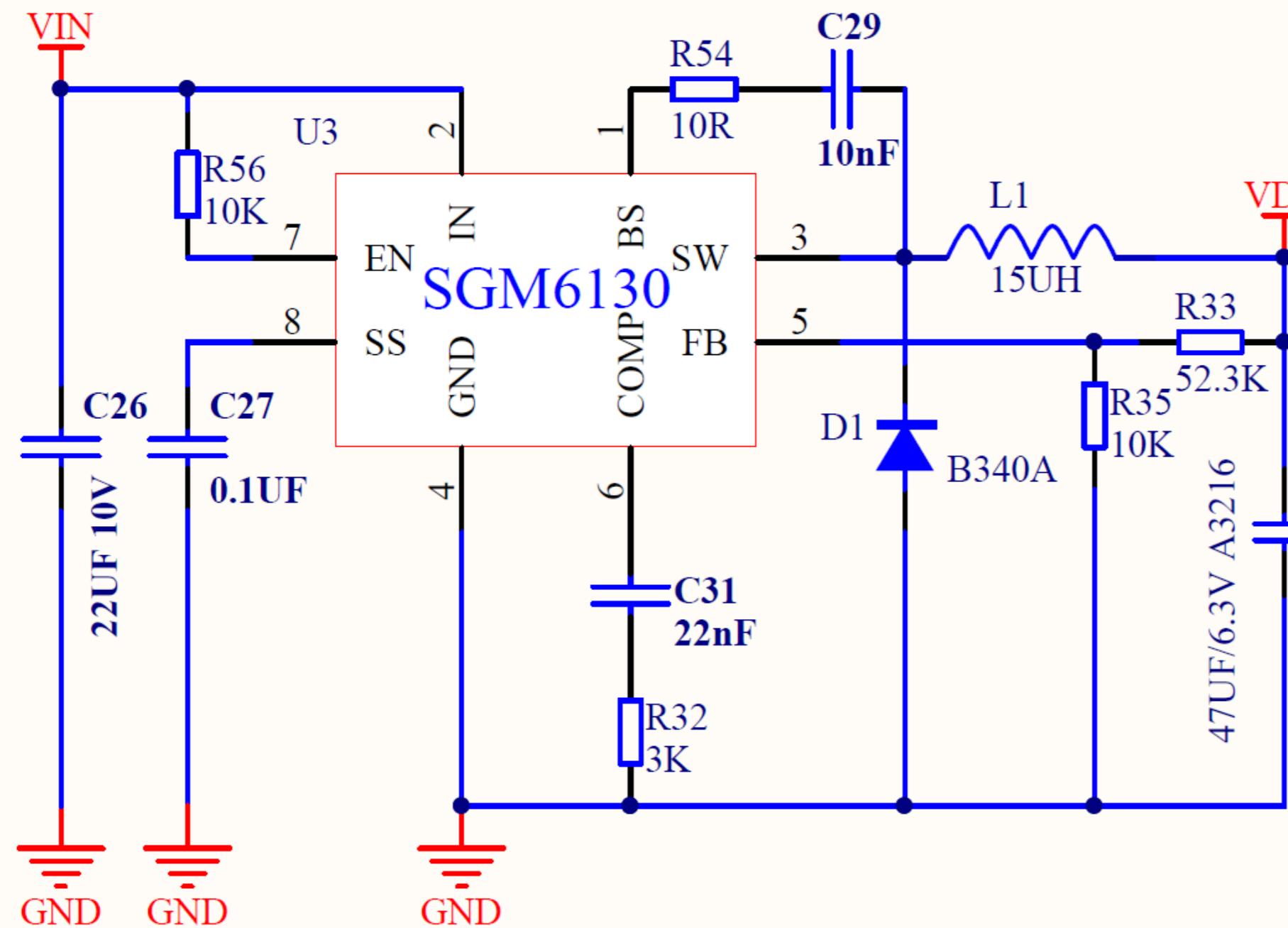
# Motor Driver



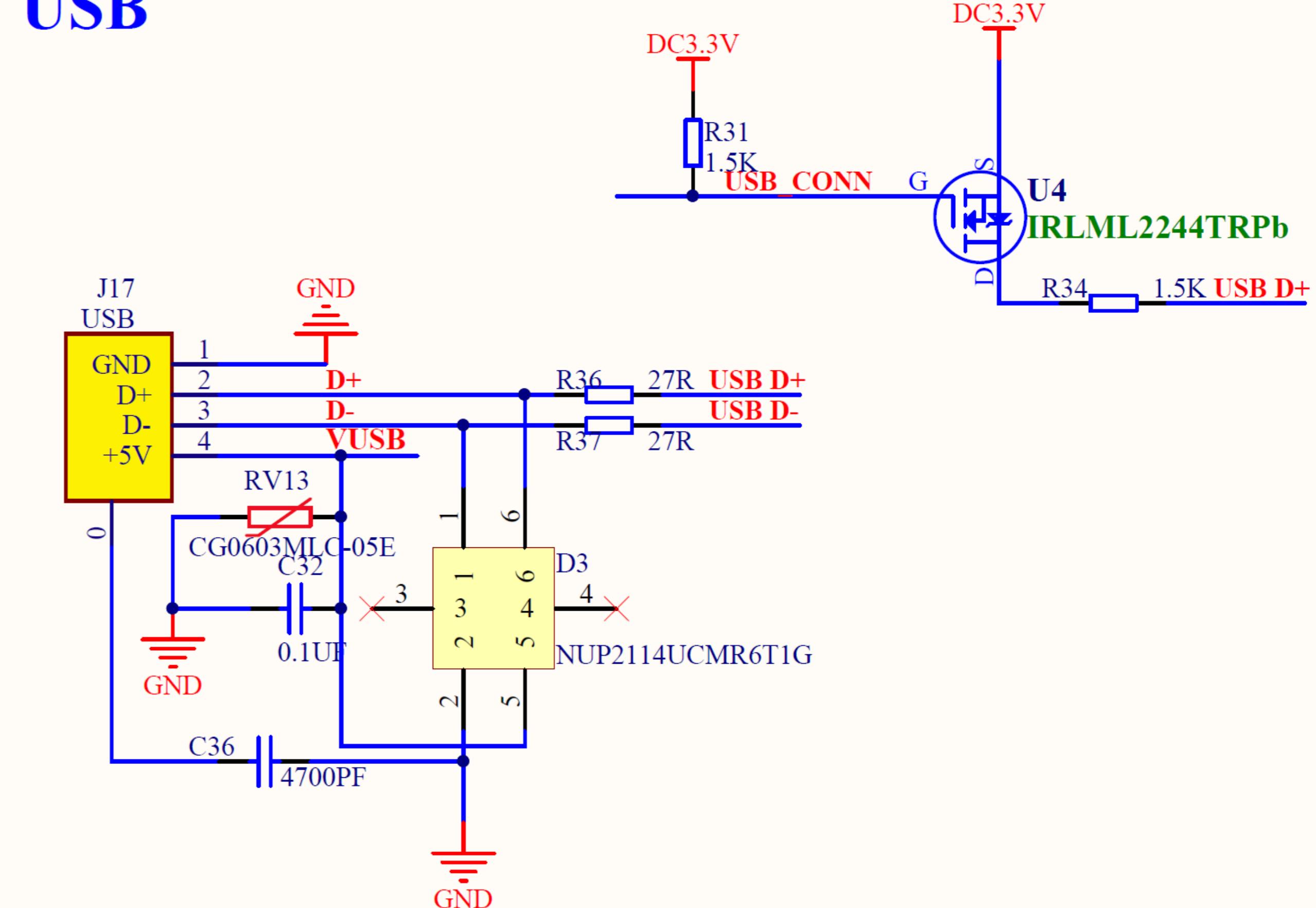
# Motor Driver



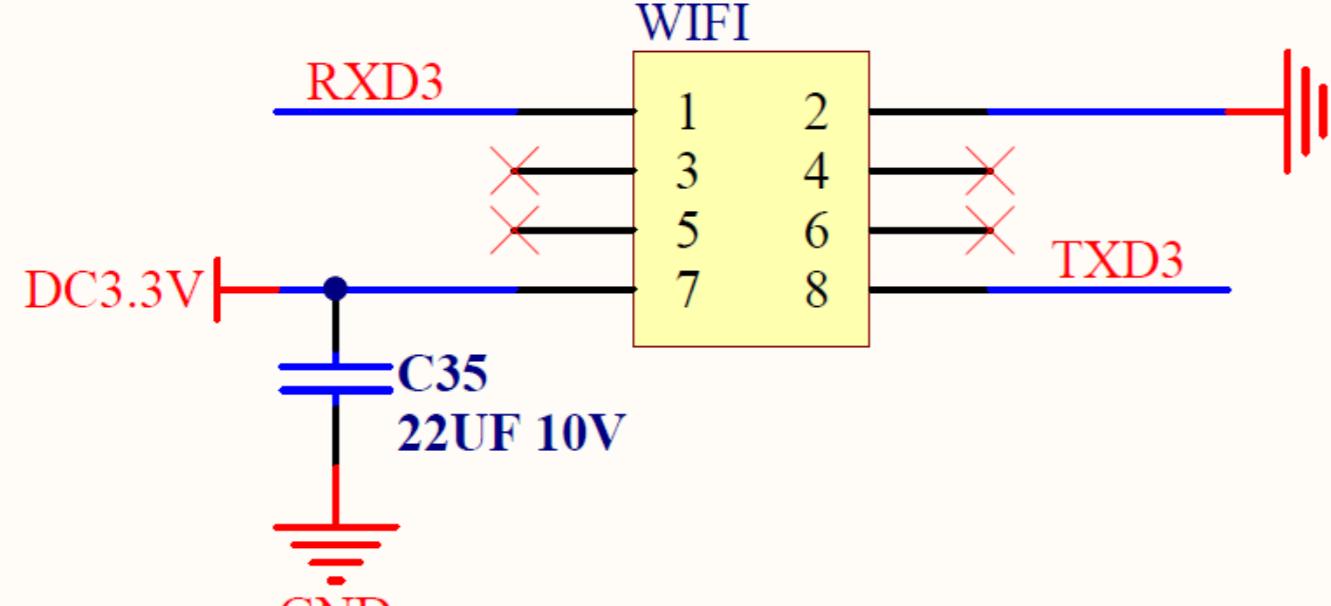
# DCDC5V



# USB

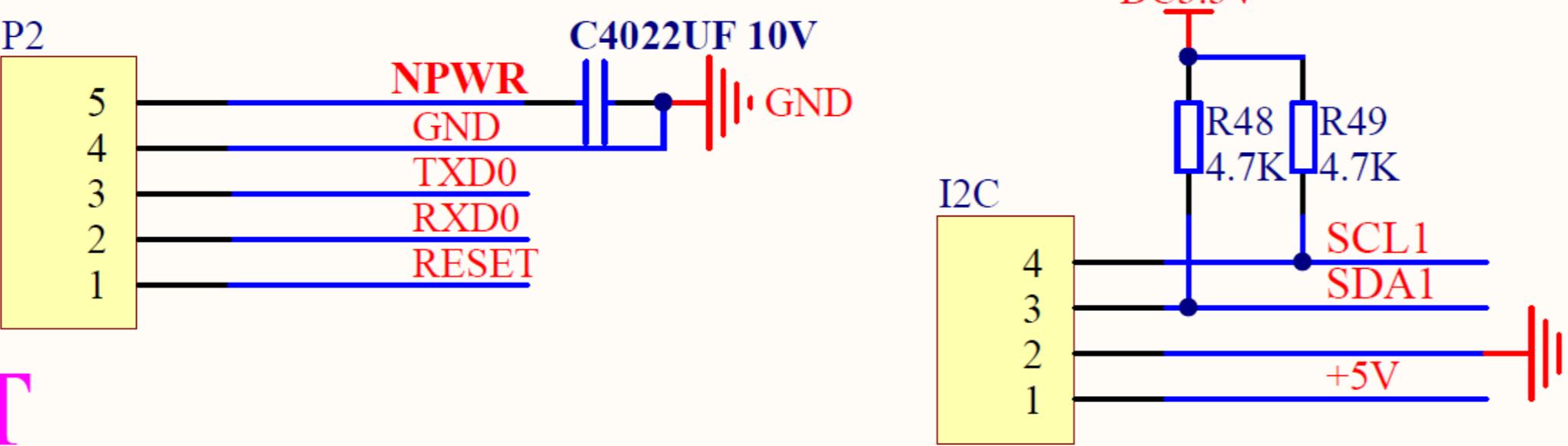


# WIFI



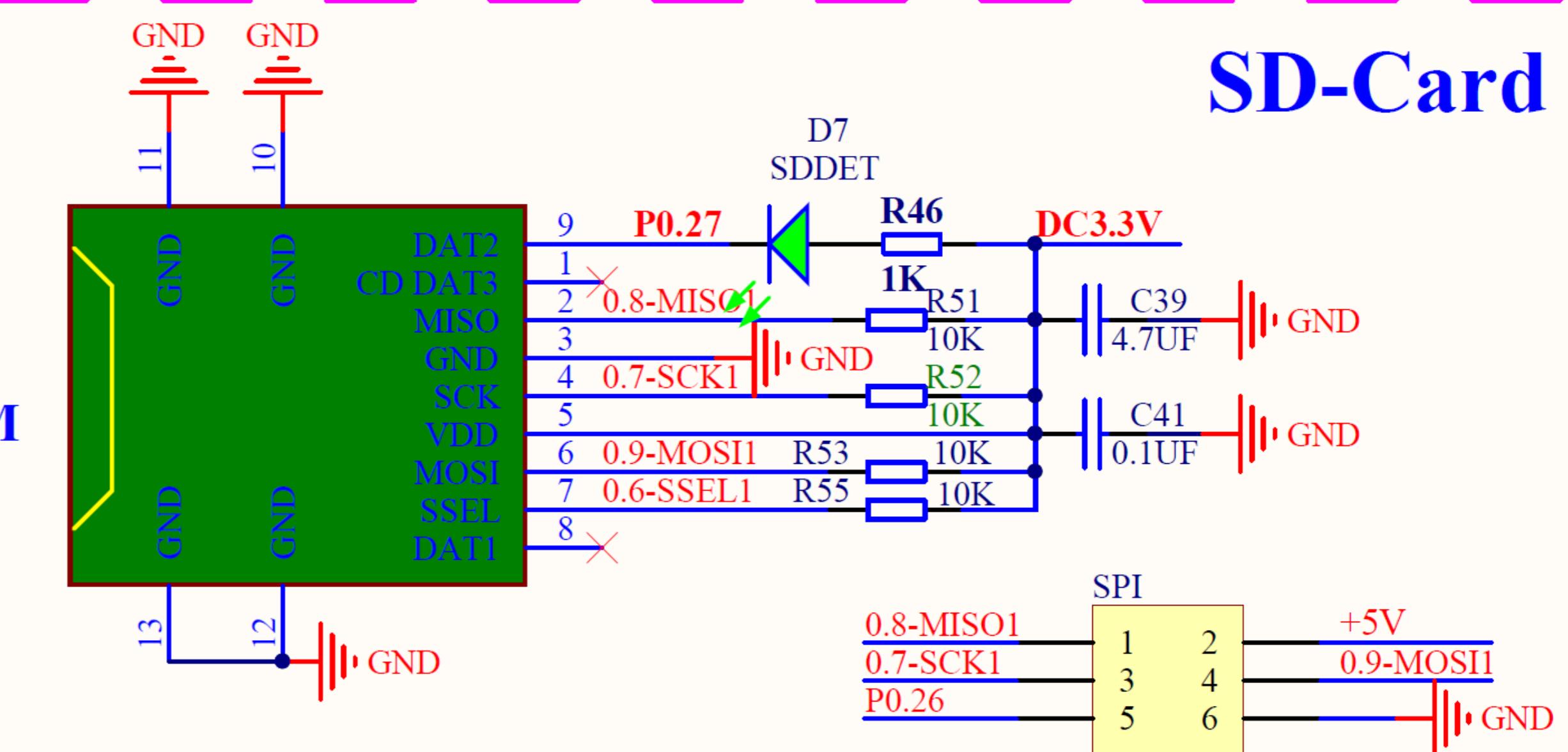
# 5V

# TFT

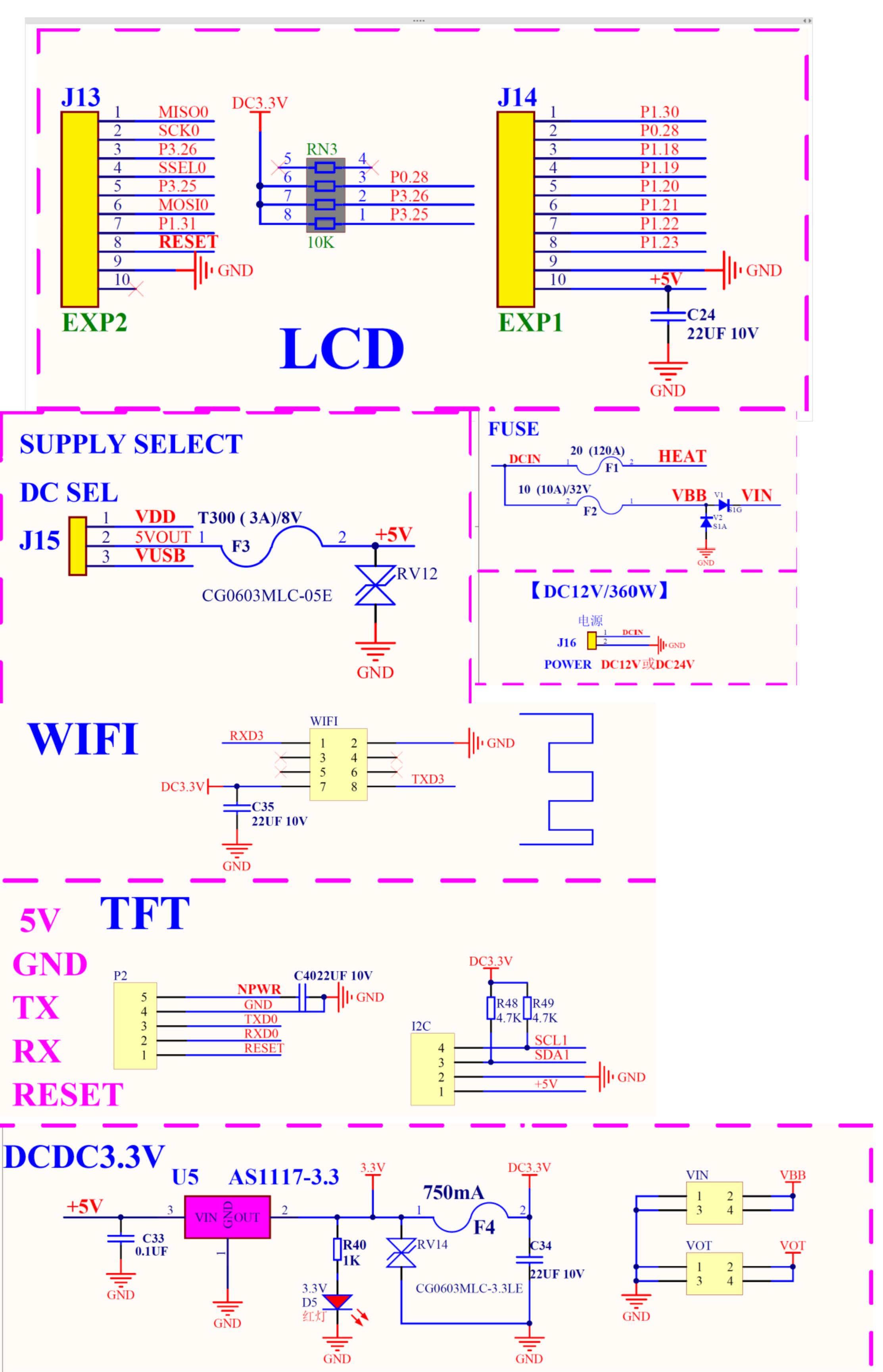


# U7

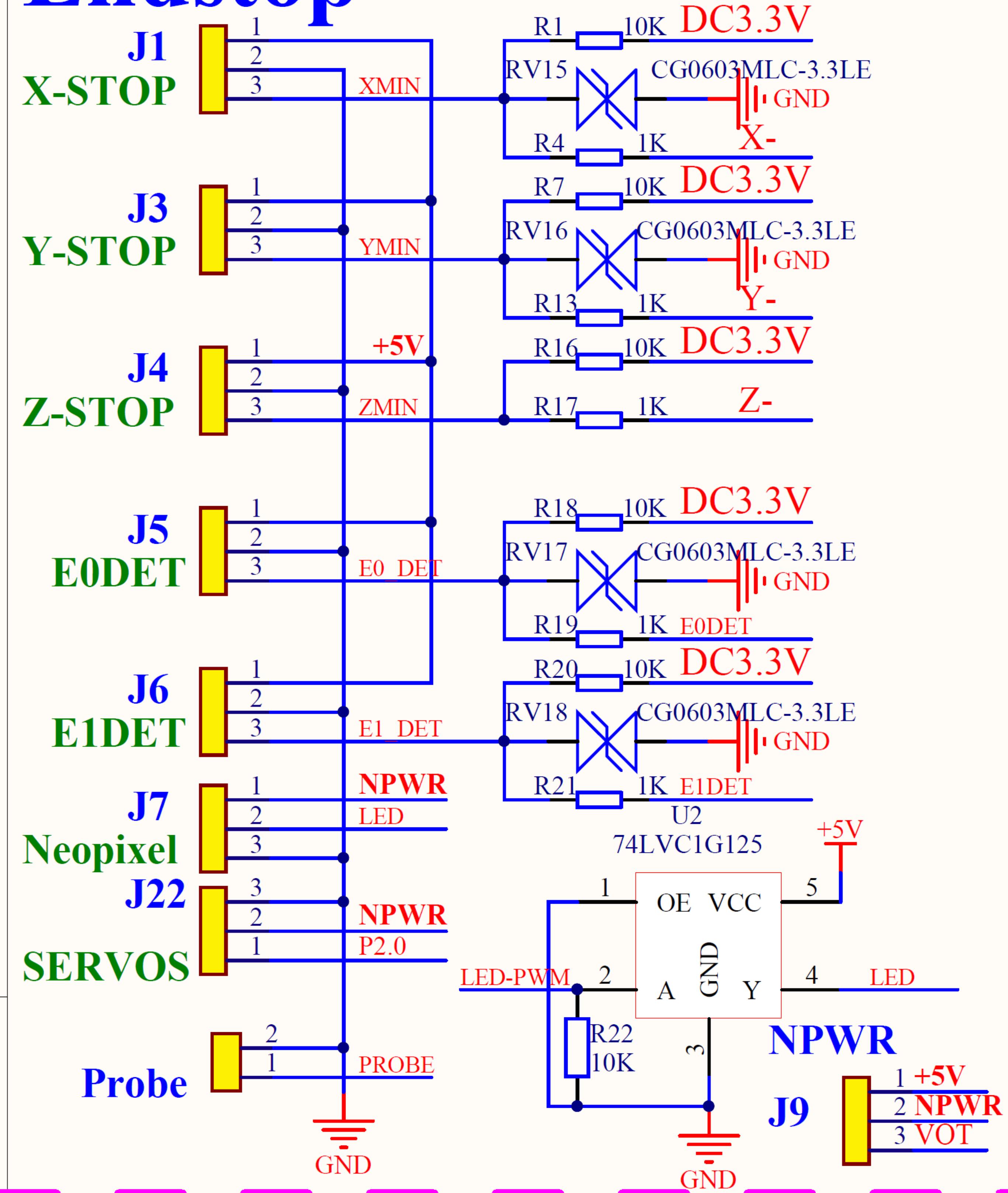
# SD-M



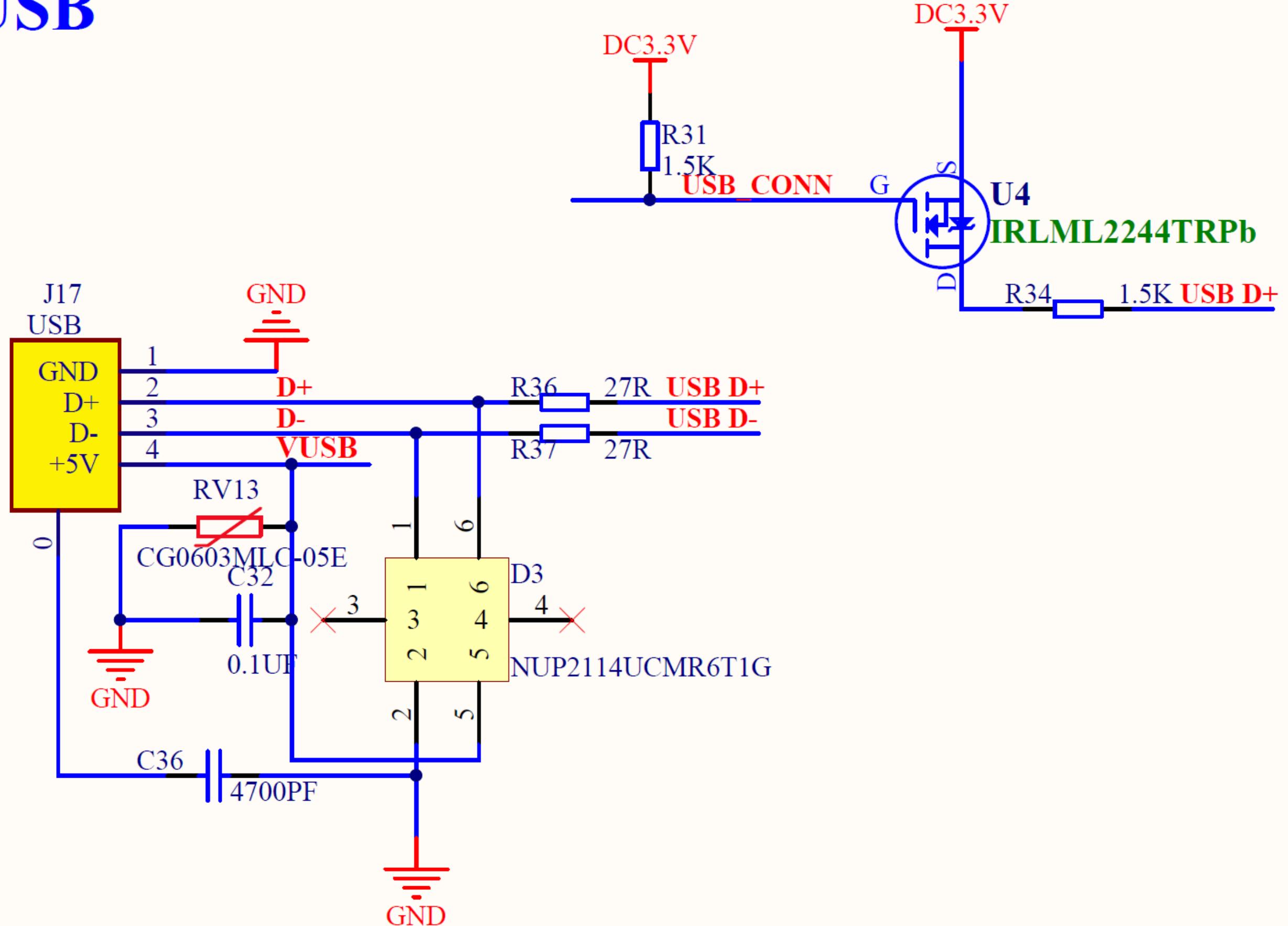
# SD-Card



# Endstop



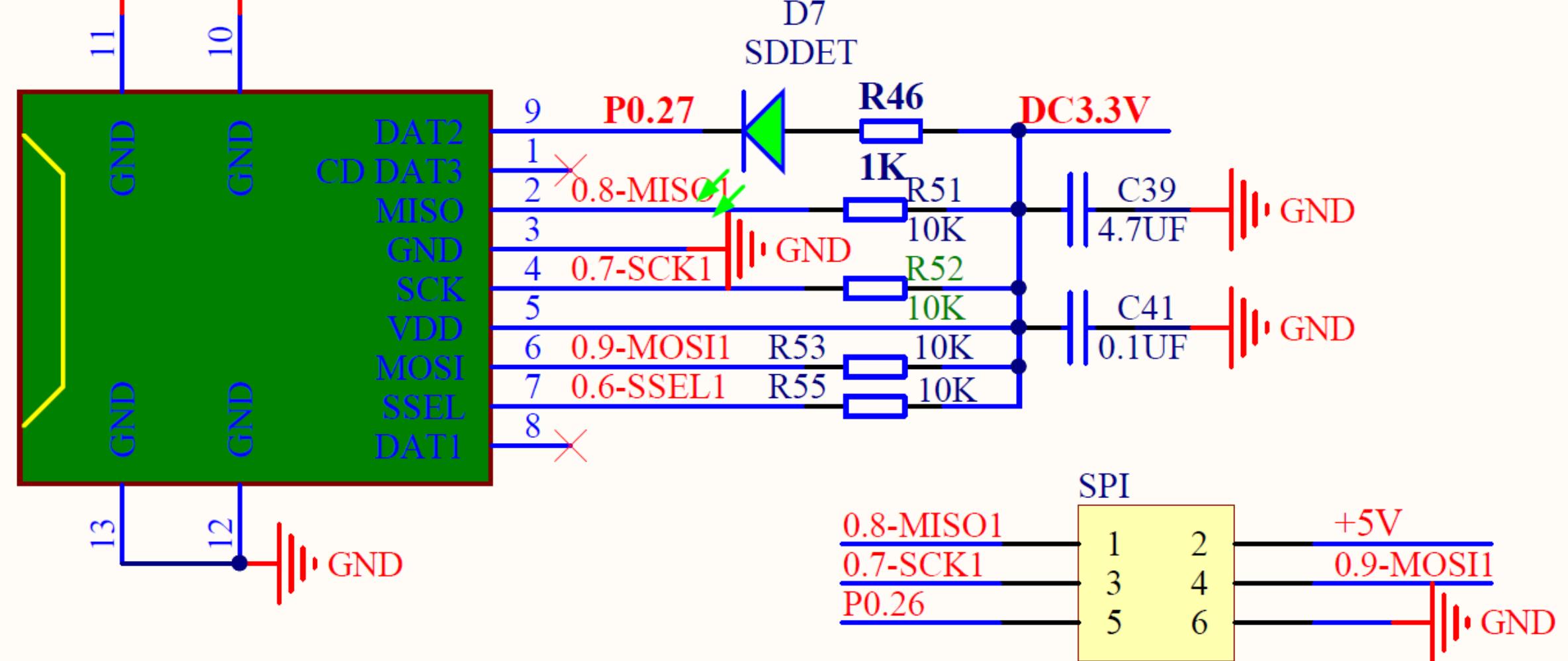
USB

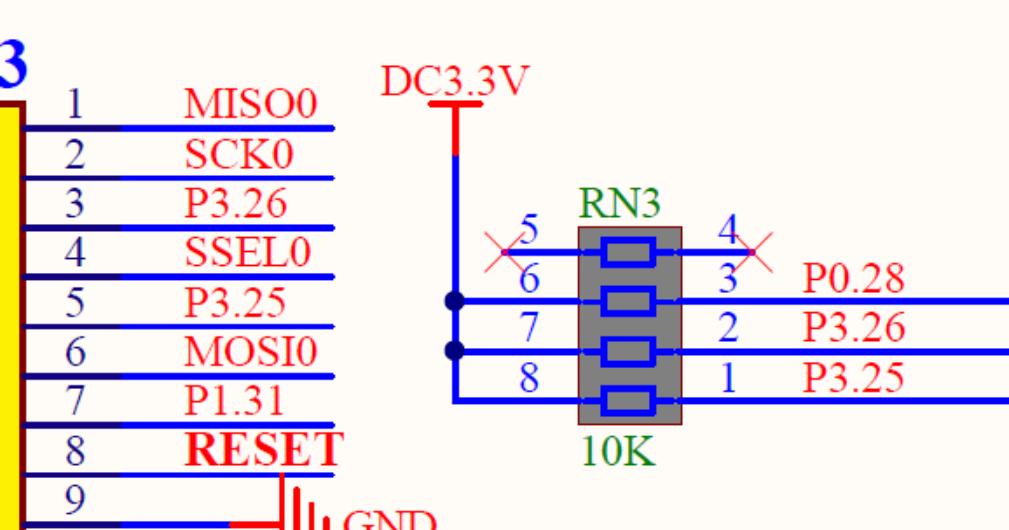
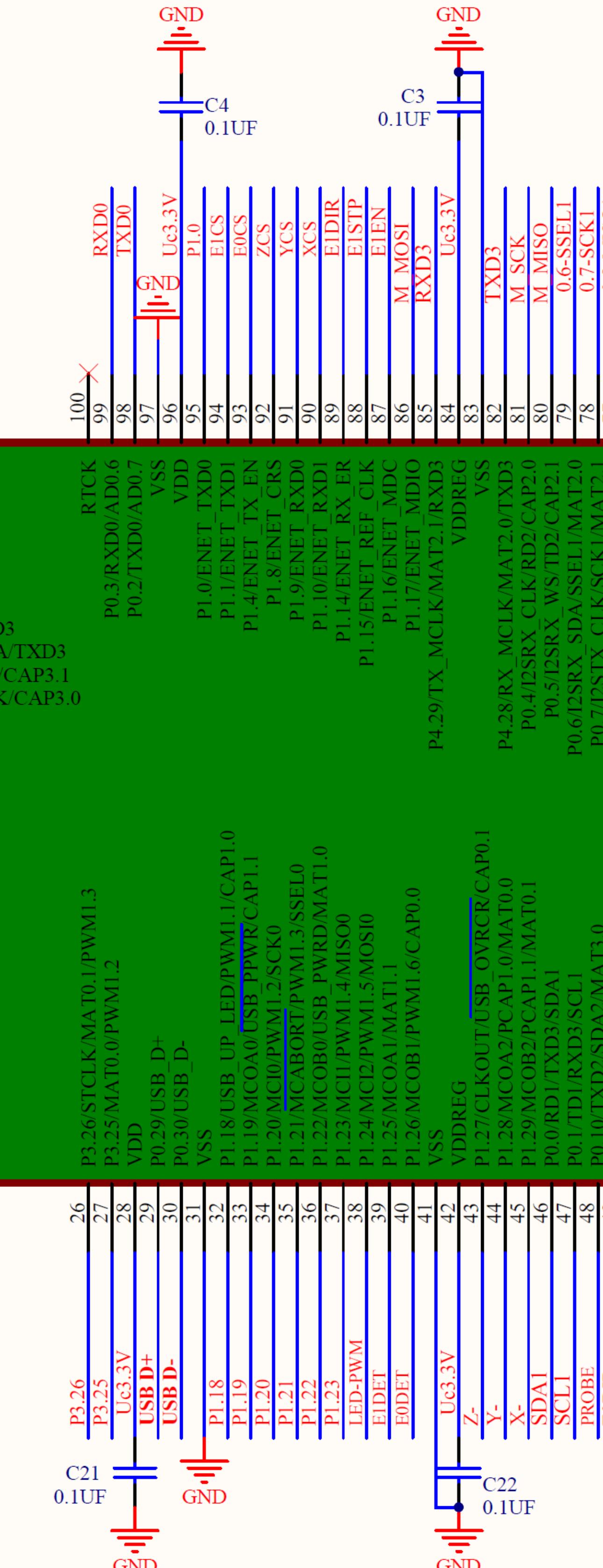
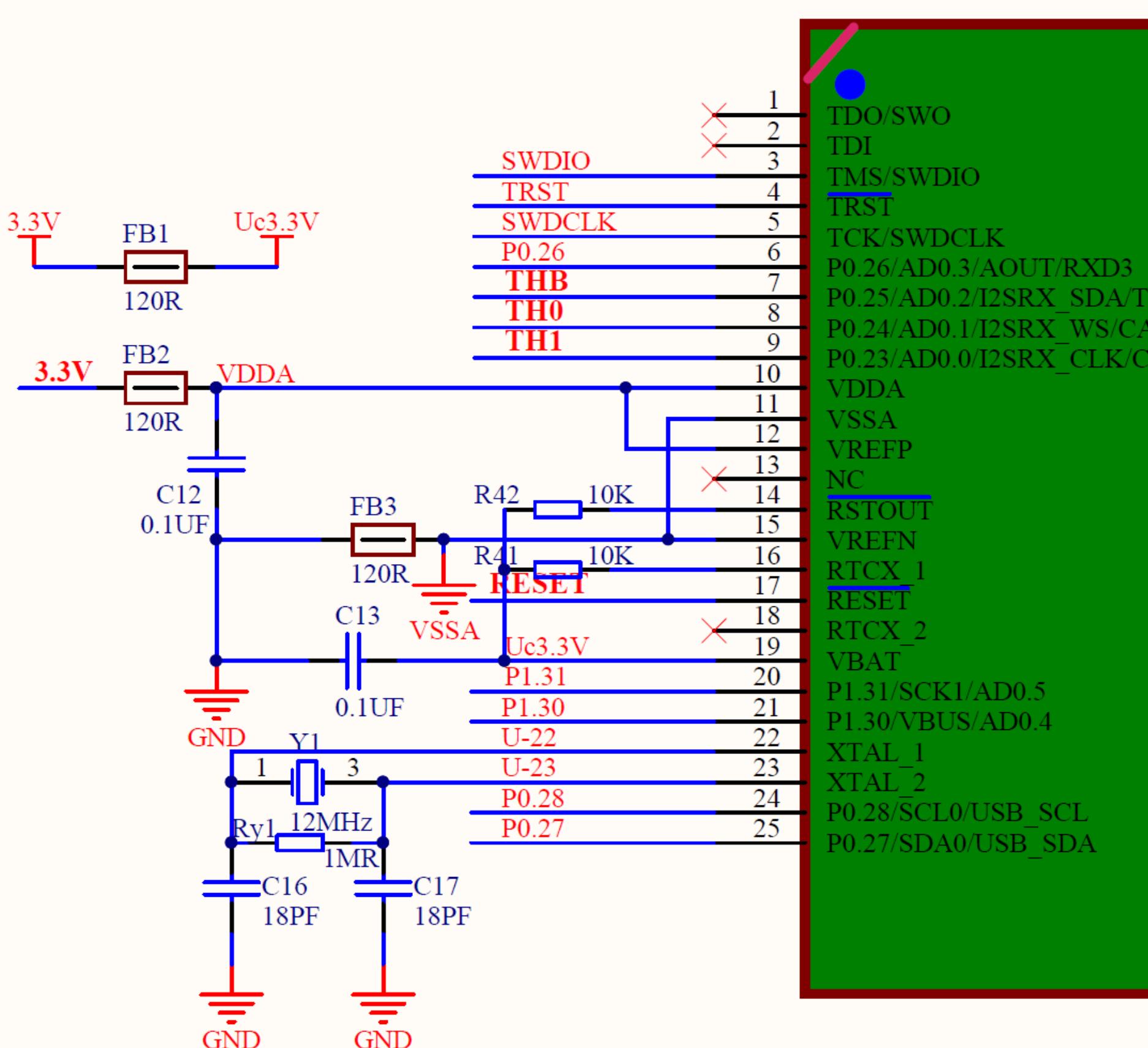
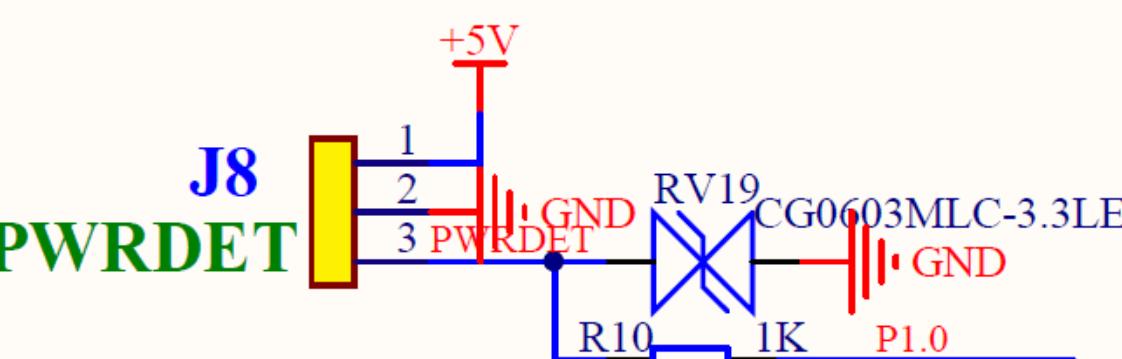
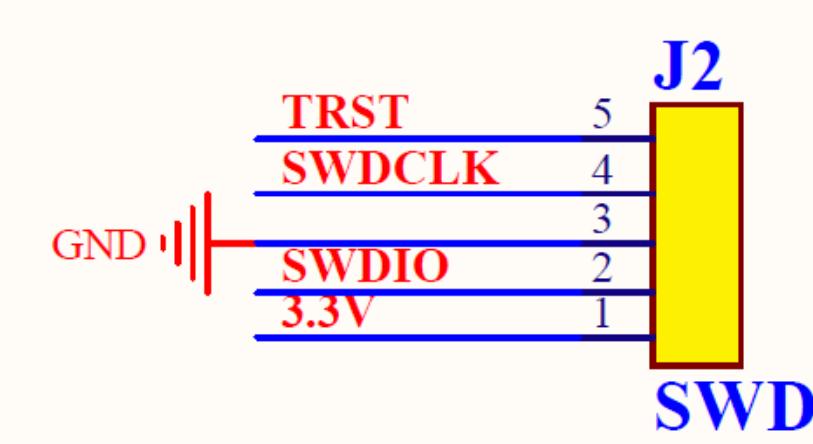


# SD-Card

# U7

## SD-M

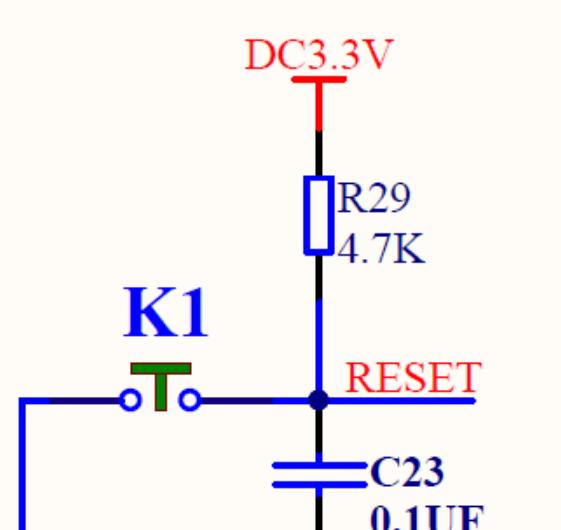




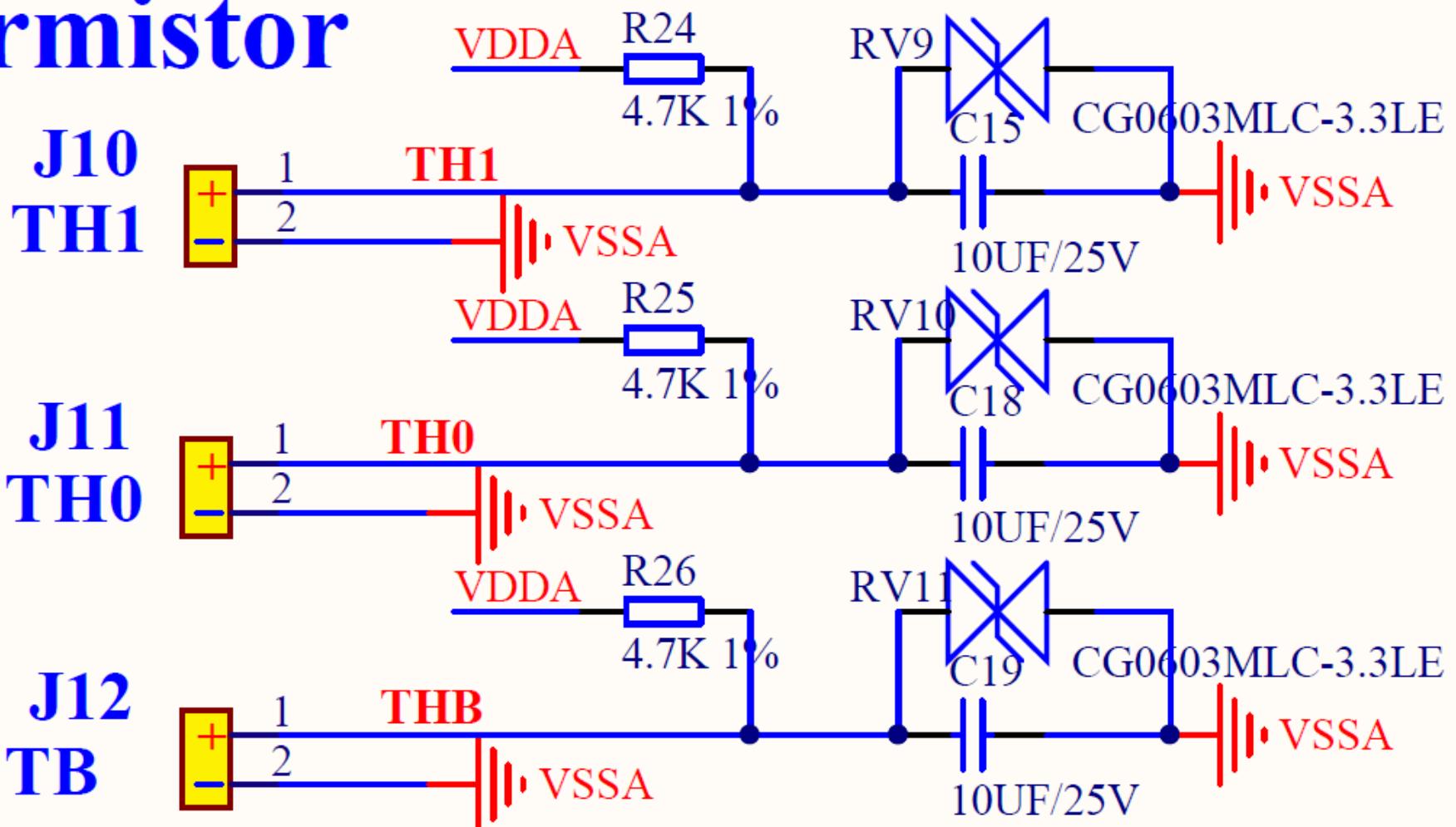
**U1**  
**LPC1768/LPC1769**



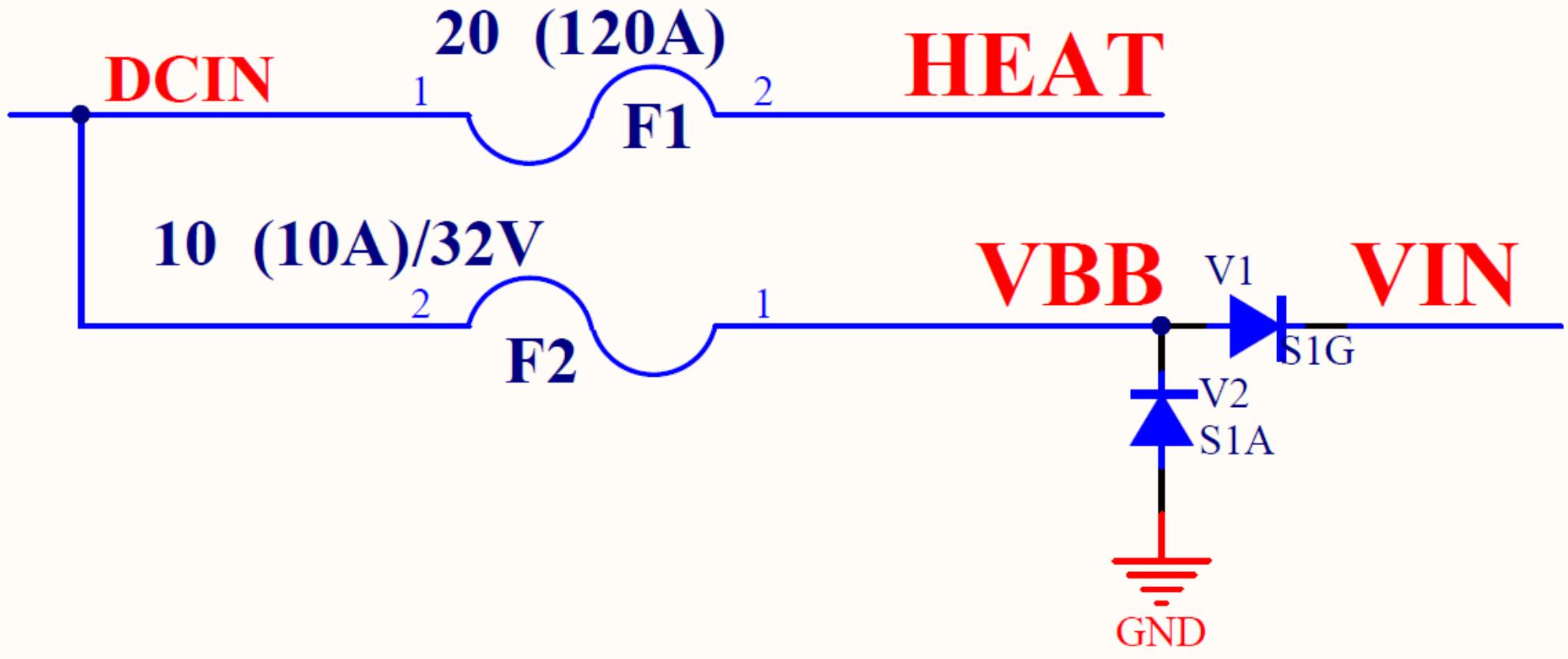
**RESET**

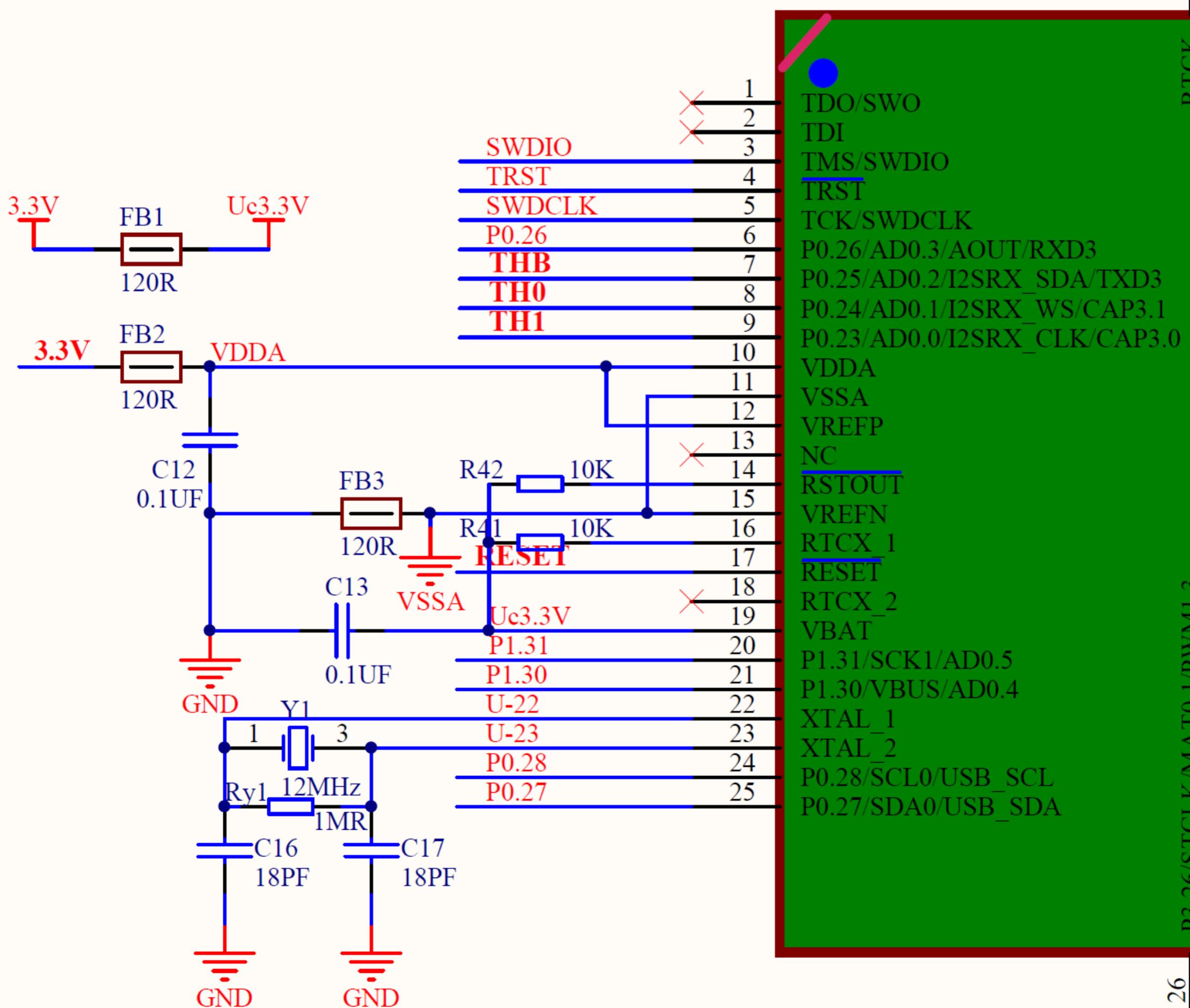
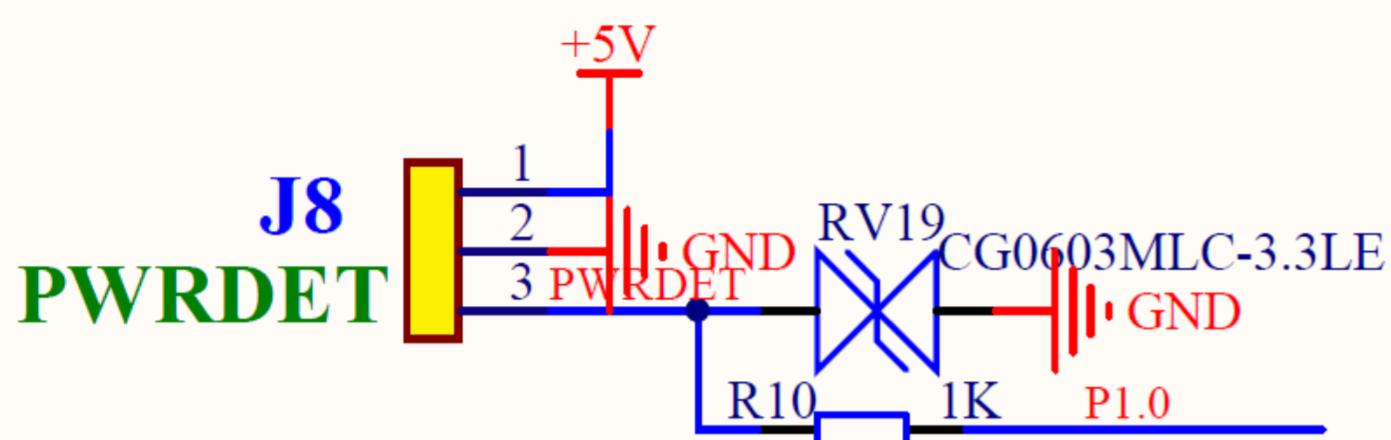
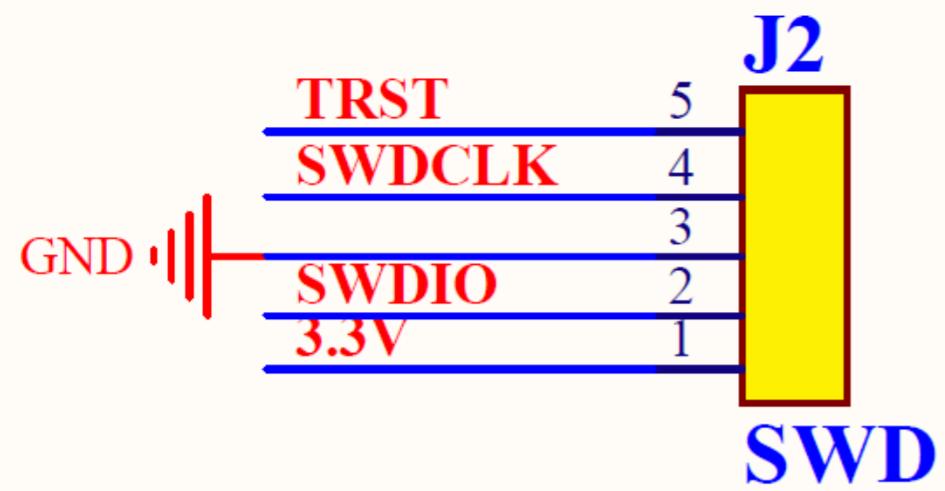


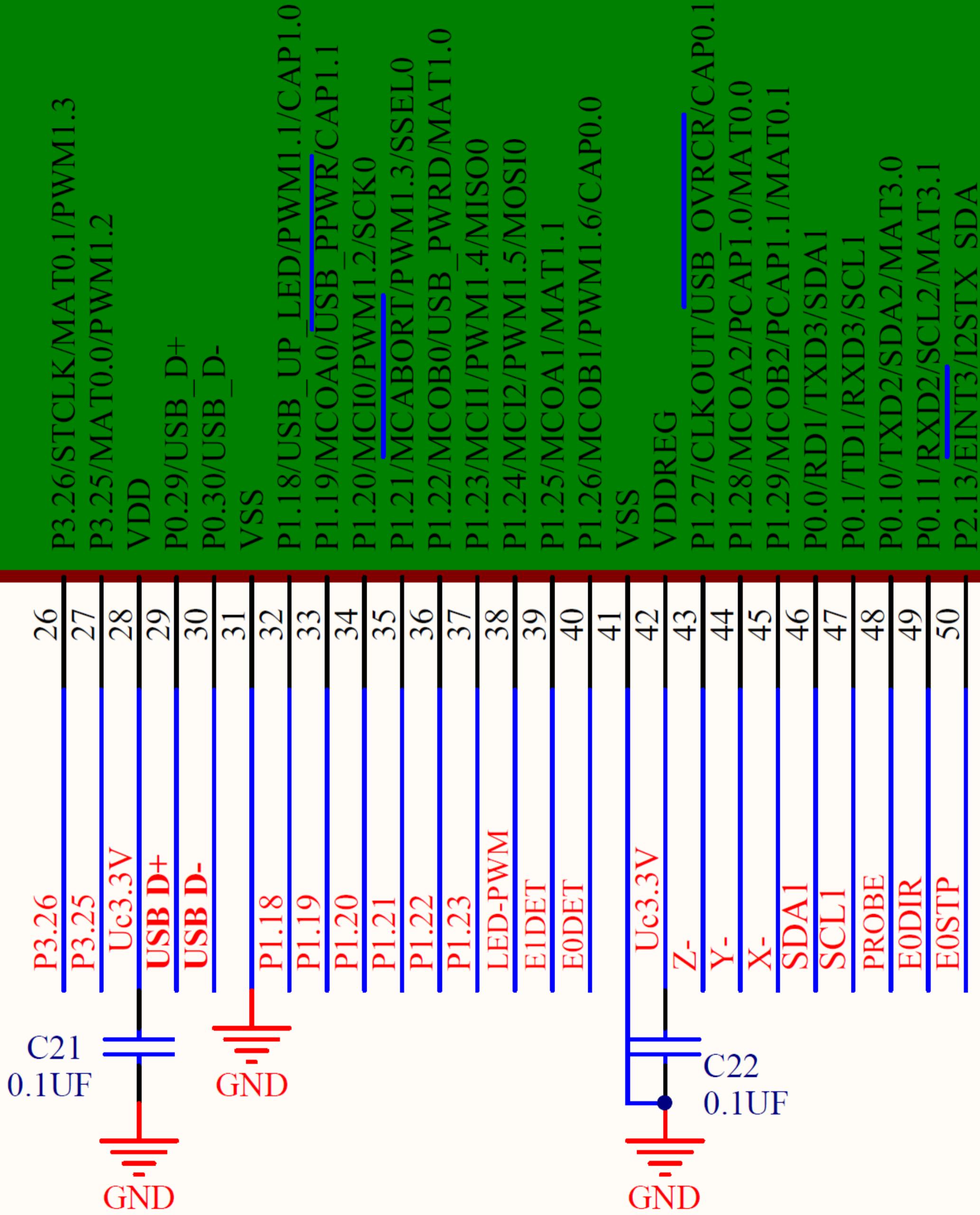
# Thermistor

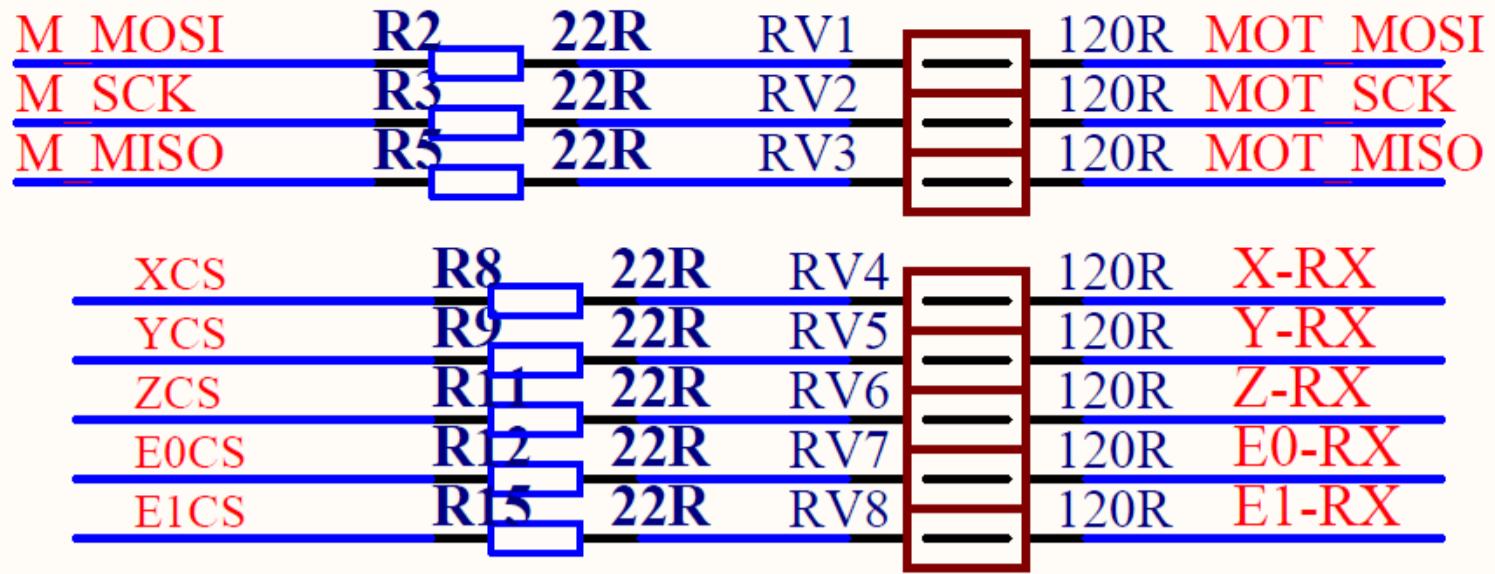


# FUSE



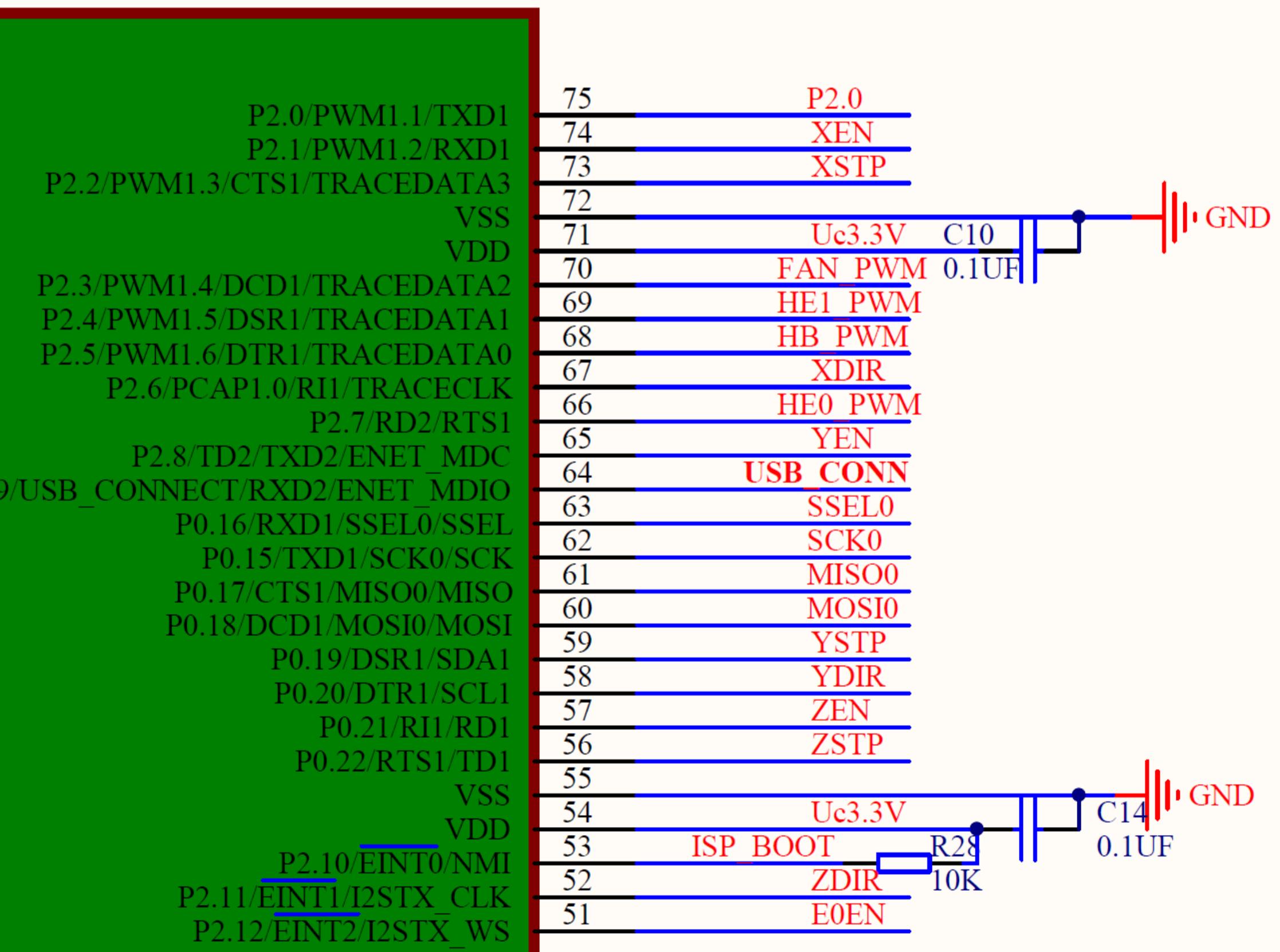


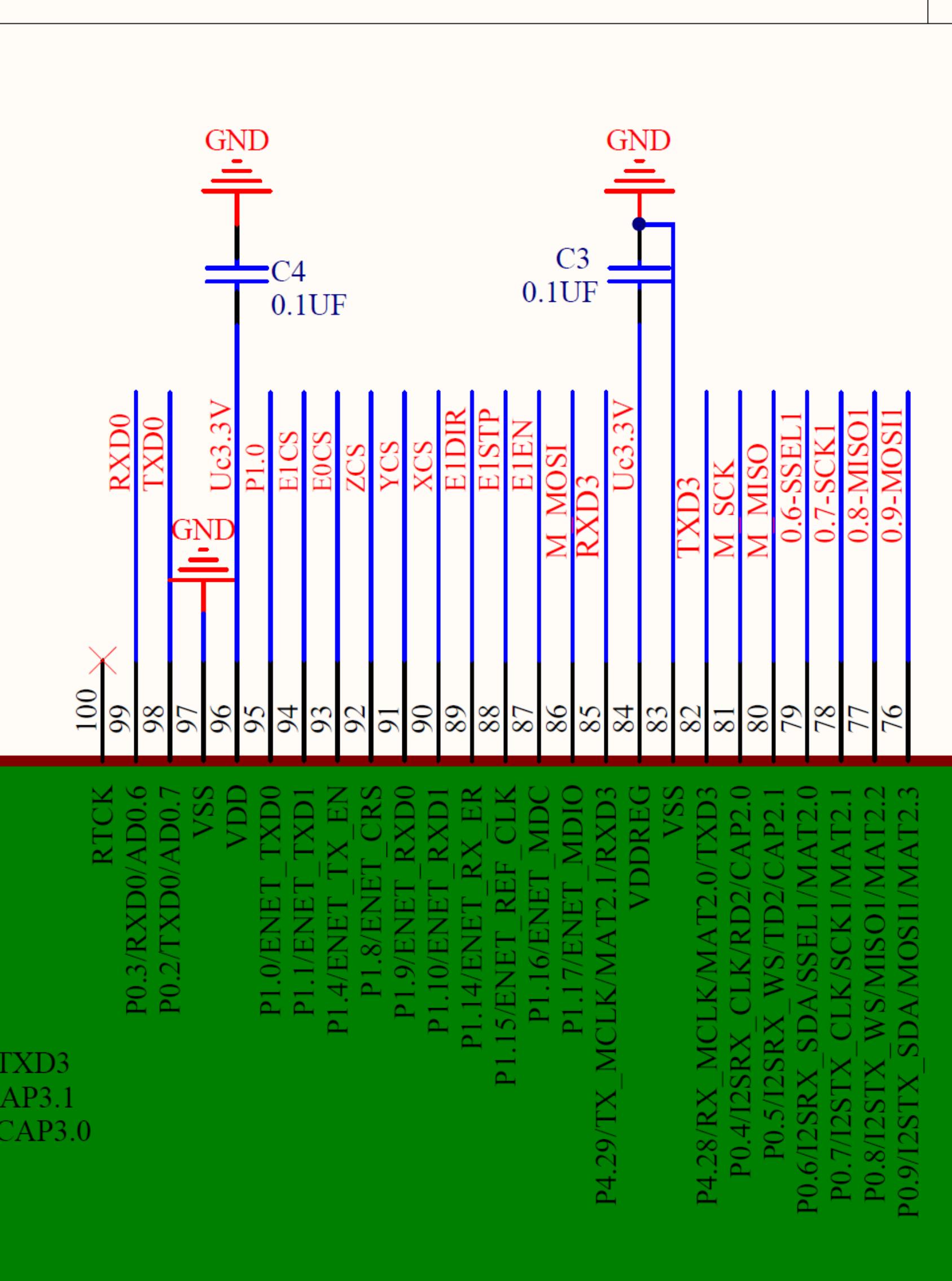




U1

## LPC1768/LPC1769





# MC74HCT125A

## Quad 3-State Noninverting Buffer with LSTTL Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT125A is identical in pinout to the LS125. The device inputs are compatible with standard CMOS and LSTTL outputs.

The MC74HCT125A noninverting buffer is designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The devices have four separate output enables that are active-low.

#### Features

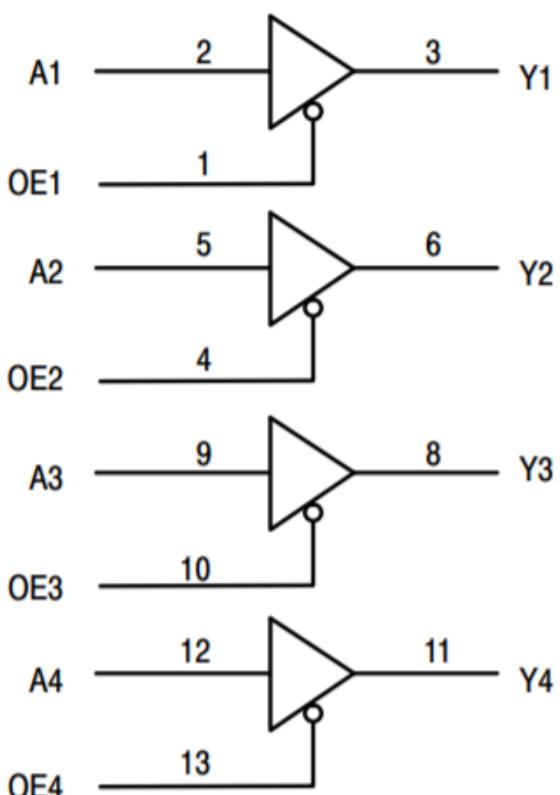
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7A Requirements
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These are Pb-Free Devices

#### PIN ASSIGNMENT

|     |   |   |    |                 |
|-----|---|---|----|-----------------|
| OE1 | 1 | • | 14 | V <sub>CC</sub> |
| A1  | 2 |   | 13 | OE4             |
| Y1  | 3 |   | 12 | A4              |
| OE2 | 4 |   | 11 | Y4              |
| A2  | 5 |   | 10 | OE3             |
| Y2  | 6 |   | 9  | A3              |
| GND | 7 |   | 8  | Y3              |

#### LOGIC DIAGRAM

##### Active-Low Output Enables



PIN 14 = V<sub>CC</sub>  
PIN 7 = GND

#### FUNCTION TABLE

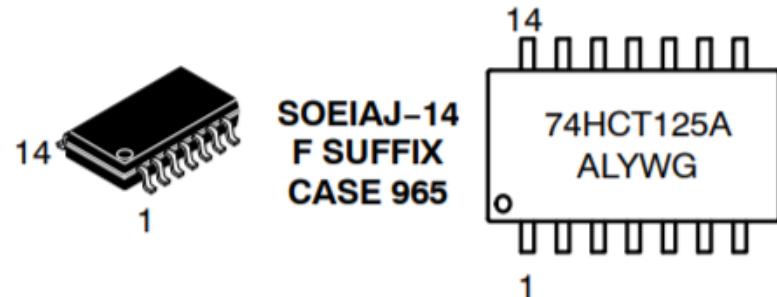
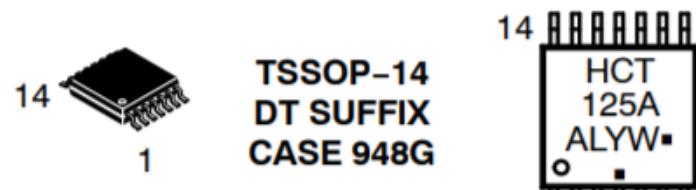
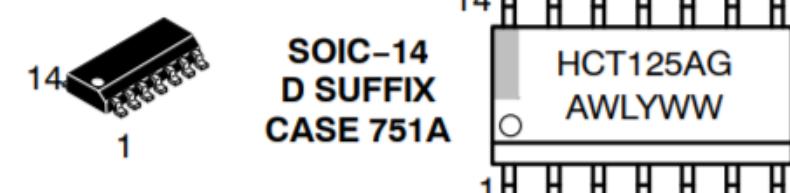
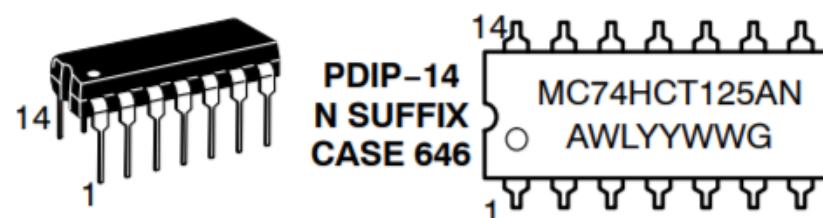
| HCT125A |    |        |
|---------|----|--------|
| Inputs  |    | Output |
| A       | OE | Y      |
| H       | L  | H      |
| L       | L  | L      |
| X       | H  | Z      |



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#### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.