A Power Management Unit With 40 dB Switching-Noise-Suppression for a Thermal Harvesting Array

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***Abstract*—A high efficiency, maximum power point tracking (MPPT) power management unit (PMU), with 3.6 μW quiescent power, aimed at a thermoelectric generator (TEG) array is presented. The proposed energy harvesting PMU is made up of a boost converter with a cascaded capacitor-less low drop-out (CL-LDO) voltage regulator. The segmented approach allows the PMU to match the TEG array's changing dynamic series resistance via the boost converter and simultaneously provide voltage regulation with adaptive, high switching noise rejection via the CL-LDO. The boost converter's switching frequency (f_{sw}) is tracked via a Sense-and-Control loop which modifies the CL-LDO's power supply rejection (PSR) characteristics to place a notch in the PSR transfer function around the average f_{sw}. Experimental results show an overall system efficiency better than 57% @ 1.6 V output voltage, PSR of 40 dB at f_{sw}, and a notch-tuning range of 15–65 kHz. The total active area is 0.93 mm^2 in 0.5 μm CMOS.**

***Index Terms*—Boost converter, energy harvesting, LDO, linear regulator, MPPT, power management unit, TEG.**

I. Introduction

INTEGRATED systems designed to fulfill the sensing and communications needs of medical implantable systems and wireless sensor networks or Internet of Things (IoT) applications have experienced a rapid evolution in recent years [1]–[5]. To keep up with the progress made in such advanced systems, similar development and improvement in compact energy sources and power management units (PMU) capable of meeting the power needs of such devices is required. Energy harvesting (EH) units have emerged as a valuable alternative to either replace or complement the battery-operation of wireless transmitters [6], [7]. In such systems, whether energy is harvested from human [6], RF [7], solar [8], vibrational [9], thermal [10], or multiple sources [11]–[13], reducing the intrinsic power consumption of the EH-PMU is critical for an efficient solution.

In addition to transferring most of the harvested energy to the load while consuming minimum power, there are other challenges the EH-PMU has to simultaneously meet. Such challenges include: maintaining a constant output voltage despite variations on the source conditions (adaptive input-to-output voltage gain); and ideally, providing a clean and regulated output voltage under different load conditions. Due to their high efficiency and intrinsic use of energy storage passive elements, most EH-PMUs use either inductor-based switching regulators [14] or switch-capacitor converters [15] to interface the EH transducer with the output load. However, due to the constant switching involved, these solutions tend to introduce large voltage ripple at the output. Although using super/ultra-capacitors alleviates the ripple problem, such devices largely impact the bill-of-materials (BOM) cost and board area.

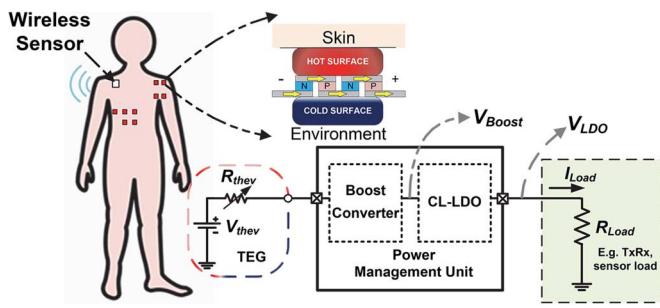

Fig. 1. Proposed EH-PMU implementation in a medical application setting.

This paper introduces an EH-PMU capable of extracting maximum power from a 3 × 3 thermoelectric generator (TEG) array via a boost converter (BC) with input resistance tracking capability. Furthermore, a low power, capacitor-less low-dropout voltage regulator (CL-LDO) cascaded with the BC acts as a ripple-reduction mechanism, providing high switching-noise-suppression to the output regulated voltage.

The proposed EH-PMU is suitable for operation in a medical application setting as the one illustrated in Fig. 1. Micropelt's MPG-DG655 TEG unit modules [16] are used to build a 3 × 3 array (electrically modeled with the R_{thev}, V_{thev} Thevenin equivalent). Taking advantage of a skin-environment temperature gradient ranging between 0.23–2.1 °C, the array is able to produce a V_{thev} of ∼200 mV while adopting configurations from all-parallel to all-series unit elements. Whilst V_{thev} can be maintained almost constant via array reconfiguration, the values for R_{thev} range between 19 Ω to 1.53 kΩ (due to unit TEG module resistance of 170 Ω). The BC uses V_{thev} as its input voltage and produces a higher voltage, V_{Boost}, which is adequate to power CMOS circuitry. A CL-LDO cascaded with the BC uses V_{Boost} as input to generate its regulated, cleaner version (V_{LDO}). Though the better quality V_{LDO} is the EH-PMU primary output, V_{Boost} is also available as a secondary output voltage.

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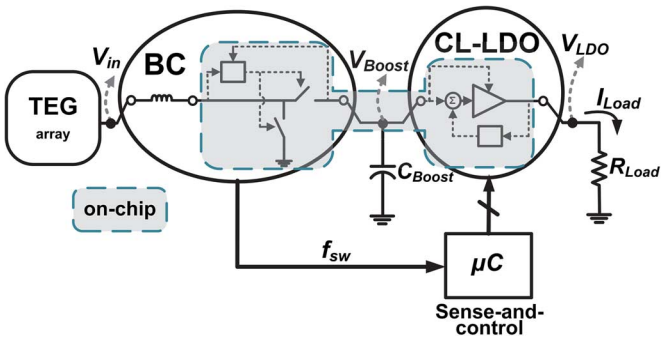

Fig. 2. EH-PMU for a TEG array using a boost converter and a CL-LDO.

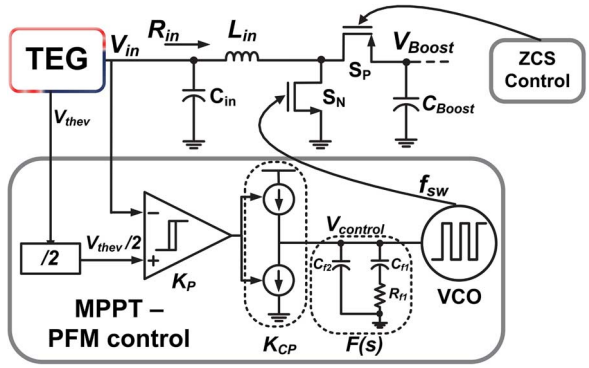

Fig. 3. Implemented boost converter with MPPT and ZCS schemes.

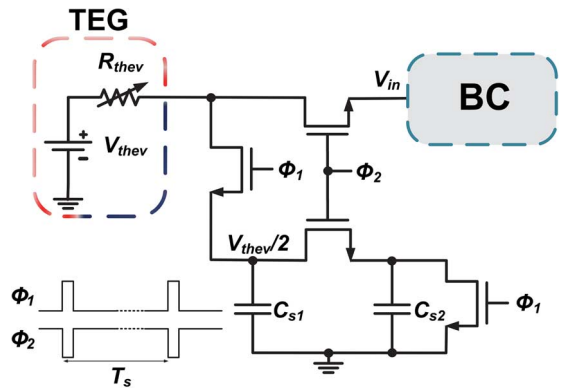

Fig. 4. Capacitive divider for $V_{thev}/2$ extraction [10].

This paper is organized as follows: Section II provides a system-level description of the proposed EH-PMU. Section III describes the BC used as the EH-PMU front-end and its implementation. Section IV presents the CL-LDO with tunable switching-noise suppression properties used in the EH-PMU back-end. Section V describes the implementation of a Sense-and-Control loop that allows the interaction between front and back-end of the EH-PMU. Section VI presents experimental results of the proposed EH-PMU with front-end and back-end results along with overall efficiency; and finally, Section VI provides this work's conclusions.

II. Energy Harvesting Power Management Unit

In addition to low intrinsic power consumption, for an EH-PMU to be truly viable as a standalone or complementary energy source for noise sensitive blocks, it should: *a*) Extract maximum power from the EH source; and *b*) Deliver a CMOS compatible, clean, regulated output voltage. To meet these requirements, the proposed low-power EH-PMU (Fig. 2) uses a boost DC-DC switching converter (BC) as front-end and a CL-LDO as back-end. The BC applies a maximum power point tracking (MPPT) technique at the interface with the TEG array, achieving optimum energy extraction while conditioning the EH-PMU internal voltage levels.

The front-end BC brings V_{thev} to usable—higher—CMOS levels at its output V_{Boost} (1.8 V). However, demanding voltage regulation and reduced voltage ripple from the front-end, increases the burden and complexity on the BC, which translates in a power hungry BC controller and a low system efficiency. Conversely, using a cascaded CL-LDO provides superior ripple rejection and a steady and regulated output voltage (V_{LDO}, 1.6 V) to the EH-PMU load. The supply-noise-rejecting capabilities of the proposed CL-LDO come from programmable notch-like characteristics in its supply-to-output path. Furthermore, the ultra-low power consumption of the CL-LDO yields high efficiency. Leveraging the superior switching-noise suppression of the CL-LDO, it is possible for our EH-PMU to use an off-chip capacitor C_{Boost} in the order of nF. While replacing the supercapacitor [9] with a nF-C_{Boost} reduces the long-term energy storage capabilities, it also considerably reduces the board area and bill-of-materials expenses. In turn, the regulated output voltage at V_{LDO} is an inexpensive solution, suitable for loads with low supply-ripple and low current requirements [4], [5].

To complement the EH-PMU, a Sense-and-Control (SaC) loop is implemented using an external microcontroller. The SaC determines the BC average switching frequency ($\overline{f_{sw}}$) and generates tuning signals for the CL-LDO to place a notch around $\overline{f_{sw}}$. As a result, significant ripple reduction at the EH-PMU output is obtained and experimentally demonstrated.

III. Energy Harvesting Power Management Unit Front-End

The EH-PMU front-end uses the BC shown in Fig. 3, which employs zero current switching (ZCS) and MPPT techniques to improve its efficiency. As suggested in [10], [17], MPPT is achieved by matching the resistance of the source (TEG array, R_{thev}) to the input resistance of the harvester (R_{in}). In Fig. 3, the MPPT loop modulates the switching frequency (f_{sw}) of the BC until the $R_{in} \approx R_{thev}$ condition is reached.

It is during each reconfiguration event within the TEG array that the BC must quickly and accurately track and match the new R_{thev} value to ensure continuous maximum power transfer from the array. Once R_{in} has been matched to R_{thev}, the input voltage for the BC settles at half the TEG array open circuit voltage $V_{thev}/2$, indicating that the maximum point for power (MPP) transfer has been reached. Thus, following the MPP under R_{thev} changes due to TEG array reconfiguration requires a dynamic MPPT scheme.

For comparison purposes, the $V_{thev}/2$ threshold is obtained through a capacitive divider [10] (Fig. 4). During phase φ_1 the TEG-BC connection is opened and V_{thev} is sampled into capacitor C_{s1}. Later, during φ_2, the TEG-BC connection is restored and C_{s1} is connected in parallel with C_{s2}. Through charge redistribution, the voltage developed in both C_{s1} and C_{s2} is now equal to $V_{thev}/2$ (provided $C_{s1} = C_{s2}$).

A. Input Resistance Matching

As mentioned in Section I, the TEG array modules can reconfigure their interconnections to take advantage of different temperature gradients naturally available throughout the human body to increase overall system power extraction. For the proposed 3×3 array, the two major scenarios that take into consideration the best/worst case power conditions are the fully par-

allel and fully series connections of the array, respectively. The design of the EH-PMU was aimed at voltages ranging from 50 mV to 200 mV, which are voltages delivered by a single TEG module under a temperature gradient of approximately 0.23 °C to 2.1 °C.

The series-parallel connection of the TEG array leads to an R_{thev} ranging from 1.53 kΩ to 19 Ω for the series and parallel configurations, respectively. For the design of the BC, Discontinuous Conduction Mode (DCM) was selected due to the low power nature of the application and in order to maintain power consumption to a minimum. For DCM operation, [18] shows that R_{in} can be approximated to:

$$R_{in} \approx \frac{2L_{in}f_{sw}}{D_{NMOS}^2} \tag{1}$$

In (1), L_{in}, f_{sw}, and D_{NMOS} are the input inductor value, switching frequency of the BC, and duty cycle of the control signal of NMOS switch S_N; all in reference to Fig. 3. This prompts the use of a Pulse Frequency Modulation (PFM) scheme to control R_{in}. Although both D_{NMOS} and f_{sw} are capable of modulating R_{in}, the R_{in}-quadratic dependency on D_{NMOS} requires a highly precise and power hungry control scheme. Hence, f_{sw} is selected as the control variable to maintain a linear control of R_{in} by setting the value of D_{NMOS} at 50% of the switching period.

A second approach to minimize power consumption by the BC was to restrict the f_{sw} range over which the converter will operate to low values. This reduces the total dynamic power consumption for the system. Choosing a 5 mH inductor as L_{in} sets the value of f_{sw} to vary from ∼38 kHz to ∼500 Hz for the required R_{thev} values to match. While this L_{in} value might seem high, it is not uncommon for integrated energy harvesting systems to use off-chip inductors with similar or higher values [19]. In our case, the selected L_{in} value allows successful operation using low switching frequencies, which in turn reduces the overall power consumption and maximizes the global efficiency.

B. Maximum Power Point Tracking Loop

As described in [10], the MPPT scheme possesses a matching range over which the system can assure maximum power extraction. The MPPT scheme allows for rapid maximum power extraction when changes occur on the equivalent R_{thev}. Similar to a phase locked loop (PLL), loop stability is a primary concern in order to avoid unstable responses from the system when an R_{thev} change occurs.

The block diagram in Fig. 5 presents the small-signal model that makes up the MPPT system of Fig. 3, where $V_{thev}/2$ and V_{in} are the halved open circuit voltage of the TEG array and the input voltage of the BC, correspondingly. The variables K_P, K_{CP}, $F(s)$, and $H_{c-in}(s)$ are the linear gain of the comparator, charge pump bias current, filter transfer function, and control-to-input transfer function for the BC, respectively. Hence, the open loop transfer function of the complete MPPT loop is given by:

$$TF_{OL}(s) = K_P K_{CP} F(s) H_{c-in}(s) \tag{2}$$

The control-to-input transfer function, $H_{c-in}(s)$, is obtained following [18]. Assuming steady-state operation, both the input source (V_{thev}) and the BC output voltage (V_{Boost}) can be presumed to be AC ground during the small-signal analysis due to the 10 nF C_{Boost}. Under these assumptions, the small-signal model shown in Fig. 5 is used to analyze the MPPT loop stability. The parameters j_1 and r_1, (Fig. 5) are obtained via three dimensional Taylor series expansions of the average input and output voltages and duty cycle [20] at steady-state operation. The variable $V_{control}$, seen in both Fig. 3 and Fig. 5, is the VCO control voltage coming from the filter block, $F(s)$.

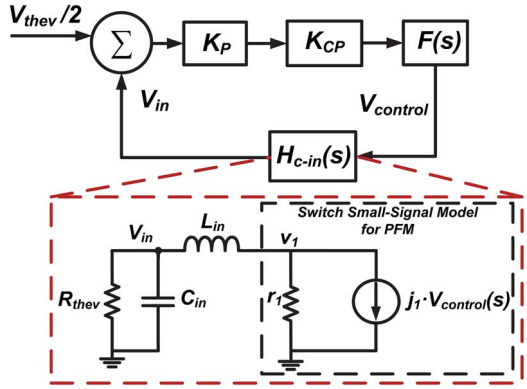

Fig. 5. Control loop and equivalent small-signal model for PFM BC.

Using the simplified model of Fig. 5, the $H_{c-in}(s)$ transfer function includes the effect of the VCO linear gain and yields:

$$H_{c-in}(s) = \frac{V_{in}(s)}{V_{control}(s)} = \frac{\frac{j_1 r_1}{L_{in}C_{in}}}{s^2 + 2\xi\omega_o s + \omega_o^2} \tag{3}$$

where

$$\omega_o = \sqrt{\frac{R_{thev} + r_1}{L_{in}C_{in}R_{thev}}} \tag{4}$$

$$\xi = \frac{(L_{in} + C_{in}R_{thev}r_1)}{2\sqrt{(C_{in}L_{in}R_{thev})(R_{thev} + r_1)}} \tag{5}$$

Extending the charge-pump-based PLL analogy, an external, second order passive loop filter $F(s)$ formed by capacitors $C_{f1,2}$ and resistor R_{f1} (Fig. 3) is used to enhance the MPPT loop response. In this case, (2) becomes:

$$TF_{OL}(s) = \frac{K_p K_{CP}(sC_{f1}R_{f1} + 1)H_{c-in}(s)}{(C_{f1} + C_{f2})s\,(s(C_{f1}\|C_{f2})R_{f1} + 1)} \tag{6}$$

Assuming a V_{in} of 100 mV, with C_{f1} of 100 nF, C_{f2} of 10 nF, and R_{f1} of 500 Ω, for a $K_P \approx 80$ dB, and K_{CP} of 100 nA (charge pump current [21]); in the mid-value of R_{thev} (775 Ω), the MPPT loop has unity gain frequency (UGF) of 2 kHz, and phase margin (PM) of 88°. Thus, a second order $F(s)$ allows for a stable system response over a wide range of equivalent resistance values (R_{thev}) and a rapid response after a TEG array reconfiguration.

C. Zero Current Switching Scheme

Reducing stress on monolithic components and improving efficiency are important goals for any switching converter to reach. In order to address both these issues, a zero current switching (ZCS) technique is employed. The ZCS scheme shown in Fig. 6 minimizes the inductor current losses through the PMOS switch, S_P, and is implemented following [22]. The ZCS is performed via a skewed voltage peak detector in the V_{sw} node. This voltage is next compared to a fixed reference, V_{zref}. The comparison result is used to generate voltage V_{c2}, which eventually regulates the on/off time of S_P (Fig. 6), reducing the inductor current losses.

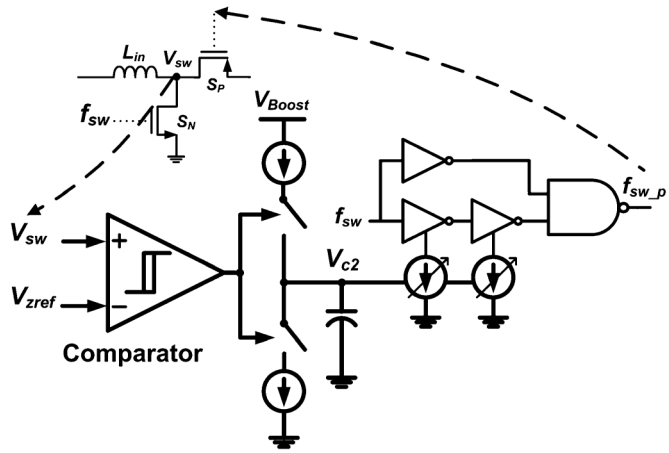

Fig. 6. Zero Current Switching Tracking loop implementation [22].

As discussed in [14], when S_P is turned off and L_{in}'s current has not been fully delivered, an associated voltage surge is perceived at V_{sw}. This voltage surge is proportional to the rate of change of the remaining current in L_{in} when S_P is off. Ideally the inductor current would fall to zero before the PMOS is switched off, thus, reducing any losses associated with this switch. A dynamic Zero Current Switching Tracking (ZCST) loop [22] is implemented to minimize the potential losses associated with negative inductor current.

IV. Energy Harvesting Power Management Unit Back-End

Even though the EH-PMU front-end successfully performs MPPT from the TEG harvester and develops an output voltage V_{Boost} sufficiently high to drive low power circuits, V_{Boost} exhibits a large voltage ripple. Thus, directly using V_{Boost} to power electronic circuits might lead to unacceptable performance or failure of the energy-recipient circuits, particularly in the case of circuits with high supply-noise sensitivity. The proposed EH-PMU incorporates an LDO as its back-end to solve this problem. Although using an LDO to reduce the ripple in V_{Boost} and produce a quiet voltage, V_{LDO}, might seem as a straightforward solution; the high end-to-end efficiency expected from the EH-PMU limits the power that can be used to design a high performance LDO. Furthermore, to reduce the cost of the required external components of the solution, a capacitor-less LDO (CL-LDO) is used.

For the CL-LDO in the EH-PMU back-end to successfully attenuate the magnitude of the ripple in V_{Boost}, the CL-LDO should possess high power supply rejection (PSR) at and around the ripple frequency (f_{sw}). Multiple CL-LDO advanced structures with notorious PSR improvements have been recently proposed [23]–[27]. However, most of these works report current consumptions from several to a few hundreds of μA and are designed to deliver load currents between 20 to 100 mA. Nonetheless, in the case of a CL-LDO targeted for EH applications, the available current to deliver to the load might be scarce and dependent on the conditions surrounding the EH transducer (thermal gradient between the TEG plates). Thus, investing even ten μA to get a well regulated and ripple-reduced output voltage represents a major cut to the available current to be delivered to the load, and can seriously harm the end-to-end system's efficiency. Thus, to reduce the CL-LDO complexity and quiescent current, it is convenient to analyze the basic CL-LDO structure of Fig. 7 to determine its fundamental PSR limits.

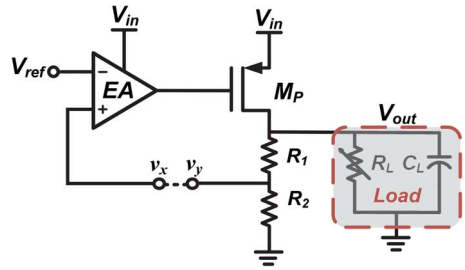

Fig. 7. Simple CL-LDO structure.

A. Basic CL-LDO

In the CL-LDO of Fig. 7, the error amplifier (EA) is assumed to be a single stage differential pair amplifier; the pass transistor ($\mathrm{M_P}$) is a PMOS device; resistors R_{1-2} form a feedback voltage divider, $\beta = R_2/(R_2 + R_1)$; and V_{ref} is selected such that $V_{out} \approx \beta V_{ref}$ (assuming large loop gain). The load is modeled by resistor R_L and capacitor C_L (to account for the load *parasitic* capacitance and/or a small on-chip capacitance).

The open loop gain of the CL-LDO in Fig. 7 ($LG(s)$, evaluated from v_x to v_y) is given by (7). $LG(s)$ contains two poles (ω_{px} and ω_{py}) and one zero (ω_z). A_{EA} and A_{MP} represent the DC voltage gain of the EA and $\mathrm{M_P}$, respectively. To approximate the locations of the poles (8) and zero (9), it is assumed that *a*) C_L is small and *b*) The EA output conductance, g_{oE}, is smaller than the total output conductance, g_{OUT}, formed by g_L $(1/R_L)$ and the $\mathrm{M_P}$ conductance, g_{oMP}. Note that C_p and C_{gd} in (8)-(9) stand for the total $\mathrm{M_P}$'s gate-to-source (including-to-bulk), and gate-to-drain parasitic capacitance, respectively.

$$LG(s) = A_{EA}(s)A_{MP}(s)\beta = \frac{A_{EA}A_{MP}\beta(s/\omega_z - 1)}{(s/\omega_{px}+1)(s/\omega_{py}+1)} \tag{7}$$

$$\omega_{px} \approx \frac{g_{oEA}}{A_{MP}C_{gd}},\ \omega_{py} \approx \frac{g_{OUT}(C_p/C_{gd}+1)+gm_{MP}}{(C_p/C_{gd}+1)C_L+C_p} \tag{8}$$

$$\omega_z \approx \frac{gm_{MP}}{C_{gd}} \tag{9}$$

The approximations for ω_{px} (typically the dominant pole) and ω_z are consistent with the expressions found in previous works [28]. However, due to the low I_L in our application, the $\mathrm{M_P}$ transconductance (gm_{MP}) and g_{oMP} values might have similar magnitudes. Thus, a detailed expression for ω_{py} is provided in (8). As expected, satisfactory phase margin and loop stability can only be achieved if enough separation exists between ω_{px} and ω_{py} for all I_L of interest. In this case, loop stability can be achieved using Miller compensation at expense of reduced gain-bandwidth product (GBW) and increased power consumption.

Similarly, the PSR of the CL-LDO in Fig. 7 is given in (10). $PSR(s)$ has two zeros and two poles which are approximated in (11) and (12), respectively. Analyzing (10), it can be concluded that the DC PSR of the CL-LDO starts to degrade at ω_{zPSR1}, and in order to improve the PSR performance, ω_{zPSR1} should be pushed to higher frequencies. Unfortunately this solution generally entails increased power consumption, which cannot be tolerated in a CL-LDO for low power EH applications.

$$PSR(s) = \frac{1}{A_{EA}A_{MP}\beta}\frac{(s/\omega_{zPSR1}+1)(s/\omega_{zPSR2}+1)}{(s/\omega_{pPSR1}+1)(s/\omega_{pPSR2}+1)} \tag{10}$$

$$\omega_{zPSR1} \approx \frac{g_{oEA}}{A_{MP}C_{gd}}, \quad \omega_{zPSR2} \approx \frac{gm_{MP}}{C_p} \tag{11}$$

$$\omega_{pPSR1} \approx \frac{gm_{EA}}{C_{gd}}, \quad \omega_{pPSR2} \approx \frac{gm_{MP}}{C_L\left(1+\frac{C_p}{C_{gd}}\right)+C_p} \tag{12}$$

Nonetheless, it is interesting to note that ω_{zPSR1} in $PSR(s)$ and ω_{px} in $LG(s)$ share the same expression. This means that the pole at the gate of $\mathrm{M_P}$ in $LG(s)$ is reflected as a zero in $PSR(s)$. This fact will be later recalled as the basis of the proposed PSR enhancement technique.

B. Proposed CL-LDO

In the two-stage EH-PMU, the ripple noise present at V_{Boost} (front-end-output/back-end-input) exhibits the strongest components at and around the switching frequency (f_{sw}). This localized noise nature suggests that it is not strictly necessary for the CL-LDO to exhibit uniformly high PSR across the frequency spectrum (from DC through f_{sw}), and as long as the PSR at f_{sw} is adequate, most of the switching noise at V_{Boost} will not be present at the PMU output voltage (V_{LDO}). Thus, a low power CL-LDO capable to emphasize its PSR at particular frequencies is implemented as the EH-PMU back-end. For higher flexibility, the CL-LDO PSR characteristics can be modified via a programmable bank of capacitors to reject particular frequencies (f_{sw}) within the range of interest.

One way for the CL-LDO to selectively reject a given f_{sw}, is to make its PSR transfer function to partially resemble a notch filter. If said notch is centered at f_{sw}, the main CL-LDO ripple noise components can be significantly attenuated at the PMU output. This approach allows improving the PSR performance without using an LDO with high PSR for all frequencies (which in general results in large power consumption).

The concept of using a tunable, continuous time notch/bandreject filter to remove noise at specific, well-identified frequencies has been widely exploited in wireless receivers [29]–[31]. In such applications, the notch filter can be merged with the low-noise amplifier (LNA) [29] at the receiver front-end to implement either an image rejection filter or to get rid of strong blockers [30]. Notch filtering has also been demonstrated using a broadband resistive feedback LNA with embedded feedforward to improve blocker rejection at third and higher oscillator harmonics [31].

The transfer function of a second order symmetrical notch filter is shown in (13) [32].

$$H_{NOTCH} = \frac{K\left(s^2+\omega_{zN}^2\right)}{s^2+\left(\frac{\omega_{oN}}{Q_p}\right)s+\omega_{oN}^2} \tag{13}$$

Note that whereas the poles of (13) can be real or complex, the zero-pair $(\pm\omega_{zN})$ is complex. The natural frequency is represented by ω_{oN}, K is the gain in the passband, and Q_p is the quality factor. Thus, to grant notch filter characteristics to the PSR of the CL-LDO in Fig. 7, a pair of complex *poles* should be placed at the gate of $\mathrm{M_P}$, such that, due to the loop action, are reflected as complex *zeros* in the PSR transfer function.

Including a notch in the CL-LDO PSR transfer function using techniques similar to the presented in [29]–[31] is neither straightforward nor convenient. In the case of an LNA with notch filtering, the notch is generally placed at frequencies out of the band of interest (to reject interferers and out-of-band blockers) and the additional phase shift at the notch frequency, $|\omega_{zN}|$, does not affect the correct reception of the transmitted signals within the system bandwidth. However, in the case of the LDO, the loop GBW is maximized (within power budget) to have fast transient response and extended noise suppression. Thus, when the f_{sw} is lower than the LDO GBW, the phase shift due to the required complex *poles* at the gate of $\mathrm{M_P}$ (responsible for generating the notch in the PSR transfer function) might jeopardize the loop stability and render the LDO unstable. For this reason, any modification made to include complex *poles* at the gate of $\mathrm{M_P}$ in the circuit of Fig. 7 should not affect the loop stability.

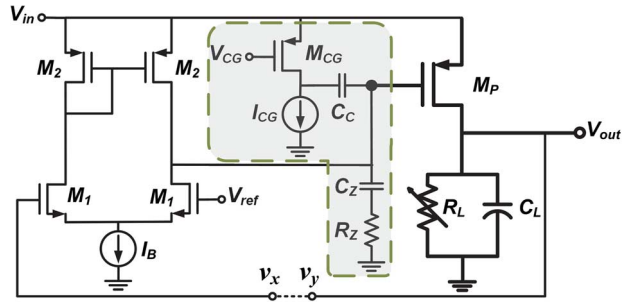

Fig. 8. Transistor-level implementation of the proposed CL-LDO.

Consider the circuit of Fig. 8 where the EA of the CL-LDO in Fig. 7 is implemented at the transistor level using an NMOS-input differential pair $(\mathrm{M_1}-\mathrm{M_2})$. Shown in a dashed line box in Fig. 8 is an auxiliary circuit used to modify the PSR characteristics of the CL-LDO and simultaneously stabilize the regulator. The auxiliary circuit is composed of transistor $\mathrm{M_{CG}}$ (biased via $\mathrm{V_{CG}}$ and $\mathrm{I_{CG}}$), a coupling capacitor C_C and a series R_ZC_Z load. To understand the function of the auxiliary circuit, the operation of the CL-LDO in Fig. 8 should be analyzed from two different perspectives: circuit stability and PSR.

C. CL-LDO Stability

If $\mathrm{V_{CG}}$ in Fig. 8 is a clean bias voltage, for the $v_x - v_y$ loop-stability purposes the auxiliary circuit appears only as an equivalent passive load. This load is formed by the parallel of the series R_ZC_Z branch and the series $R_{CGEQ}C_C$. While C_C, C_Z, and R_Z are passive elements, R_{CGEQ} is the parallel of the $\mathrm{M_{CG}}$ output resistance and the output resistance of the current source $\mathrm{I_{CG}}$. This is further illustrated in Fig. 9, where the small signal model of the $v_x - v_y$ loop is shown (note that for this analysis V_{ref} and V_{in} in Fig. 8 are assumed clean voltages -analog ground-). In Fig. 9, g_{mEA} and g_{mMP} represent the transconductances of the EA and $\mathrm{M_P}$, respectively, g_{oEA} is the EA output conductance, C_{gd} is the gate-to-drain parasitic capacitance of $\mathrm{M_P}$ and C_1 is the total parasitic capacitance at the gate of $\mathrm{M_P}$ (gate-to-source plus gate-to-bulk parasitic capacitances mainly). The expression for the equivalent admittance of the auxiliary circuit seen in the $v_x - v_y$ loop $-Y_{EQ}-$ is given in (14), where g_z and g_{CGEQ} denote the conductances of R_Z and R_{CGEQ}. The expressions for the zeros $(\omega_{zEQ1,2})$ and pole (ω_{pEQ}) of (14) are given in (15) and (16), respectively.

$$Y_{EQ}^{-1} = Z_{EQ} = \frac{1}{g_Z+g_{CGEQ}}\frac{(s+\omega_{zEQ1})(s+\omega_{zEQ2})}{s(s+\omega_{pEQ})} \tag{14}$$

$$\omega_{zEQ1} = \frac{g_{CGEQ}}{C_C} \qquad \omega_{zEQ2} = \frac{g_Z}{C_Z} \tag{15}$$

$$\omega_{pEQ} = \frac{g_zg_{CGEQ}}{g_z+g_{CGEQ}}\left[\frac{C_Z+C_C}{C_ZC_C}\right] \tag{16}$$

Using (14), it can be shown that the open loop gain (from v_x to v_y) of the circuit in Fig. 8 can be simplified to (17)

$$\frac{v_y}{v_x} = \frac{-A_{EA}A_{MP}(s+\omega_{zEQ1})(s+\omega_{zEQ2})(s-\omega_{z3})}{(s+\omega_{pST1})(s+\omega_{pST2})(s+\omega_{pST3})(s+\omega_{pST4})} \tag{17}$$

The loop gain of the proposed CL-LDO (17) has three zeros and four poles. Two of the zeros arise directly from the auxiliary circuit $(\omega_{zEQ1,2})$ and the third zero (ω_{z3}) is the same as the zero in the basic CL-LDO $LG(s)$ in (7) (i.e. $\omega_{z3} = \omega_z$ in (9)). Conversely, it is hard to determine useful, closed-form expressions for the poles of (17) unless the following application-specific (low power EH system) assumptions are made: *a*) $C_C > C_Z > C_L$; *b*) $\mathrm{M_P}$ provides only low I_L levels, thus C_{gd} and C_1 are both $\ll C_Z$; *c*) A_{MP} is low; and *d*) Both EA and $\mathrm{M_{CG}}$ operate at low inversion levels, however $g_{CGEQ} < g_{oEA}$ (e.g. $\mathrm{I_{CG}} < \mathrm{I_B}$ in Fig. 8).

The approximated, design-friendly expressions of the zeros and poles of (17) are summarized in Table I. Interestingly, ω_{zEQ1} and ω_{pST1} virtually cancel each other, which reduces (17) to a two-zero, three-pole system. Moreover, ω_{pST4} and ω_{z3} can be regarded as high frequency time constants, further simplifying the CL-LDO stability analysis to a two-pole $(\omega_{pST2,3})$ one-zero (ω_{zEQ2}) system where the GBW can be approximated as $A_{EA}A_{MP}\omega_{pST2}$.

Feedback resistors R_1 and R_2 (Fig. 7) have been removed in the proposed CL-LDO (Fig. 8); this yields $\beta = 1$ and reduces the CL-LDO quiescent current consumption. Note that the coupling action of C_C enables the interaction of the auxiliary circuit with the $v_x - v_y$ regulation loop, allowing for the $\mathrm{M_P}$ bias point to be determined by the regulation loop.

The required CL-LDO I_L range is determined based on the min and max theoretical power (P_{in}) that can be extracted from the TEG array; this is given by V_{thev}^2/R_{thev}. For the mid-range temperature gradient (100 mV V_{thev}), the min-max P_{in} range is $\sim 6-500\ \mu$W. In the ideal 100% EH-PMU efficiency scenario, these P_{in} values translate to a CL-LDO I_L range of about 4–300 μA @ 1.6 V V_{LDO}. The Bode plot of the loop gain is shown in Fig. 10 for a C_L of 10 pF and I_L of 4 μA, 300 μA and 1 mA. For the target I_L values, the UGF varies from 480–870 kHz and the PM is better than 48° in the worst stability case, proving that the adopted frequency compensation resulting from the auxiliary circuit is suitable for this application. In the out-of-range I_L case of 1 mA, the UGF is reduced due to the action of ω_{pST3}, but the PM is 99° and the loop is still stable.

D. CL-LDO PSR

The PSR small signal model of the proposed CL-LDO is shown in Fig. 11. Unlike the small signal representation for the loop gain in Fig. 9, for PSR-purposes transistor $\mathrm{M_{CG}}$ is directly on the input signal path to the output (V_{LDO}). As a result, $\mathrm{M_{CG}}$ implements a common-gate stage whose output is AC-coupled (via C_C) to a load formed by the series $R_Z C_Z$ circuit and the gate of $\mathrm{M_P}$. In the model of Fig. 11, the EA is represented as

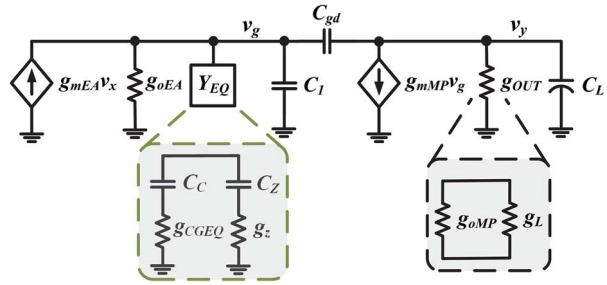

Fig. 9. Small signal model to analyze stability in the proposed CL-LDO.

TABLE I
PROPOSED CL-LDO LOOP POLES AND ZEROS

ZEROS	POLES
$\omega_{zEQ1} \approx \frac{g_{CGEQ}}{C_C}$	$\omega_{pST1} \approx \omega_{zEQ1}\frac{g_{oEA}}{g_{oEA}+g_{CGEQ}}$
$\omega_{zEQ2} \approx \frac{g_Z}{C_Z}$	$\omega_{pST2} \approx \omega_{zEQ2}\frac{g_{oEA}+g_{CGEA}}{g_Z+g_{CGEA}}$
$\omega_{z3} \approx \frac{g_{mMP}}{C_{gd}}$	$\omega_{pST3} \approx \frac{g_{OUT}(g_Z+g_{CGEQ})}{g_{mMP}C_{gd}+(g_Z+g_{CGEQ})C_L}$
--	$\omega_{pST4} \approx \frac{g_{mMP}C_{gd}+(g_Z+g_{CGEQ})C_L}{C_L(C_1+C_{gd})+C_1C_{gd}}$

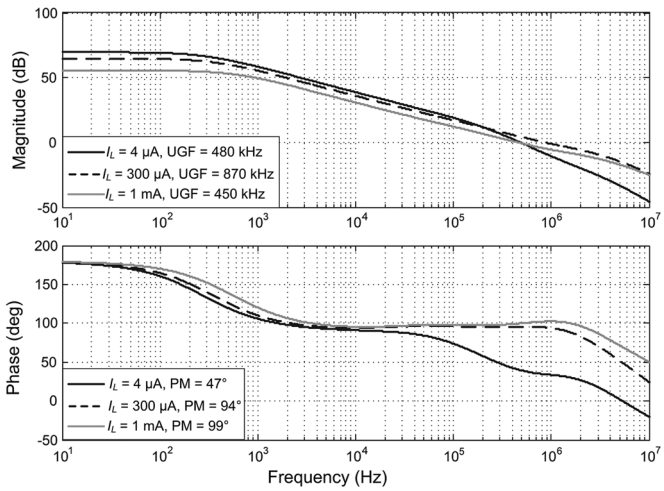

Fig. 10. CL-LDO loop gain for different I_L values (postlayout simulation).

in [33], [34]. Conductances g_1, g_2 and g_{m1}, and current source I model the used Type-A EA [34] ($\mathrm{M_1} - \mathrm{M_2}$ in Fig. 8). Except for g_{mCG} ($\mathrm{M_{CG}}$ transconductance) and g_{oCG} and g_{ocm} (output conductances of $\mathrm{M_{CG}}$ and current mirror $\mathrm{I_{CG}}$ in Fig. 8, respectively) all the variables are as previously defined. It can be shown that the PSR of the Fig. 11 model contains a total of four zeros and four poles, but more importantly, the PSR expression can be arranged as (18). (See equation at the bottom of the page.)

Under the same *a*)–*d*) assumptions of Section IV-C, the location of the poles of (18) can be approximated as shown in Table II. Note that the four poles ω_{pN1-4} are real and exist in

$$PSR_{NOTCH}(s) \approx \frac{1}{A_{EA}A_{MP}} \frac{(s/\omega_{zN1}+1)\left(s^2+2\zeta\omega_{No}+\omega_{No}^2\right)(s/\omega_{zN4}+1)}{(s/\omega_{pN1}+1)(s/\omega_{pN2}+1)(s/\omega_{pN3}+1)(s/\omega_{pN4}+1)} \tag{18}$$

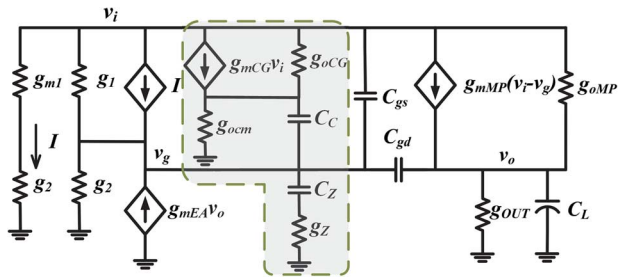

Fig. 11. Small signal model to analyze PSR in the proposed CL-LDO.

TABLE II
PROPOSED CL-LDO PSR POLES AND ZEROS

ZEROS/NOTCH/ζ	POLES
$\omega_{zN1} \approx \frac{g_{oEA}}{A_{MP}A_{CG}C_C}$	$\omega_{pN1} \approx \frac{g_{oCG}}{C_C}$
$\omega_{No}{}^2 \approx \frac{g_Z g_{mcg}}{2C_Z C_{gd}}$	$\omega_{pN2} \approx \frac{g_Z}{C_Z}$
$\zeta \approx \frac{C_Z g_{mcg}}{8 g_Z C_{gs}}$	$\omega_{pN3} \approx \frac{g_{mEA}}{C_{gd}}$
$\omega_{zN4} \approx \frac{g_{mMP}}{C_{gs}}$	$\omega_{pN4} \approx \frac{g_{mMP}C_{gd}}{(C_L+C_{gd})(C_{gs}+C_{gd})}$

the LHP. However, of particular interest is the location of the zeros since, as previously discussed, the PSR degradation onset occurs at the location of the most dominant zero in the PSR (ω_{zN1}), but also any notch-filter-like behavior will stem from the characteristics of the zeros. While the location of ω_{zN1} can be controlled with C_C, it is fair to assume this is the dominant zero due to the presence of A_{MP} and A_{CG} ($\mathrm{M_{CG}}$ gain) in the ω_{zN1} expression. Also in Table II, ω_{zN4} can be safely regarded as a high-frequency zero since it is dependent on small parasitic capacitance C_{gs} (due to small $\mathrm{M_P}$). More relevant for the operation of the overall EH-PMU is the interaction of ω_{zN2-3}. Although these two zeros do not directly appear in (18), their effect is captured in the form of a second order equation in the numerator of (18). It can be shown that if the damping factor of the second order equation (ζ, in Table II) is smaller than 1, ω_{zN2} and ω_{zN3} generate a complex pair with non-zero real component, producing a notch at the frequency ω_{No}.

Assuming a fixed, small C_{gd} (a few pF due to small $\mathrm{M_P}$), the notch can be tuned via g_z, g_{mcg} and C_z. Furthermore, R_z ($1/g_z$,) is implemented using a high-R resistor with a total value of $\sim$ 300 kΩ, leaving g_{mcg} and C_z as the notch-tuning elements. To account for potential parameter variations, a programmable capacitor bank is used to realize C_z. A 4-bit external control signal is used to choose between 16 different C_z values (for a maximum of $\sim$40 pF). A second degree of programmability is added by externally setting $\mathrm{V_{CG}}$ to vary g_{mcg} as needed. For assumption a) in Section IV-C to remain valid, a second 4-bit capacitor bank for C_C is also implemented and set accordingly (for a maximum of $\sim$80 pF). The need for the C_C bank was first highlighted in [35], where a more complex expression for ω_{No} is presented since assumption a) is not made. According to the ω_{No} expression, a combination of the aforementioned values requires a g_{mcg} smaller than 1 μS to produce a notch within the target f_{sw} range. Such g_{mcg} values can be obtained with less than 1 μA $\mathrm{I_{CG}}$ (Fig. 8), which complies with the low power requirement of the CL-LDO.

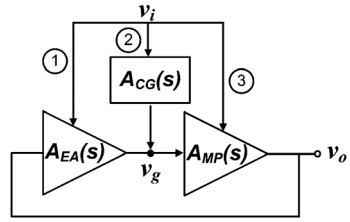

Fig. 12. Simplified PSR block diagram for the proposed CL-LDO.

Although the PSR is inversely proportional to the loop gain [34], notice that the zeros in Table II (PSR) do not directly correspond to the poles in Table I (loop gain) and vice versa. This property of the proposed CL-LDO allows to have a set of complex zeros in the PSR transfer function without complex poles in the loop gain. To understand the beneficial pole-zero disparity between (17) and (18), consider Fig. 12 where a simplified PSR block diagram of the CL-LDO is shown. $A_{EA}(s)$, $A_{MP}(s)$ and $A_{CG}(s)$ represent the frequency-dependent gain of the EA, $\mathrm{M_P}$ and auxiliary circuit (dashed line box in Fig. 11), respectively. Paths 1, 2 and 3 represent the v_i-to-v_o noise paths affecting the PSR. Assuming large loop gain, path 1 suffers large attenuation at v_o, thus only paths 2 and 3 are considered in this conceptual analysis

Solving for v_o/v_i in Fig. 12 yields (19), where $A_{MPDP}(s)$ is the direct path from v_i-to-v_o due to g_{mMP} and g_{oMP}. Condensing the effects of the auxiliary circuit in $A_{CG}(s)$, it can be shown that (19) has four poles and four zeros if the individual $A_{EA}(s)$, $A_{MP}(s)$, $A_{CG}(s)$, and $A_{MPDP}(s)$ have: one-pole (at v_g); one-pole (at v_o) and one-zero (due to C_{gs} and C_{gd}); two poles and two zeros; and one pole (at v_o), respectively. Furthermore, (19) approximates (18) under the assumptions made and introduces a notch in the PSR without compromising the loop stability. This is due to $A_{CG}(s)$ being purely passive for stability purposes (Fig. 9) but active for PSR purposes (Fig. 11), thus (17) and (18) experience different effects from $A_{CG}(s)$.

$$\frac{v_o}{v_i} = PSR_{NOTCH} = \frac{A_{CG}(s)A_{MP}(s) + A_{MPDP}(s)}{1 + A_{EA}(s)A_{MP}(s)} \quad (19)$$

V. SENSE-AND-CONTROL LOOP

An off-chip Sense-and-Control (SaC) loop was implemented using the low power, 8-bit Microchip's microcontroller PIC16F1783. After the BC has reached MPP and locked into a nearly constant f_{sw} (for a given load current), the PIC determines the average f_{sw} ($\overline{f_{sw}}$) and uses this value to map it on a look-up table (LUT). The LUT contains the appropriate control signals for the CL-LDO such that the notch is placed at f_{sw} for maximum voltage ripple suppression. For every $\overline{f_{sw}}$ of interest, the LUT contains two calibration entries, one for the analog $\mathrm{V_{CG}}$ value (generated through the PIC's 8-bit digital-to-analog converter with a resolution better than 4 mV in a 0–1 V range), and a second entry with the proper 8-bit digital word to tune the C_C and C_Z capacitor banks (4 bits per bank).

Once the tuning is completed, the CL-LDO notch is placed in the vicinity of $\overline{f_{sw}}$, effectively rejecting the undesired BC switching noise. The CL-LDO notch can be tuned as often as $N_P/\min(f_{sw})$ seconds (N_P is the number of f_{sw}-periods used to estimate $\overline{f_{sw}}$). In our prototype, a high PSR is obtained by accurately measuring $\overline{f_{sw}}$ (N_P of 100), which allows for optimum notch placement. Since slow load changing conditions

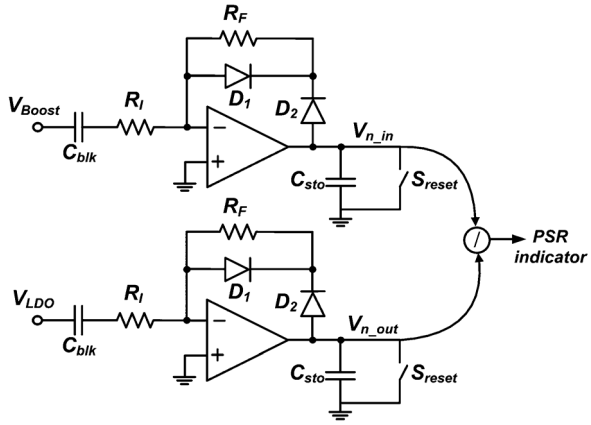

Fig. 13. PSR measurement circuit.

are assumed, the notch tuning is performed with a 1-second interval. Note that a slow update rate avoids unnecessary power consumption on the external PIC (70 μA in this case). While our proof-of-concept uses an off-chip SaC loop, notice that an on-chip finite-state-machine (FSM) could implement the SaC loop. Within the FSM, a synchronous counter could be used to measure f_{sw} and directly tune the banks of capacitors with its final count. Similarly, this count (binary word) could be used in a basic digital-to-analog converter to generate the analog $\mathrm{V_{CG}}$ value for notch calibration purposes.

A. Look-Up-Table Contents Optimization

While the LUT can be filled using data obtained at the design and simulation stage, such calibration entries might require small adjustments to compensate for potential process variations. A straightforward way to verify the adequacy of the initial calibration estimates to tune a notch at frequencies $f_{sw}(0) \ldots f_{sw}(n)$ is with a one-time CL-LDO PSR characterization using said estimates and updating the LUT as necessary. Alternatively, it is possible to perform a foreground, automatic PSR estimation to determine if the initial calibration estimates provide suitable notch control and noise rejection. If the PSR is not satisfactory for a particular $f_{sw}(k)$, the calibration entry for $f_{sw}(k)$ is then adjusted accordingly and updated in the LUT.

The circuit in Fig. 13 can be used for PSR estimation. In this approach, a peak detector based on signal amplification (R_F/R_I) and partial rectification [36] is employed to estimate the supply noise at the CL-LDO input and output. Before the measurement, the initial calibration estimates for a notch at $f_{sw}(k)$ are used. After the measurement is completed, the PIC used for the SaC loop can sample the results at $V_{n\_in,out}$ and process them to obtain a PSR indicator. If the PSR indicator is satisfactory, the calibration entries for $f_{sw}(k)$ are confirmed and marked as reliable in the LUT. Otherwise, if the initial calibration estimates are off after fabrication (resulting in insufficient PSR due to imperfect notch tuning), the PIC runs a search algorithm (Fig. 14) to find a new calibration estimate that provides a notch (and higher PSR) at $f_{sw}(k)$. Once the new calibration entries are determined, the LUT is updated. This process is repeated for every f_{sw} of interest.

Note that the suggested, on-board PSR measurement method can be seamlessly integrated, and while the amplifiers required might consume additional power, the power overhead is experienced only during a short period of time required for the LUT optimization, after which both amplifiers can be shut-down.

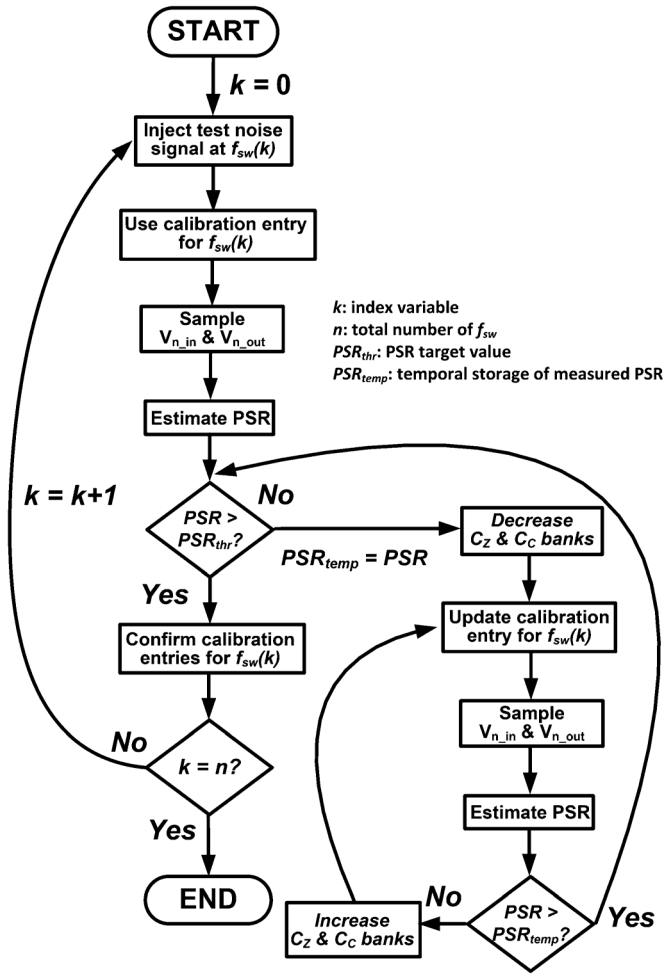

Fig. 14. LUT optimization algorithm.

Furthermore, additional, more complex techniques to measure PSR on-chip can be used [37].

VI. MEASUREMENTS

The EH-PMU was designed and fabricated in 0.5 μm CMOS process. Fig. 15 presents the testbench setup and die microphotograph, with an active area of 0.93 mm^2.

Resistance matching between the EH-PMU front-end (BC) was performed by varying the series impedance of a 3 $\times$ 3 TEG array composed of MPG-DG655 modules. While the details of the array reconfiguration are out of the scope of this work, a total of 42 switches [10] enable any possible parallel/series combination of the units in the array. These interconnecting switches can be controlled by the same PIC implementing the SaC loop. By monitoring the output of an off-the-shelf temperature sensor, the PIC can decide the state of the interconnecting switches and reconfigure the array.

Resistance variation step was performed from 19 Ω to 1.53 kΩ in order to make sure stability is correctly achieved under drastic loop parameter variations. Fig. 16 shows that the correct MPP is achieved of 100 mV for both TEG resistance equivalencies. Broader ranges of matching can be accomplished via a tradeoff between f_{sw} and L_{in} value.

The BC and CL-LDO outputs are shown in Fig. 17 (upper and lower signals, respectively) for a load current of 10 μA. Before the notch is introduced (Fig. 17(a)) the CL-LDO output shows an attenuation of the switching noise of $\sim$6 dB. However, when

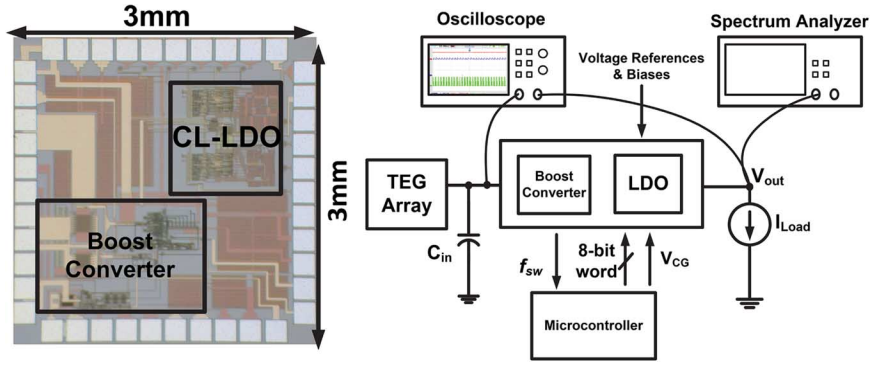

Fig. 15. Die microphotograph and testbench setup.

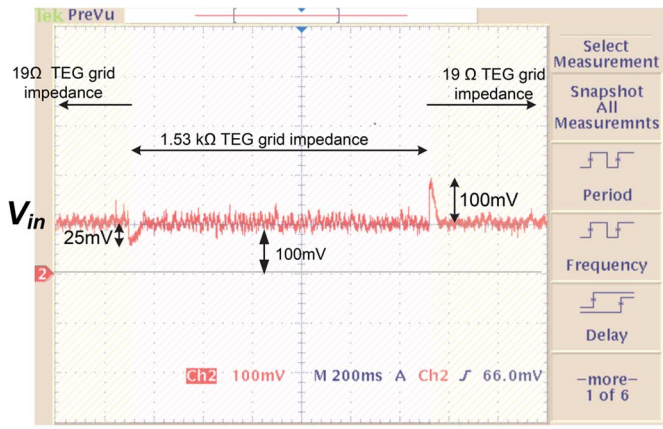

Fig. 16. Correct MPPT is achieved through PFM control loop.

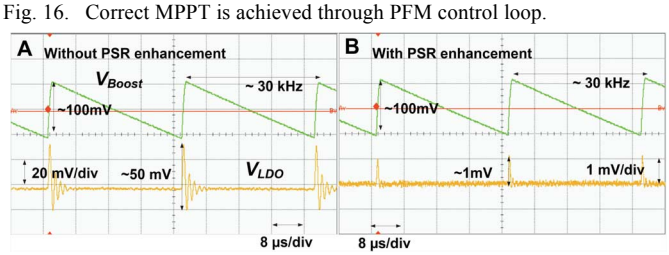

Fig. 17. Switching noise suppression from CL-LDO.

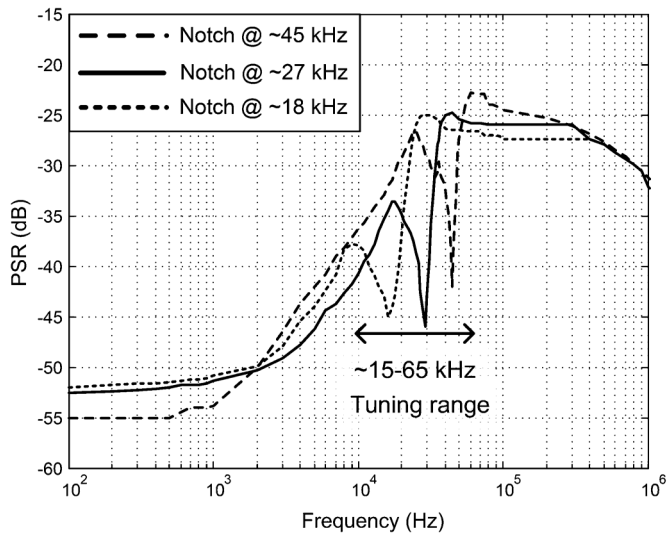

Fig. 18. CL-LDO measured PSR with notch tuning range of 15–65 kHz.

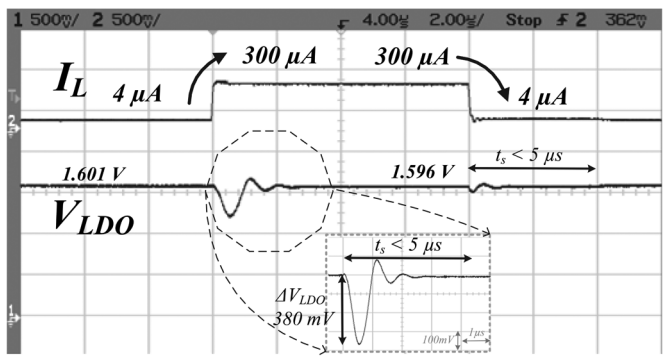

Fig. 19. CL-LDO load transient response to a 4 μA to 300 μA I_L step.

the CL-LDO tuning is completed and the notch in the PSR has been properly placed (Fig. 17(b)), the attenuation reaches 40 dB.

The measured CL-LDO PSR is shown in Fig. 18 for three combinations of C_C bank, C_Z bank and g_{mcg}. The total range over which the notch can be programmed is roughly between 15 kHz to 65 kHz. While the BC might switch at $f_{sw} < 15$ kHz, the intrinsic, low-frequency PSR of the CL-LDO can successfully attenuate the ripple at these f_{sw} values. Although the optimum ripple rejection is achieved when the notch is centered at f_{sw}, in the event of slight f_{sw} variations ($f_{sw}^* = f_{sw} + \Delta f_{sw}$) after the notch has been tuned, the switching noise at f_{sw}^* will still experience attenuation due to the steep skirt around the center notch frequency (e.g., a notch centered at 27 kHz has 36 dB suppression at 32 kHz, this is Δf_{sw} of 18.5%).

From the CL-LDO load transient response to a 4–300 μA I_L step (Fig. 19), the measured load regulation is 17 mV/mA. Interestingly, even though the modest bandwidth of the CL-LDO results in a settling time of 5 μs, this recovery interval represents less than 3% of the total Rx-to-Tx or Tx-to-Rx turnaround time in IEEE 802.15.4 standard-compliant devices [38]. Thus, an ultra-low power radio powered by the proposed EH-PMU could afford a frequency synthesizer with a settling time of nearly 187 μs and still meet the IEEE 802.15.4 standard (which specifies a turnaround time of 12 symbol periods or 192 μs @ 62.5 ksymbol/s).

Influenced by the small on-chip C_L and low bias current available to drive the gate capacitance of M_P, the Fig. 19 measurement also shows that the voltage undershoot (ΔV_{LDO}) departs up to 380 mV from the nominal V_{LDO}. Despite its short duration, there might be load circuitry for which this V_{LDO} undershoot could cause undesired operation. When necessary, it is possible to combine the proposed CL-LDO with voltage spike-triggered dynamic biasing techniques [39] to reduce the magnitude of the voltage dip, at the expense of increased current consumption.

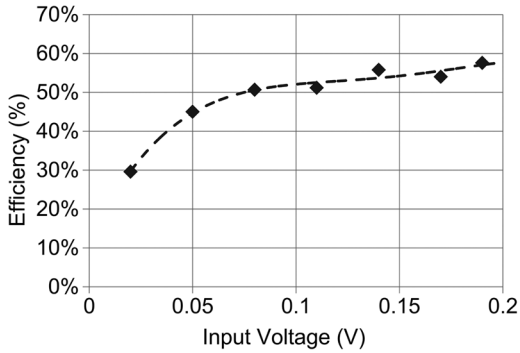

Fig. 20. End-to-end system efficiency.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	[8]	[11]	[12]	[13]	This work
Input voltage	0.38-3.3 V	20-160 mV	30 mV	1 V	50-250 mV
Output voltage	Multiple	1.88 V	Multiple	1.8 V	1.6 V
Quiescent	1.2 µW	-	-	-	3.6 µW
MPPT	✓	✓	✗	✗	✓
Max. Efficiency	92%	58%	38%	88%	57.57%
PSR	-	-	-	-	**-40 dB @f_{sw}**
Topology	Buck +Boost	Buck +Boost	Rectifier +Boost+LDO	Buck +Boost	Boost +LDO
Process	0.13 µm	0.35 µm	0.13 µm	0.35 µm	0.5 µm

As shown in Fig. 20, the overall maximum system end-to-end efficiency was measured at 57.57% (V_{Boost} of 1.8 V and V_{LDO} of 1.6 V) for input (V_{thev}) voltages of 140 and 190 mV. The total EH-PMU power consumption is 3.6 μW (1 μW in the BC and 2.6 μW in the CL-LDO). Table III presents the overall system performance for the proposed EH-PMU compared to state-of-the-art systems. The total power consumption does not take into account the power consumed by the microcontroller SaC implementation.

VII. CONCLUSION

An energy harvesting power management unit (EH-PMU) based on a combination of a boost converter and a capacitorless LDO (CL-LDO) with high efficiency and enhanced noise suppression has been presented. The boost converter delivers MPPT from an array of TEG devices through a frequency modulation scheme. The matching scheme is capable of correctly match from 19 Ω to 1.53 kΩs. The CL-LDO includes an auxiliary circuit for enhanced PSR. A notch at the switching frequency of the boost converter is added in the CL-LDO PSR transfer function. The EH-PMU employs a Sense-and-Control loop to send the switching frequency information from the boost converter to the CL-LDO to correctly shift the notch to the switching frequency. End-to-end system efficiency of 57.57% is achieved by the EH-PMU, and 40 dB noise suppression at the switching frequency is measured. The proposed power consumption/power delivering capabilities of the EH-PMU are suitable for energy harvesting assisted devices in the 100 s of μW range.

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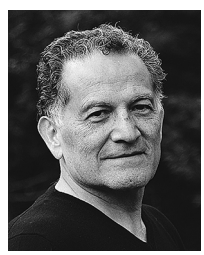

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