An Ultra-Low Power Power Management Unit with -40dB Switching-Noise-Suppression for a 3x3 Thermoelectric Generator Array with 57% Maximum End-to-End Efficiency

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***Abstract*— A high efficiency, dynamically adaptable Power Management Unit (PMU) consuming less than 3µW, for an energy harvesting system based on a thermoelectric generator (TEG) array is presented. A boost converter with a cascaded low drop-out (LDO) voltage regulator comprises the proposed PMU. The design approach allows the PMU to reach maximum power transfer by matching the TEG's dynamic series resistance and simultaneously provide adaptive switching noise rejection. The boost converter's switching frequency (f_{sw}) is tracked via a background sense-and-control loop which modifies the LDO's power supply rejection (PSR) characteristics to place a notch around the average f_{sw}. Overall system efficiency is better than 57%, and PSR of -40dB at f_{sw} are achieved. The total active area is 0.93 mm^2 in 0.5 µm CMOS.**

Keywords—MPPT, DC-DC converter, Linear regulator, LDO, energy harvesting, TEG

I. INTRODUCTION

With the move towards ever more energy efficient wireless sensors, power consumption becomes a commodity which must be managed efficiently to allow long battery-operated periods. Harvesting energy from alternative sources provides battery-powered systems the possibility to relax requirements on power consumption for long up-time operation. From photovoltaic, biological, kinetic, radio-frequency, or thermal sources [1-5], power can be effectively and inexpensively foraged.

Recently, several approaches have showcased what energy harvesting power management units (PMU) are capable of performing [1, 6]. However, [6] does not perform maximum power point tracking (MPPT) for a thermoelectric generator (TEG) device, severely limiting the PMU efficiency. The PMU in [1] achieves both MPPT and load regulation, but time-interleaves the inductor between multiple inputs/output, limiting its current delivery capabilities for the load.

This paper presents a solution tackling MPPT, load regulation, and enhanced power supply rejection (PSR) for an array of TEG modules. Fig. 1 depicts the overall system structure for the proposed PMU. From Fig.1, it can be observed that the PMU is divided into two main blocks: A boost DC-DC switching converter, and a low dropout voltage (LDO) regulator. The boost converter has a dual purpose: It brings the reduced TEG output voltage into usable -higher- voltage levels (at V_{Boost} in Fig. 1), and enables maximum power extraction from the TEG array. The latter is achieved using a closed-loop pulse frequency modulation (PFM) scheme to dynamically match the TEG array and boost converter's source and input resistances, respectively.

For the regulation stage, an LDO is cascaded with the boost converter. The LDO in Fig. 1 provides voltage regulation and adaptive-programmable supply noise suppression at the PMU output node. To provide the PMU with superior PSR, the LDO PSR characteristics are modified to introduce a notch with programmable location in its supply-noise-to-output transfer function (TF).

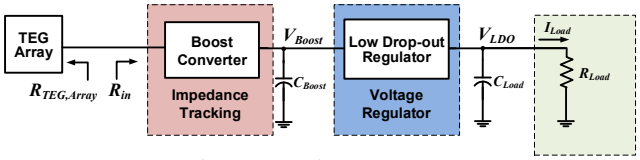

Fig. 1. Proposed PMU structure.

The paper is organized as follows: Section II offers a system level description of the implementation of the TEG array along with the system architecture description. Section III presents the configurations for both the boost converter and LDO. Section IV presents experimental results and finally, Section V concludes this paper.

II. POWER MANAGEMENT UNIT FOR TEG ARRAYS

The proposed PMU implements a reconfigurable 3 by 3 TEG module array. This is done to take full advantage of the higher power available under multiple temperature gradient scenarios [7]. A first order model for the TEG array is shown in Fig. 2. . The output voltage of the array, $V_{TEG,Array}$, is modeled by a temperature-gradient-dependent voltage source with a series, variable source resistance, $R_{TEG,Array}$, which depends on the effective electrical internal resistance of the TEG module array.

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As discussed in [7], $R_{TEG,Array}$ will change whenever the TEG array experiences a reconnection , dependent on power availability. From Fig. 1, it is the boost converter's capability to dynamically match its input resistance, R_{in} to $R_{TEG,Array}$, which allows the PMU to achieve MPPT.

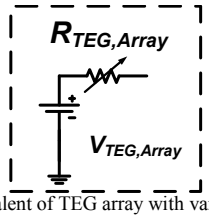

Fig. 2. Electrical equivalent of TEG array with variable source resistance.

The characterized TEG module for the array was based off of the Micropelt TEG MPG-D655 [8]; where the equivalent source resistance for a single module is ~170 Ω. For a 3 by 3 array the best/worst case power conditions would be when the entire array is connected in a parallel or series fashion, respectively. A temperature gradient of approximately from 0.23°C to 2.1°C is assumed for the TEG array for series and parallel connection settings. This leads to an open circuit (Thevenin) voltage of approximately 200 mV, and equivalent source resistance ranging from 19 Ω to 1.53 kΩs, where the maximum power point (MPP) is ~100 mV.

The implemented PMU is capable of operating at MPP for the aforementioned resistance value scenarios, while simultaneously suppressing switching noise at the output. Section III describes how both features are achieved under ultra-low power operation.

III. Boost Converter and Low Drop-out Regulator

Fig. 3 shows the overall system architecture with both the boost converter and LDO highlighted. The system delivers a 1.8 V value at V_{Boost} and 1.6 V value at V_{LDO}. The particulars of each block are detailed in the following subsections.

A. Boost Converter

The architecture of the boost converter presented in this project closely follows the design parameters set out in [7], both for efficiency improvement, through a Zero Current Switching (ZCS) scheme, and MPPT implementation.

For the range of resistances to match, the boost converter must effectively be capable of achieving these same values for R_{in}, which (as shown in [7]) can be controlled through the switching frequency (1).

$$R_{in} = \frac{2\,L_{in}\,f_{sw}}{D_{NMOS}^2} = 8\,L_{in}\,f_{sw} \qquad (1)$$

where L_{in} is the inductor value, f_{sw} the switching frequency and D_{NMOS} is the duty cycle for the NMOS switch (Fig. 3). For linear control of R_{in}, the D_{NMOS} was set to 50%.

Since power consumption is a critical factor to minimize in any energy harvesting system, an approach to decrease the dynamic power consumption by reducing f_{sw} to a minimum. A value of 5mH was selected for L_{in}, allowing for an f_{sw} of 33.5 kHz and ~0.5 kHz for the targeted $R_{TEG,Array}$ values.

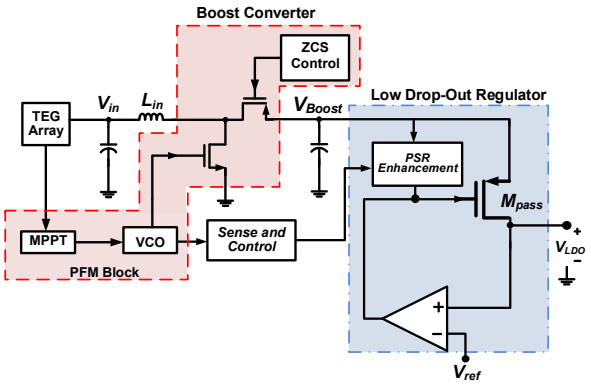

Fig. 3. Proposed system architecture for PMU.

Fig. 4 shows the block diagram of the PFM block, which performs the MPPT operation. The tracking scheme employed compares the input voltage, V_{in}, with half the TEG array's Thevenin voltage ($V_{TEG,Array}/2$). The result of this comparison is used by a voltage controlled oscillator (VCO) to modulate f_{sw} until a $R_{TEG,Array}$ and R_{in} match is achieved. The resistive matching point corresponds to a V_{in} and $V_{TEG,Array}/2$ matching, thus enabling the MPP condition.

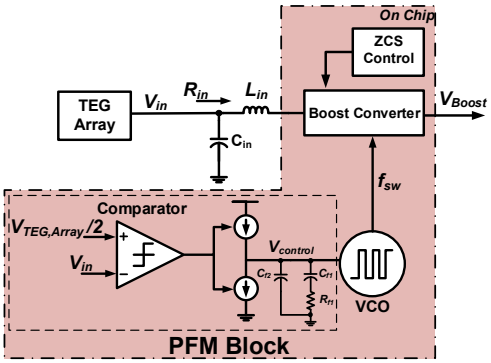

Fig. 4. Pulse Frequency Modulation control loop to achieve MPP.

The $V_{control}$ node set by a current steering charge pump and a passive filter. The critical parameter for improved loop performance lies in the passive filter (C_{f1}, C_{f2}, and R_{f2}), which was designed to increase loop bandwidth and assure an appropriate phase margin for both TEG array resistance scenarios.

B. Low Drop-out Regulator

As previously stated in the boost converter design, power consumption of the PMU is a critical factor which must be reduced. If it can be afforded, a small power investment in an LDO provides the system with a steady, regulated output voltage and improved PSR.

The core of the LDO used in the proposed PMU (Fig. 3) is based on an error amplifier and pass transistor topology [9]. The error amplifier (EA) is an NMOS-input differential pair, and the pass device (M_{PASS}) is a PMOS FET. Using an NMOS-input EA and an adequate voltage reference (V_{ref}), the feedback network, comprised of two feedback resistors [9], can be eliminated; reducing the LDO current consumption and silicon

area. Unfortunately, the PSR the aforementioned LDO would be limited by the loop DC gain and the modest bandwidth that can be achieved with reduced EA bias current.

Extending the PSR frequency range of on-chip LDOs entails a wide bandwidth, power hungry EA. However, the localized nature of the supply noise in the proposed PMU can be focus on maximizing the LDO PSR at f_{sw}. One way to obtain an LDO with such PSR characteristic is to provide the LDO PSR TF with a notch-like stop band at f_{sw}. To implement a notch in the LDO PSR TF in a power-efficient way, one can take advantage of the LDO loop property to reflect the (complex) poles at the gate of the EA into (complex) zeros in its PSR TF. Note that in order to preserve the LDO loop stability, the path or circuit used to add such zeros to the LDO PSR TF should have minimum effect on the regulating loop. An LDO and auxiliary circuit that meet these criteria are proposed in Fig. 5.

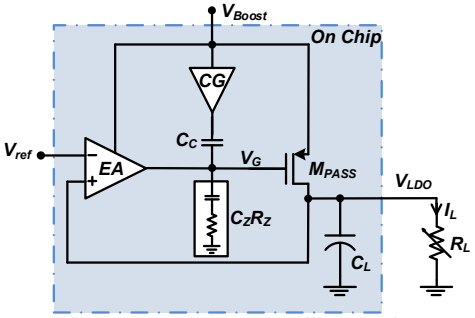

Fig. 5. Proposed LDO and auxiliary circuit.

In Fig. 5, a PMOS-input common-gate (CG) amplifier is AC-coupled via capacitor C_C to node V_G. A passive series RC network C_zR_z along with CG, are used to introduce the required complex conjugate pair. Both C_c and C_z are controlled through an 8-bit control word to modify the net RC network value. It should be noted that for small-signal loop-stability purposes, both the CG internal bias and V_{Boost} voltages are AC grounded. Thus, CG has no effect in the regulating loop. Furthermore, due to the C_C coupling action, the M_{PASS} bias point is determined only by the EA. This avoids disturbing the LDO DC operation.

Considering the M_{PASS} gate-source (C_{gs}), gate-drain (C_{gd}) and load capacitances (C_L), the loop *stability* TF has four LHP poles and three zeros. Fortunately, it is possible to perform near pole-zero cancellations between the closely spaced real poles and zeros added by C_C, C_Z and R_Z in Fig. 5; thus, allowing the LDO loop to be stabilized as in the two poles, one zero case.

Similarly, the PSR TF contains a total of four real and stable poles and four zeros. By properly selecting the values of C_C and the C_ZR_Z network, it is possible to have two real LHP and two complex zeros to introduce a notch in the PSR TF. Furthermore, tuning Cc, Cz and gm_{cg} (CG transconductance), the frequency of the notch can be programed over the range of interest (10-30 kHz) before the complex zeros become real. The simplified expression for the notch location becomes:

$$\omega_o^2 = \frac{g_z gm_{Mp_{ass}}\left(C_C gm_{cg} - C_Z g_{cg}\right)}{C_C C_{gs}\left(C_{gd} g_Z + C_Z g_{Mp_{ass}}\right) + C_Z C_{gd}\left(C_{gs} g_{cg} + C_C g_{Mp_{ass}}\right)}^{1} \quad (2)$$

[1]In (2), g_z and g_{cg} represent the equivalent R_Z and CG conductances, respectively.

In summary, the notch frequency can be tuned accordingly to follow f_{sw} and constantly provide improved PSR at the PMU output voltage.

C. Sense-and-control (SaC)

In order to take full advantage of the programmable LDO PSR characteristics and to provide a sound proof-of-concept, a sense-and-control (SaC) loop was implemented using an off-chip, low power microcontroller (PIC16F1783). The SaC loop measures the steady state, average f_{sw} ($\overline{f_{sw}}$) and uses an internal, pre-loaded look-up table to map $\overline{f_{sw}}$ to the corresponding 8-bit control word to be applied to the LDO control port (which tunes the value of C_C and C_Z). As part of the fine tuning, an analog voltage is also generated from the microcontroller to set the proper value of gm_{cg}. It should be noted that this implementation could easily be integrated as part of the PMU for a self-contained solution.

IV. Experimental Results

The PMU was designed and fabricated in 0.5 µm CMOS process. Fig. 6 presents the die microphotograph of the entire system, with an active area of 0.93 mm^2.

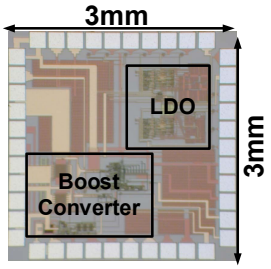

Fig. 6. Die microphotograph.

A. Maximum Power Point Tracking

Resistance matching between the PMU front-end (boost converter) was performed by varying the series impedance of a simulated 3x3 TEG array composed of a commercially available TEG module [8]. Resistance variation step was performed from 19 Ω to 1.53 kΩ in order make sure stability is correctly achieved under drastic loop parameter variations. Fig. 7 shows that the correct MPP is achieved ($V_{TEG,Array} = 200\ mV$) of 100 mV for both TEG resistance equivalencies.

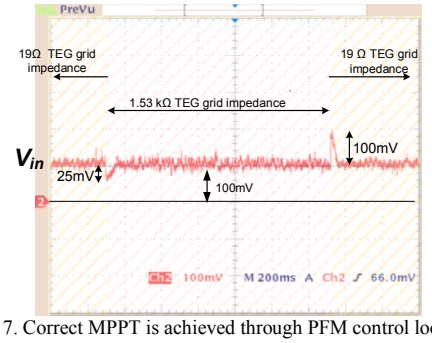

Fig. 7. Correct MPPT is achieved through PFM control loop.

Broader ranges of matching can be accomplished via a tradeoff between switching frequency and inductance value.

B. *Switching Noise suppresion*

After the boost converter has reached the maximum point for power transfer and locked into a narrow range of f_{sw} for a given load current, the SaC loop measures $\overline{f_{sw}}$ and generate the required control word and voltage for the LDO auxiliary circuit. Once the LDO tuning is completed, the notch is placed in the vicinity of $\overline{f_{sw}}$, effectively rejecting the undesired boost's switching noise. Fig. 8 shows the measured output of the boost converter and the LDO, upper and lower signals, respectively. In Fig. 8A, an attenuation of the boost's switching noise at the LDO output of only about 6dB is observed before the notch is introduced. However, when the LDO tuning is completed and the notch in the PSR TF has been properly placed (Fig. 8B), the attenuation reaches 40dB, demonstrating the LDO superior PSR performance.

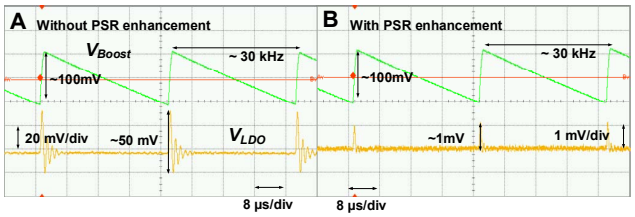

Fig. 8. Switching noise suppression from LDO.

C. *Efficiency and Performance Summary*

Overall maximum system end-to-end efficiency was measured at 57.57%. For measured efficiency, V_{Boost} node was set to 1.8 V and V_{LDO} to 1.6 V.

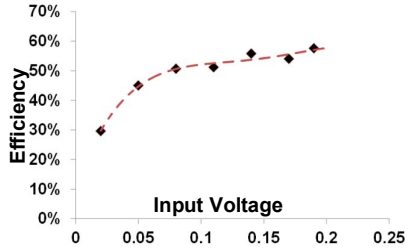

Fig. 9. End-to-end system efficiency with $P_{in} = 526\ \mu W$.

Table 1 presents the overall system performance for the proposed PMU compared to state-of-the-art systems. Power consumption for this work does not take into account the power consumed by the microcontroller SaC implementation and only considers quiescent from both the boost converter and LDO structures.

V. CONCLUSIONS

A PMU based on a combination of a boost converter and an LDO with high efficiency and enhanced noise suppression has been presented. The boost converter delivers MPPT from an array of TEG devices through a frequency modulation scheme. The matching scheme is capable of correctly match from 19 Ω to 1.53 kΩs. The LDO possesses a novel auxiliary circuit which allows for enhanced PSR via a notch at the switching frequency of the boost converter. The PMU also employs an SaC loop in order to send the switching frequency information from the boost converter to the LDO to correctly shift the notch to the switching frequency of the boost converter. End-to-end system efficiency of 57.57% is achieved by the PMU, and -40 dB noise suppression at the switching frequency is measured. The proposed power consumption/power delivering capabilities of the PMU are suitable for energy harvesting assisted devices in the 100s of μW range.

TABLE I. PERFORMANCE SUMMARY

Spec.	[1]	[6]	[5]	This work
Input voltage	20 mV-160 mV *	30 mV*	1V	50mV-250mV
Output Voltage	1.88 V	Multiple	1.8 V	1.6V
Quiescent	-	-	-	~3 µW
MPPT	Yes	No	No	Yes
Max. Efficiency	58%	38% †	88%	57.57%
PSR	-	-	-	-40 dB @ f_{sw}
Process	0.35 µm	0.13 µm	0.35 µm	0.5 µm

*For TEG
† Only for boost converter

ACKNOWLEDGMENT

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