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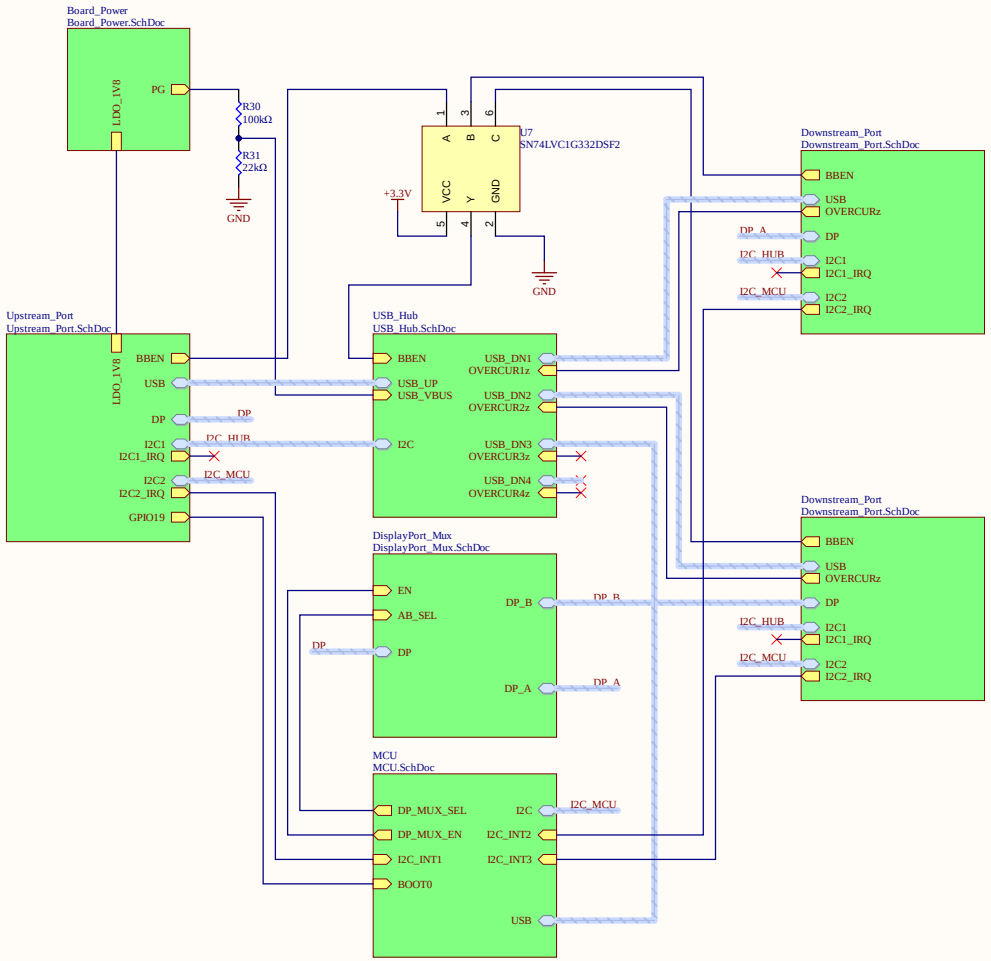

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CHK: *	
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PROJECT: Altium™

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: d529c37 [Locally Modified] | DESIGN ITEM: *

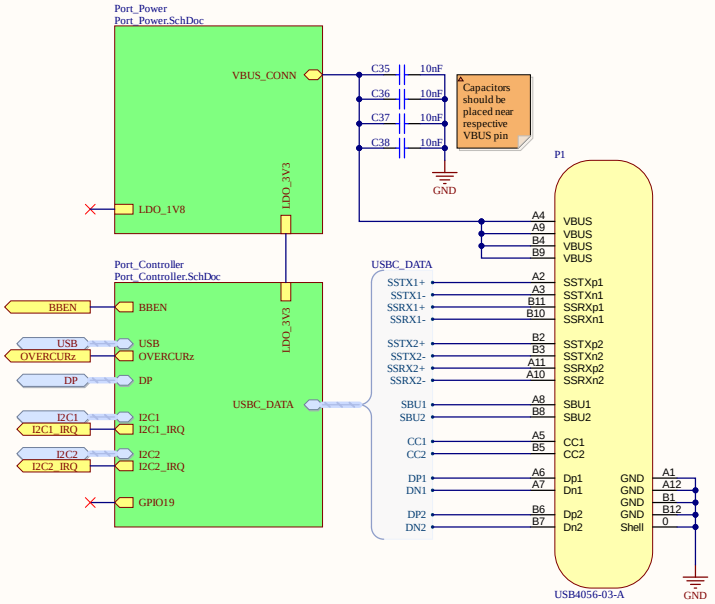
TITLE: USBC Hub

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME: Top.SchDoc | SHEET 1 OF 9

<SCH DWG NO> DWG. NO. | REV | 1 SHT.

REVISION	DESCRIPTION	DATE	APPROVED



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PROJECT

Altium

PROJECT REVISION: c7ecd1a5 DOCUMENT REVISION: c35edb01 [Locally Modified] DESIGN ITEM:

TITLE

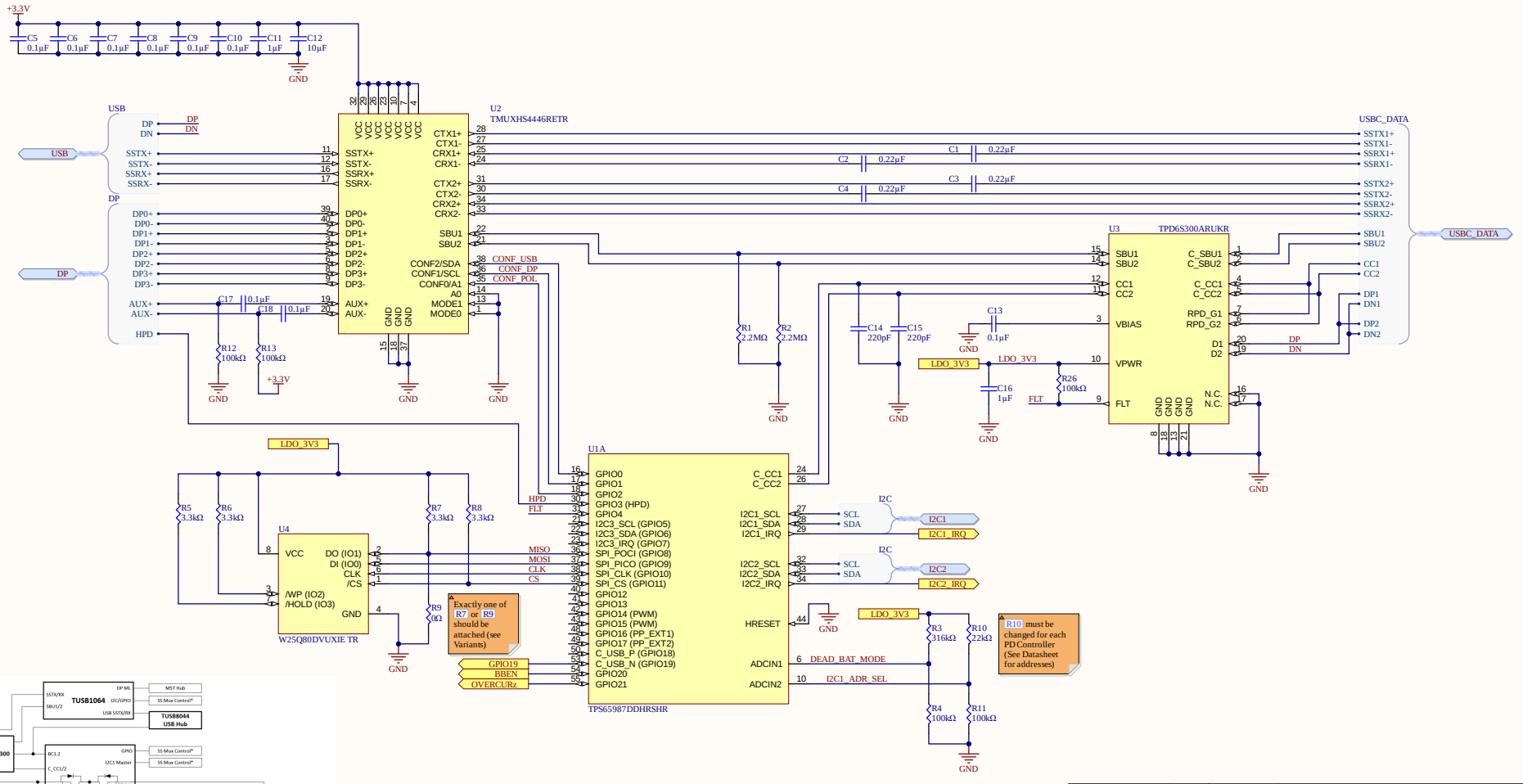
Downstream Port

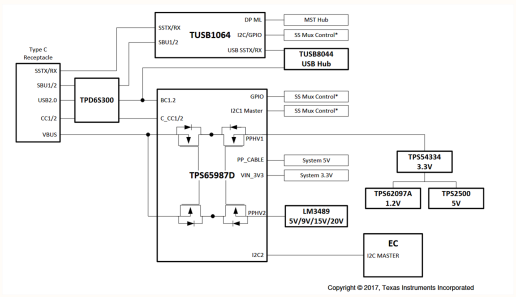
SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME Downstream_Port.SchDoc SHEET 2 OF 9

<SCH DWG NO> DWG. NO. REV 2 SHT.

REVISION	DESCRIPTION	DATE	APPROVED





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REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
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PROJECT: Altium

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: c35edb01 | DESIGN ITEM:

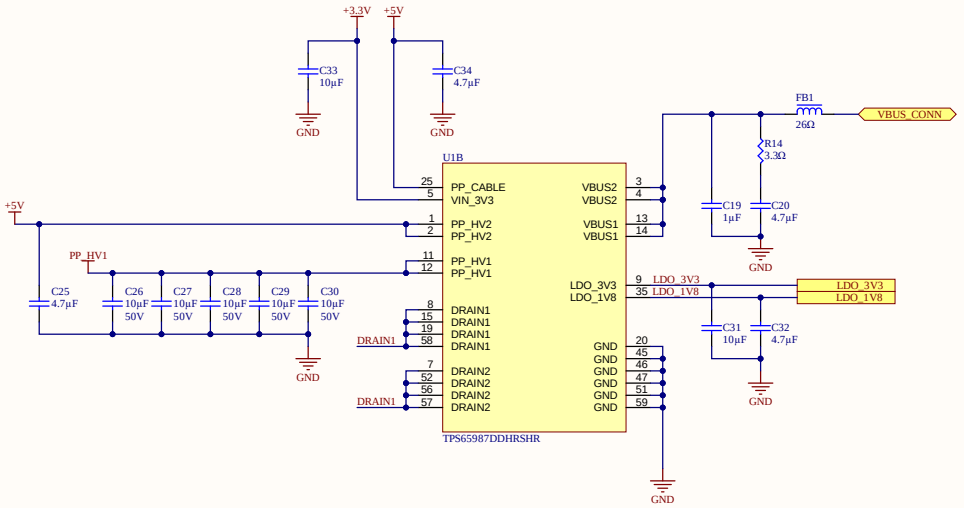
TITLE: USBC Port Controller

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME: Port_Controller.SchDoc | SHEET 3 OF 9

<SCH DWG NO> | REV 3 | SHT 3

REVISION	DESCRIPTION	DATE	APPROVED



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PROJECT

Altium™

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: 89f6a6ae [Locally Modified] | DESIGN ITEM:

TITLE

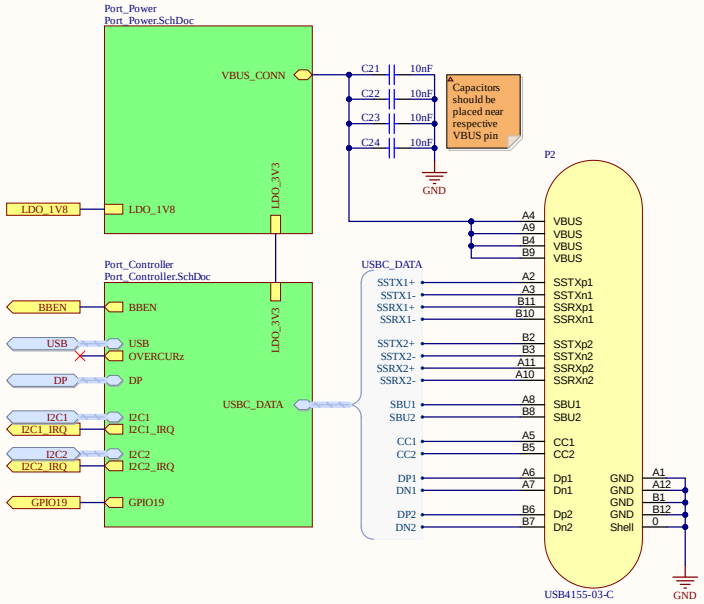
Port Power

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME Port_Power.SchDoc | SHEET 4 OF 9

<SCH DWG NO> DWG. NO. | 4 REV | SHT.

REVISION	DESCRIPTION	DATE	APPROVED



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PROJECT: Altium

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: c35edb01 [Locally Modified]

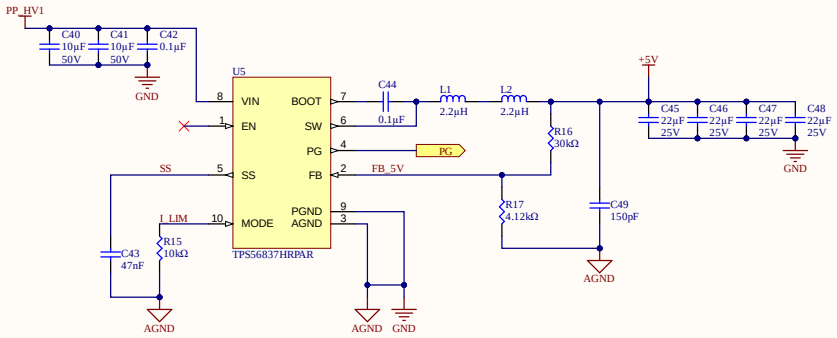
TITLE: Upstream Port

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

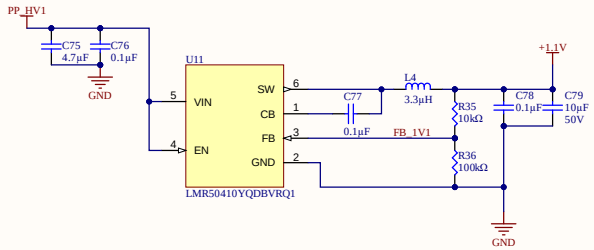
SCALE: | FILE NAME: Upstream_Port.SchDoc | SHEET 5 OF 9

REVISION	DESCRIPTION	DATE	APPROVED

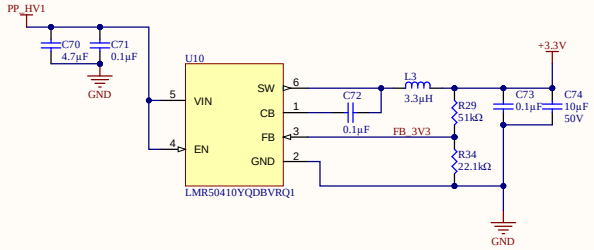
5V Buck



1.1V Buck



3.3V Buck



1.8V LDO

1.8V is supplied via integrated LDO in upstream PD Controller, LDO_1V8_3

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	

REFERENCE DOCUMENTS

BOM: <BOM DOC NO>
ASSY DWG: <ASSY DWG NO>
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PROJECT

Altium

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: c7ecd1a5 [Locally Modified] | DESIGN ITEM:

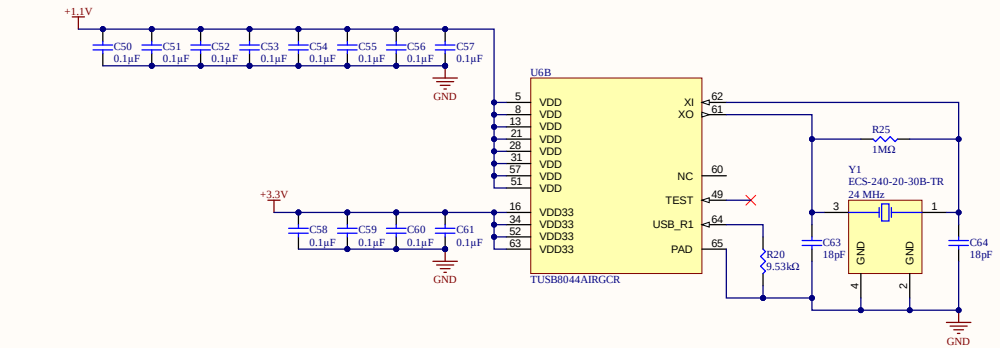
TITLE: Board Power

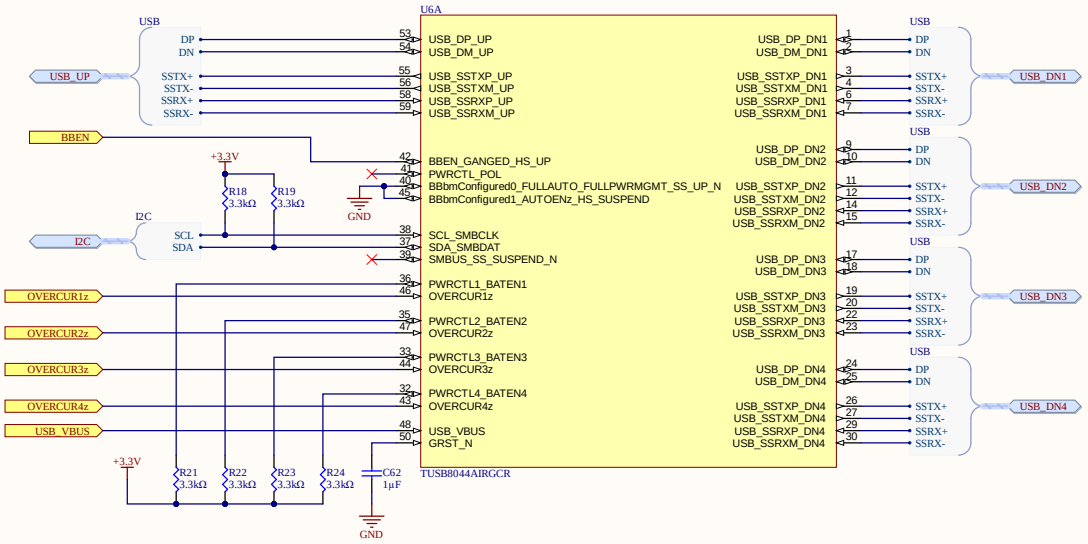
SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME: Board_Power.SchDoc | SHEET 6 OF 9

<SCH DWG NO> DWG. NO. 6 REV SHT.

REVISION	DESCRIPTION	DATE	APPROVED





APPROVALS	DATE
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PROJECT: Altium

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: 89f6a8ae | DESIGN ITEM:

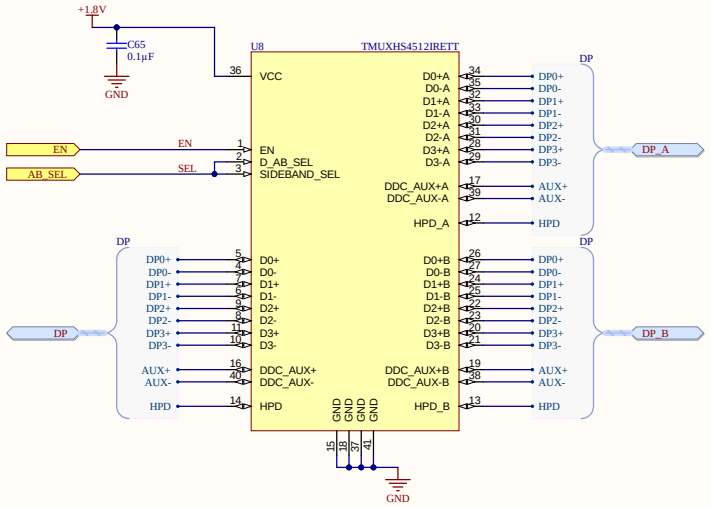
TITLE: USB Hub

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME: USB_Hub.SchDoc | SHEET 7 OF 9

<SCH DWG NO>

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
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PROJECT

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: d5299c37 | DESIGN ITEM:

TITLE

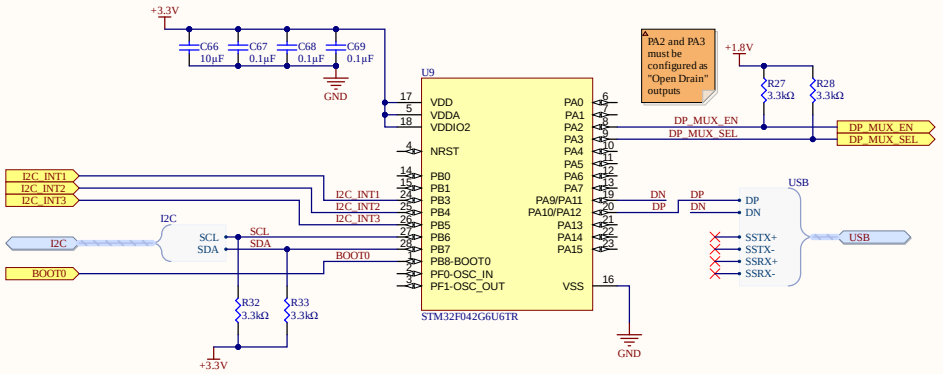
DisplayPort Mux

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME DisplayPort Mux.SchDoc | SHEET 8 OF 9

<SCH DWG NO> 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
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PROJECT

PROJECT REVISION: c7ecd1a5 | DOCUMENT REVISION: 89f6a8ae | DESIGN ITEM:

TITLE

MCU

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME MCU.SchDoc | SHEET 9 OF 9

<SCH DWG NO> 9