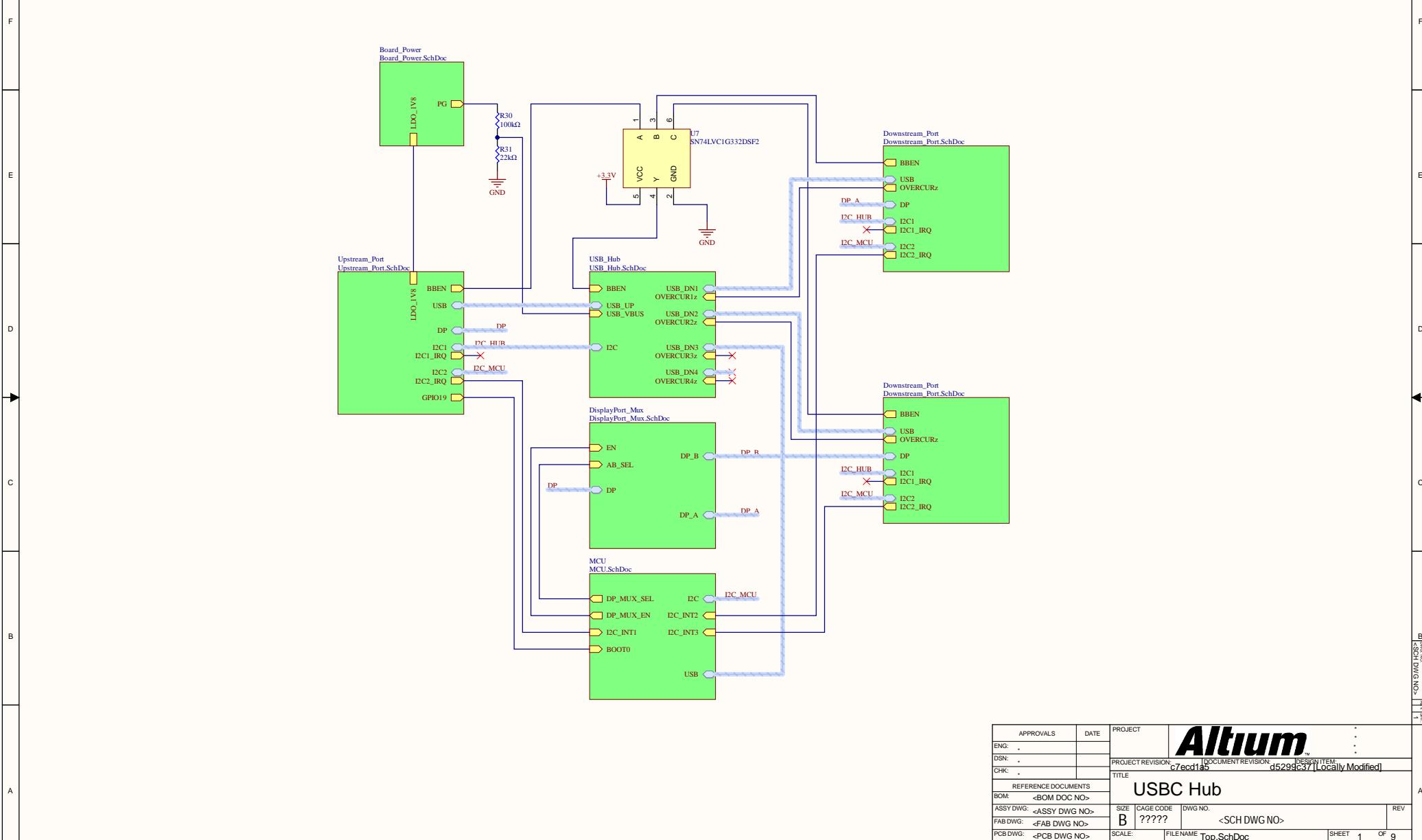


8	7	6	5	4	3	<SCH DWG NO> REV NO	1	2	1		
				↓		REV	SHT	REVISION	DESCRIPTION	DATE	APPROVED
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.											



APPROVALS	DATE	PROJECT	Altium	•
ENG:				
DSN:				
CHK:				
REFERENCE DOCUMENTS				
BOM:	<BOM DOC NO>			
ASSY DWG:	<ASSY DWG NO>			
FAB DWG:	<FAB DWG NO>			
PCB DWG:	<PCB DWG NO>			
SIZE	CAGE CODE	DWG NO		REV
B	?????		<SCH DWG NO>	
SCALE:	FILENAME	Top.SchDoc		SHEET 1 OF 9

8
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

7

6

5

4

3

<SCH DWG NO>
REV B

2

REVISION

DESCRIPTION

DATE

APPROVED

F

E

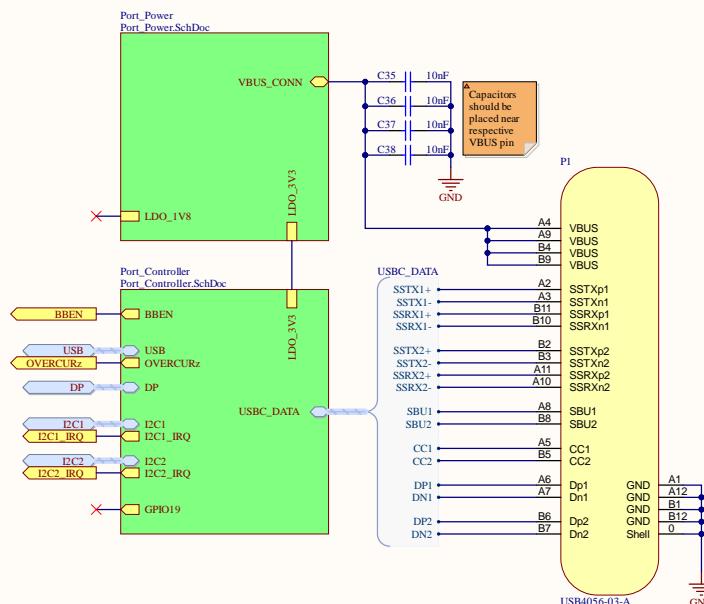
E

D

C

B

A



APPROVALS	DATE	PROJECT	Altium		
ENG: .		PROJECT REVISION: c7ecdd1ab			DOCUMENT REVISION: c35edbd01 [Locally Modified]
DSN: .					DESIGN ITEM:
CHK: .					
REFERENCE DOCUMENTS					
BOM: <BOM DOC NO>	SIZE	CAGE CODE	DWG NO:	REV	
ASSY DWG: <ASSY DWG NO>	B	?????	<SCH DWG NO>		
FAB DWG: <FAB DWG NO>					
PCB DWG: <PCB DWG NO>	SCALE:	FILENAME	Downstream_Port.SchDoc	SHEET	2 OF 9

8

7

6

5

4

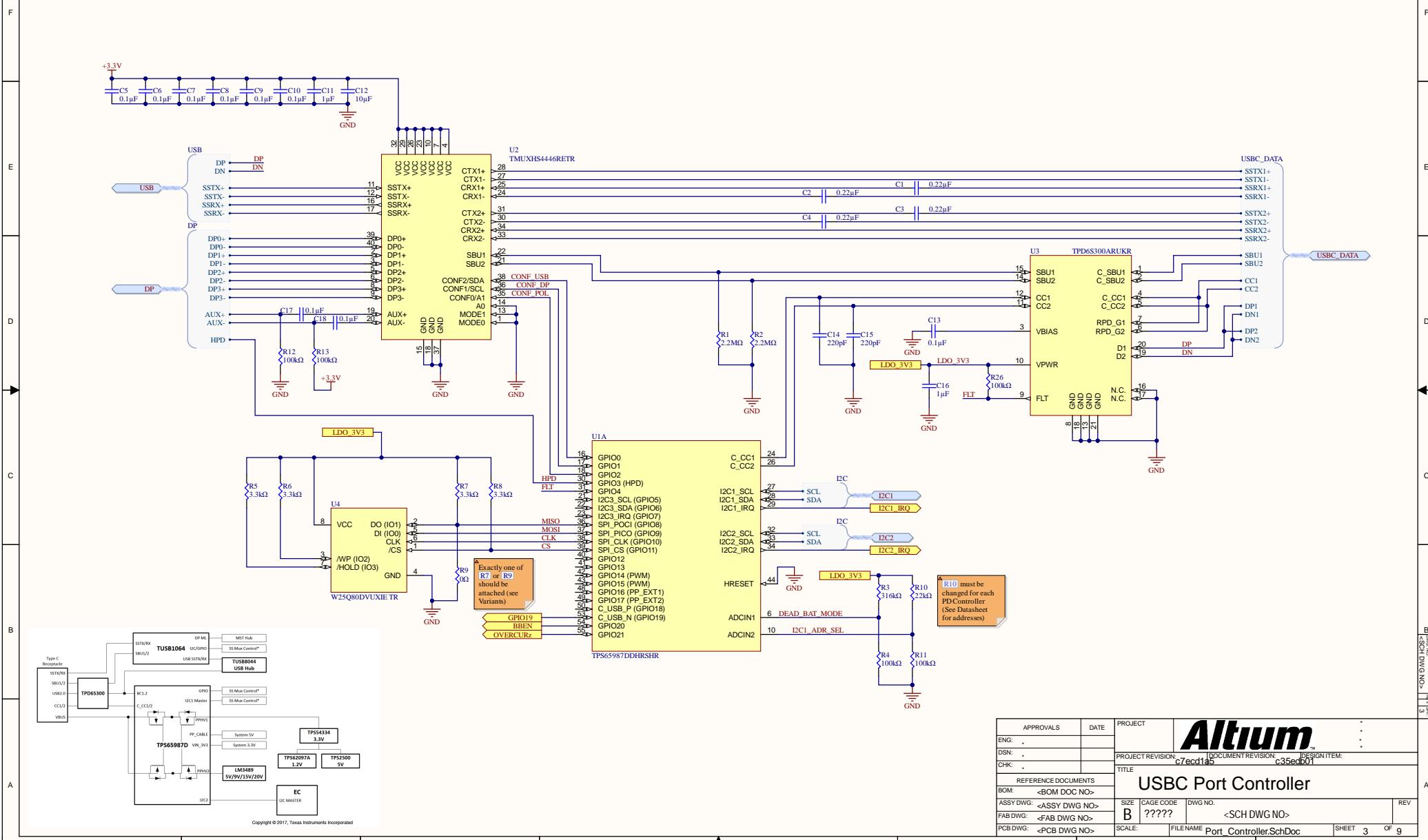
3

2

1

8	7	6	5	4	3	<SCH DWG NO> Rev. No.	3	2	1
						REVISION	DESCRIPTION	DATE	APPROVED

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARRANTY GIVEN.



APPROVALS	DATE	PROJECT	Altium
ENG: *	*		
DSN: *	*		
CHK: *	*		
REFERENCE DOCUMENTS			
BOM: <BOM DOC NO>			
ASSY DWG: <ASSY DWG NO>			
FAB DWG: <FAB DWG NO>			
PCB DWG: <PCB DWG NO>			
SCALE: *	FILE NAME: Port_Controller.SchDoc	SHEET 3 OF 9	

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

USBC Port Controller

PROJECT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

APPROVALS DATE PROJECT Altium

ENG: * DATE PROJECT Altium

DSN: * DATE PROJECT Altium

CHK: * DATE PROJECT Altium

REFERENCE DOCUMENTS DATE PROJECT Altium

BOM: <BOM DOC NO> DATE PROJECT Altium

ASSY DWG: <ASSY DWG NO> DATE PROJECT Altium

FAB DWG: <FAB DWG NO> DATE PROJECT Altium

PCB DWG: <PCB DWG NO> DATE PROJECT Altium

SCALE: FILE NAME: Port_Controller.SchDoc SHEET 3 OF 9

B GAGE CODE DWG NO: <SCH DWG NO> REV: *

CAGE CODE DWG NO: <PCB DWG NO> REV: *

ASSY DWG NO: <ASSY DWG NO> REV: *

FAB DWG NO: <FAB DWG NO> REV: *

PCB DWG NO: <PCB DWG NO> REV: *

DOCUMENT REVISION: C7ecdd1a0 DESIGN ITEM: C35ed001

TITLE: USBC Port Controller

SIZE: * CAGE CODE: DWG NO: *

8	7	6	5	4	3	<SCH DWG NO> dwg_no, rev 4	2	1
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.						REVISION	DESCRIPTION	DATE APPROVED

F

F

E

E

D

D

C

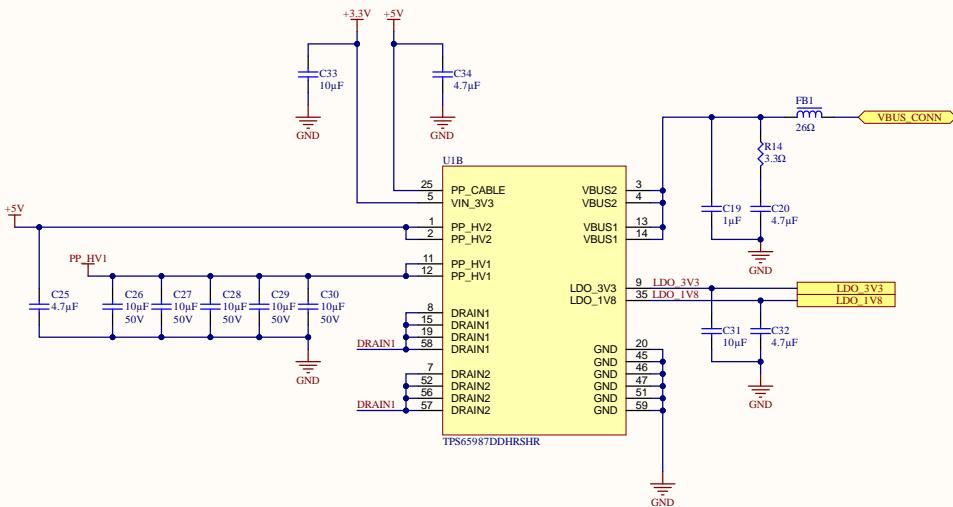
C

B

B

A

A

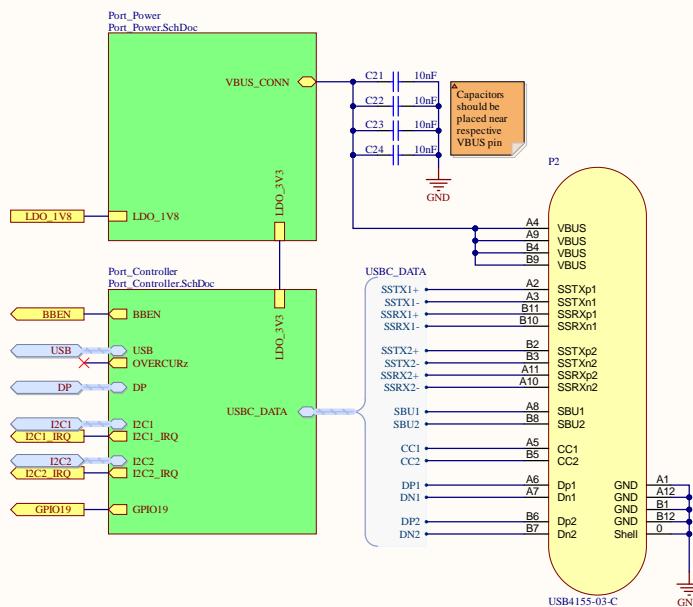


APPROVALS	DATE	PROJECT	Altium		
ENG: .			PROJECT REVISION: c/edcd1ab DOCUMENT REVISION: 89/eaabae [Locally Modified]		
DSN: .			DESIGN ITEM:		
CHK: .			TITLE: Port Power		
REFERENCE DOCUMENTS			BOM: <BOM DOC NO>		
ASSY DWG: <ASSY DWG NO>			SIZE	CAGE CODE	DWG NO.
FAB DWG: <FAB DWG NO>			B	?????	<SCH DWG NO>
PCB DWG: <PCB DWG NO>			SCALE:	FILENAME	SHEET 4 OF 9
				Port_Power.SchDoc	

8 7 6 5 4 3 2 1

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

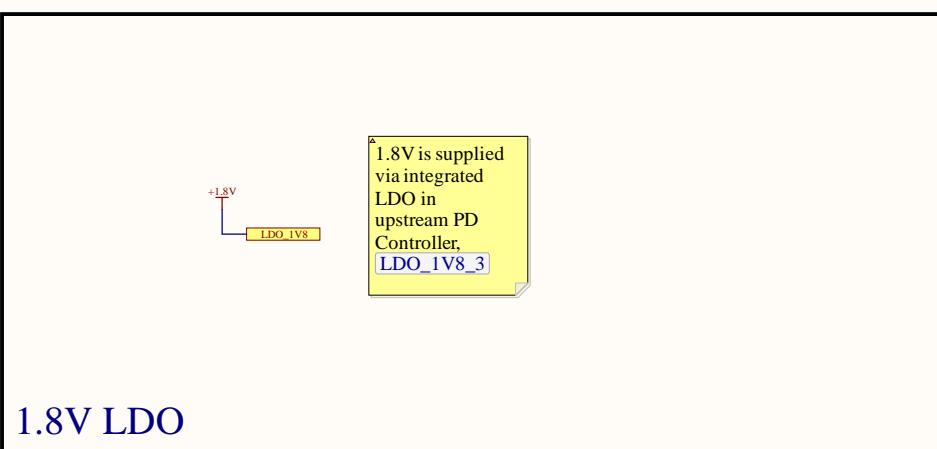
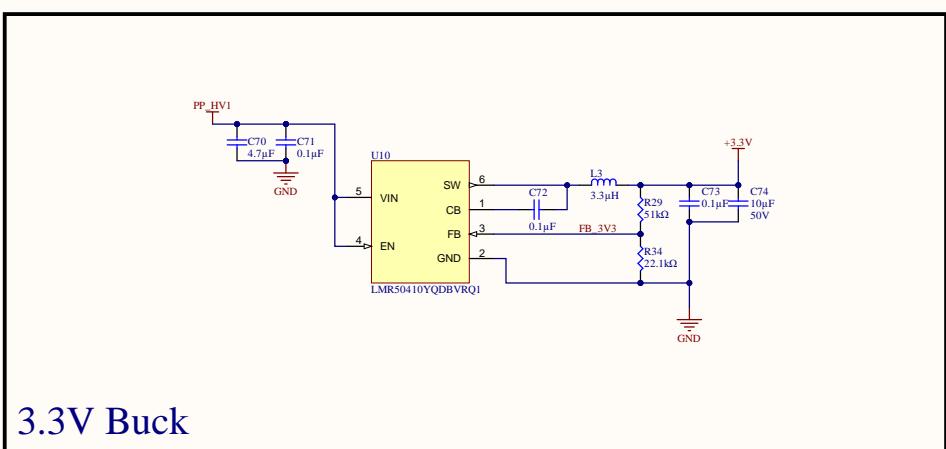
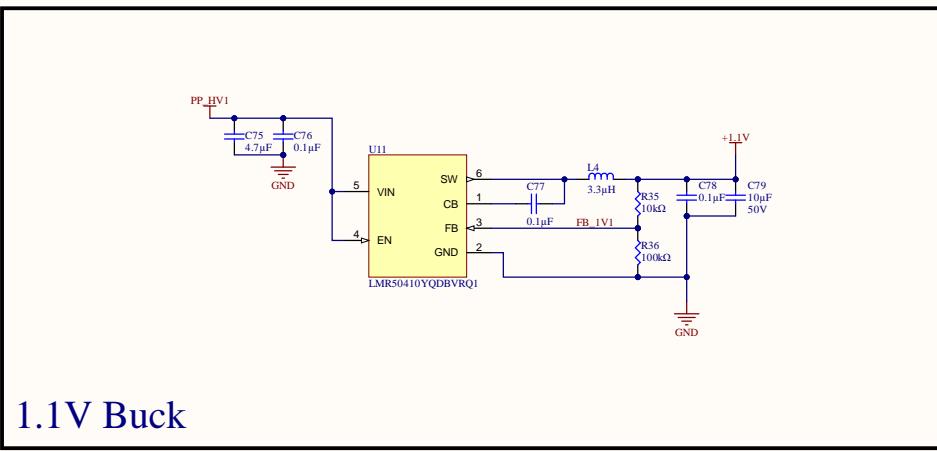
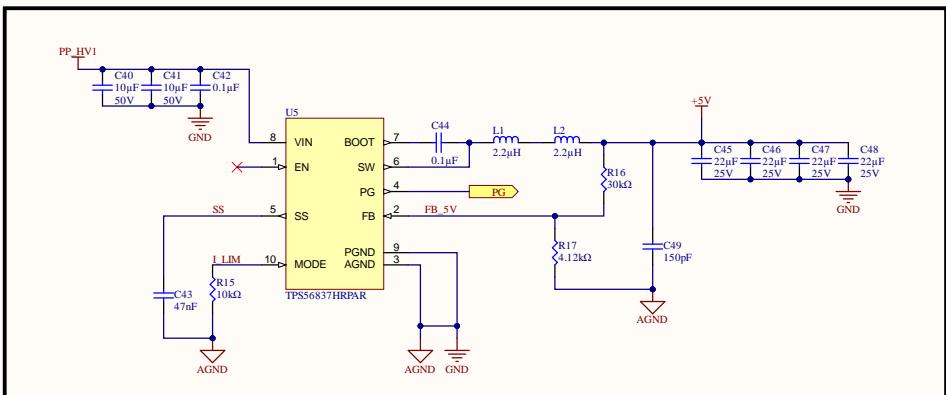
<SCH DWG NO>		REV	5 SHEET	REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Altium		
ENG: .			PROJECT REVISION: c7ecdd1ab DOCUMENT REVISION: c35edbd01 DESIGN ITEM: Locally Modified		
DSN: .			TITLE: Upstream Port		
CHK: .			BOM: <BOM DOC NO>	SIZE: B	REV: ???? <SCH DWG NO>
REFERENCE DOCUMENTS			ASSY DWG: <ASSY DWG NO>		
			FAB DWG: <FAB DWG NO>		
			PCB DWG: <PCB DWG NO>	SCALE: FILENAME Upstream_Port.SchDoc	SHEET 5 OF 9
				2	1

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

<SCH DWG NO>		6	7	8	9	10
REVISION	DESCRIPTION	DATE	APPROVED			



APPROVALS	DATE	PROJECT	Altium
ENG: .			
DSN: .			
CHK: .			
PROJECT REVISION: c7ecdd1ab DOCUMENT REVISION: c7ecdd1ab DESIGN ITEM: c7ecdd1ab [Locally Modified]			
TITLE: Board Power			
BOM: <BOM DOC NO>	CAGE CODE: B	DWG NO: ??????	REV: <SCH DWG NO>
ASSY DWG: <ASSY DWG NO>			
FAB DWG: <FAB DWG NO>			
PCB DWG: <PCB DWG NO>	SCALE: 1	FILENAME: Board_Power.SchDoc	SHEET 6 OF 9

8

7

6

5

4

3

2

1

<SCH DWG NO>

REV

7

SHEET

REVISION	DESCRIPTION	DATE	APPROVED

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARRANTY GIVEN.

F

F

E

E

D

D

C

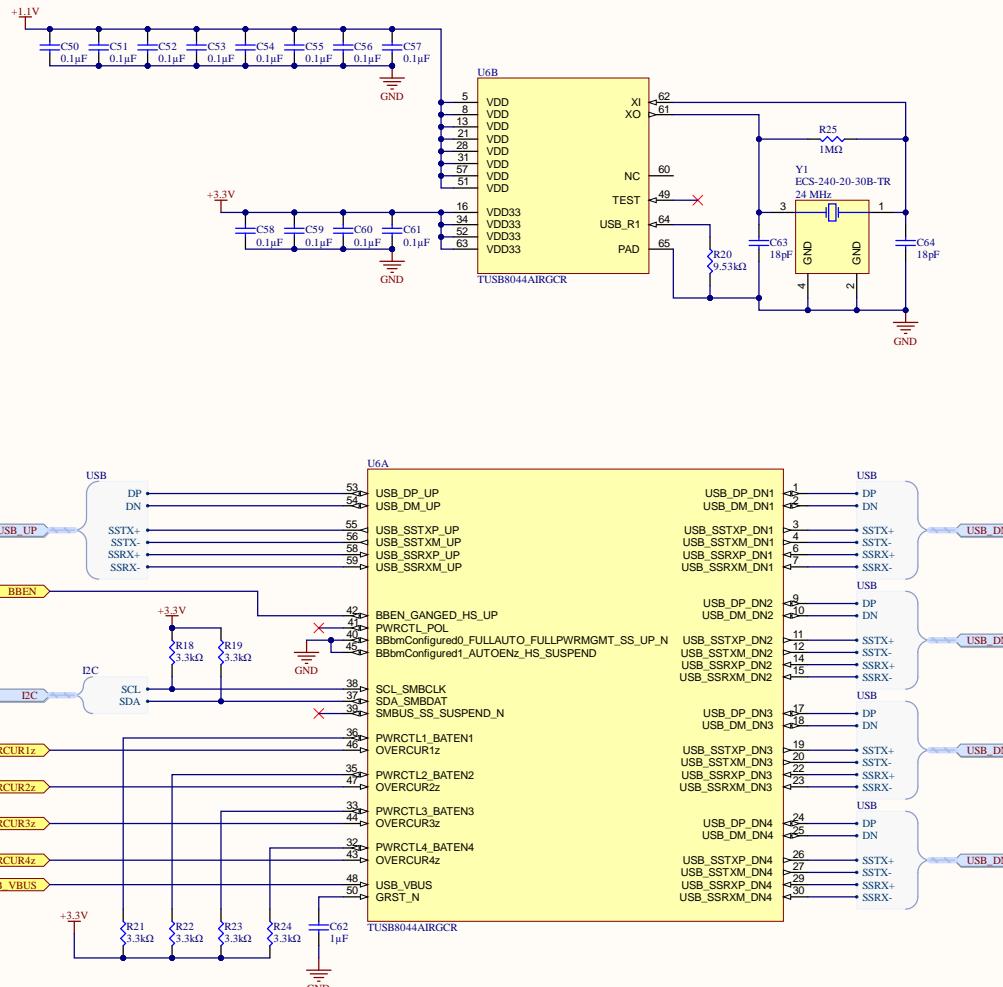
C

B

B

A

A



APPROVALS	DATE	PROJECT	Altium		
ENG: .		PROJECT REVISION:			c/edciab
DSN: .		DOCUMENT REVISION:			89fbabae
CHK: .		TITLE:			USB Hub
REFERENCE DOCUMENTS					
BOM: <BOM DOC NO>					
ASSY DWG: <ASSY DWG NO>			SIZE	CAGE CODE	DWG NO.
FAB DWG: <FAB DWG NO>			B	?????	<SCH DWG NO>
PCB DWG: <PCB DWG NO>			SCALE:	FILENAME	USB_Hub.SchDoc
			SHEET	7	OF 9
			2		1

8	7	6	5	4	3	<SCH DWG NO> DWG NO. REV 8 SHEET	2	1
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.						REVISION	DESCRIPTION	DATE APPROVED

F

F

E

E

D

D

C

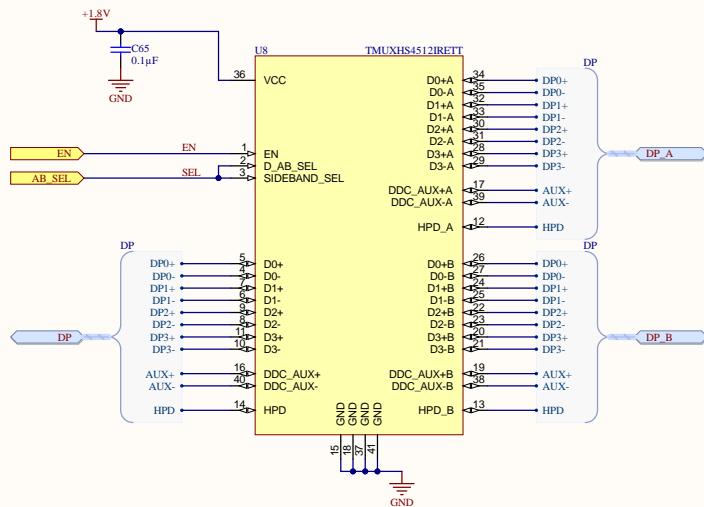
C

B

B

A

A



APPROVALS	DATE	PROJECT	Altium		
ENG:	.		PROJECT REVISION: c7ecdd1a0 DOCUMENT REVISION: d5299c37		
DSN:	.		DESIGN ITEM:		
CHK:	.		TITLE: DisplayPort Mux		
REFERENCE DOCUMENTS					
BOM:	<BOM DOC NO>		SIZE	CAGE CODE	DWG NO.
ASSY DWG:	<ASSY DWG NO>		B	?????	<SCH DWG NO>
FAB DWG:	<FAB DWG NO>		SCALE:	FILENAME	SHEET 8 OF 9
PCB DWG:	<PCB DWG NO>			DisplayPort_Mux.SchDoc	

8

7

6

5

4

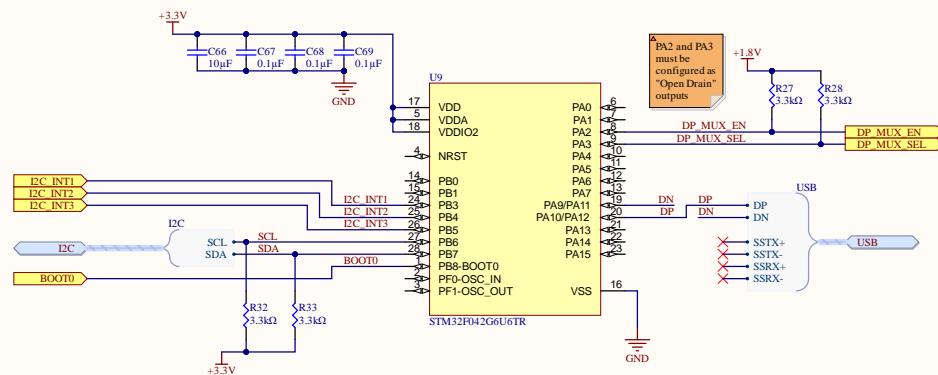
3

2

1

8	7	6	5	4	3	<SCH DWG NO> DWG NO.	REV 9	9	2	1		
				↓								
									REVISION	DESCRIPTION	DATE	APPROVED

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.



APPROVALS	DATE	PROJECT	Altium		
ENG: .		PROJECT REVISION:	c7ecdd1d	DOCUMENT REVISION:	89fbabae
DSN: .		TITLE:	MCU		
CHK: .		BOM:	<BOM DOC NO>		
REFERENCE DOCUMENTS			SIZE	CAGE CODE	DWG NO.
ASSY DWG: <ASSY DWG NO>			B	?????	<SCH DWG NO>
FAB DWG: <FAB DWG NO>			REV		
PCB DWG: <PCB DWG NO>			SCALE:	FILENAME	SHEET 9 OF 9
				MCU.SchDoc	

