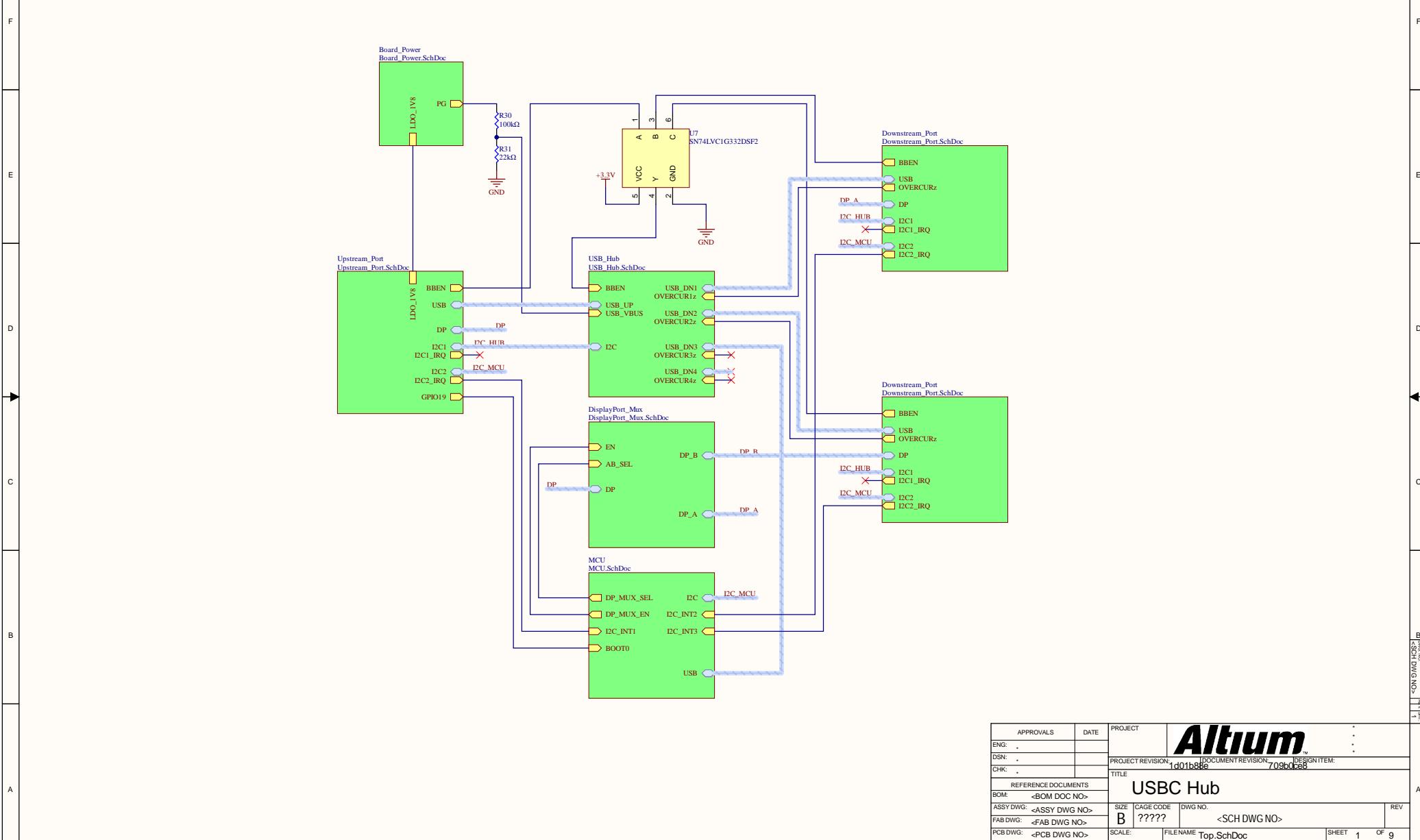


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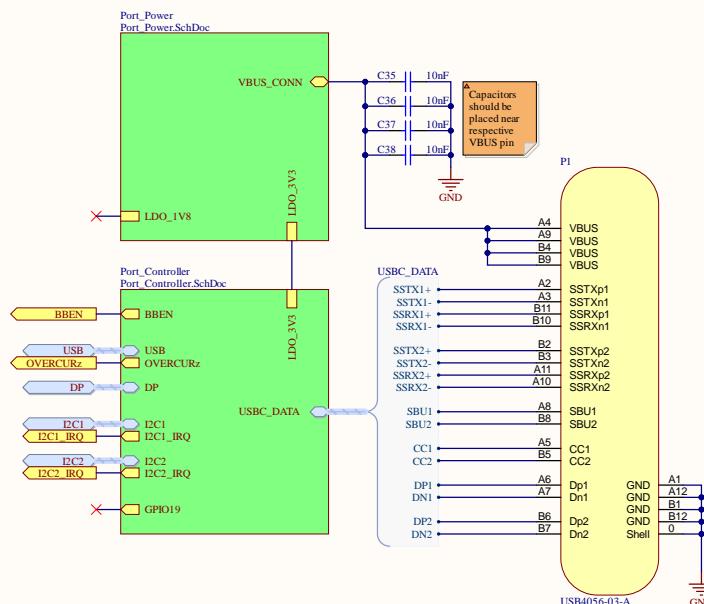


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| DSN: . | | DOCUMENT REVISION: | 709b0ec5 |
| CHK: . | | DESIGN ITEM: | |
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| FAB DWG: <FAB DWG NO> | | REV | |
| PCB DWG: <PCB DWG NO> | | SCALE: | FILE NAME |
| | | | Top.SchDoc |
| | | | SHEET 1 OF 9 |

8 7 6 5 4 3 2 1

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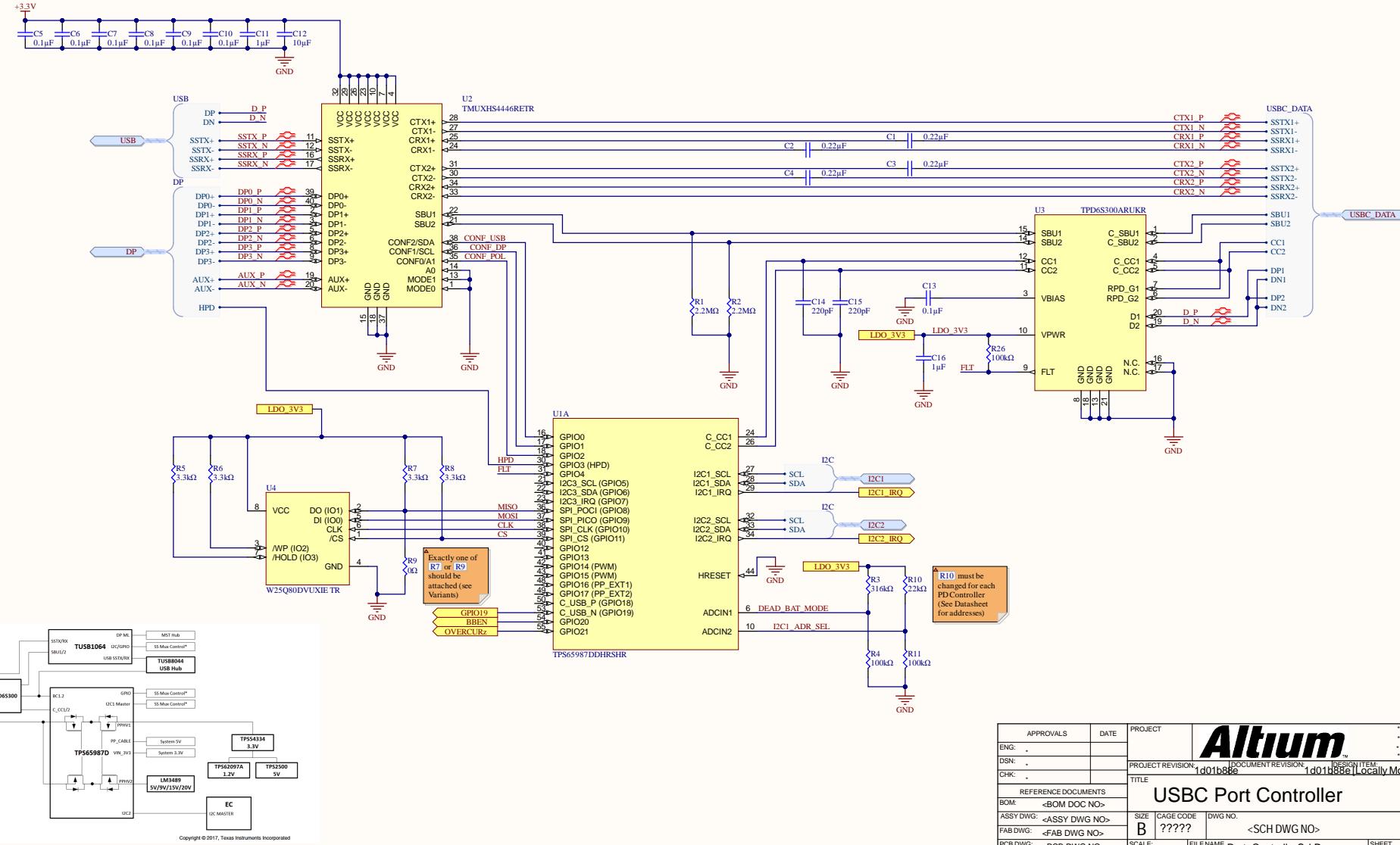
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| APPROVALS | DATE | PROJECT | Altium | . |
| ENG: | . | | | . |
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| CHK: | . | | | . |
| PROJECT REVISION: 1d01b8b8 DOCUMENT REVISION: 709b1c8e8 DESIGN ITEM: Locally Modified | | | | |
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| FAB DWG: | <FAB DWG NO> | | | |
| PCB DWG: | <PCB DWG NO> | | | |
| SCALE: | FILE NAME | Downstream_Port.SchDoc | SHEET | 2 OF 9 |
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| | | <SCH DWG NO> | | |

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| REVISION | DESCRIPTION | DATE | APPROVED | |



| APPROVALS | | DATE | PROJECT | Altium |
|---------------------|---------------|------------------------|-------------------|----------------------------|
| ENG: | . | | | |
| DSN: | . | | PROJECT REVISION | 1d01b8e |
| CHK: | . | | DOCUMENT REVISION | 1d01b8e [Locally Modified] |
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| SCALE: | FILE NAME | Port_Controller.SchDoc | HEET | 3 OF 9 |
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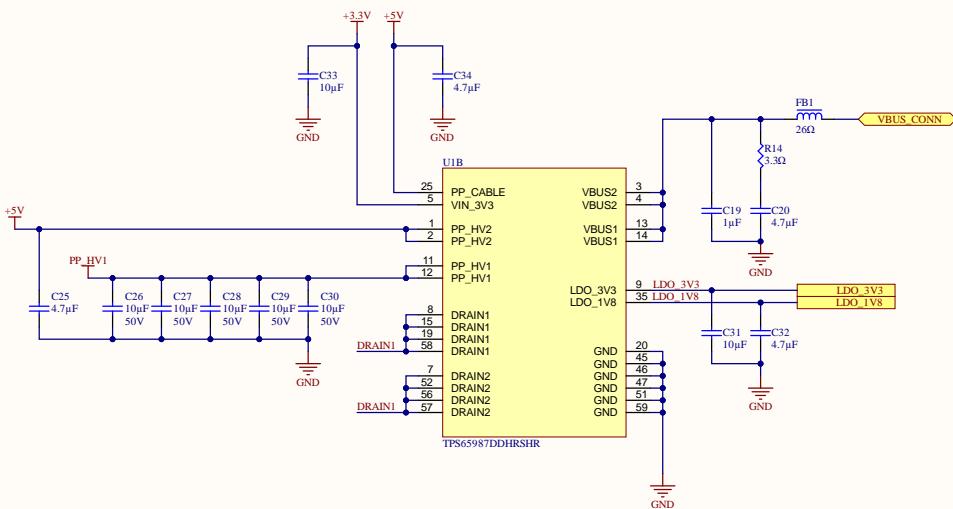
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| PCB DWG: <PCB DWG NO> | SCALE: | FILENAME | SHEET 4 OF 9 |
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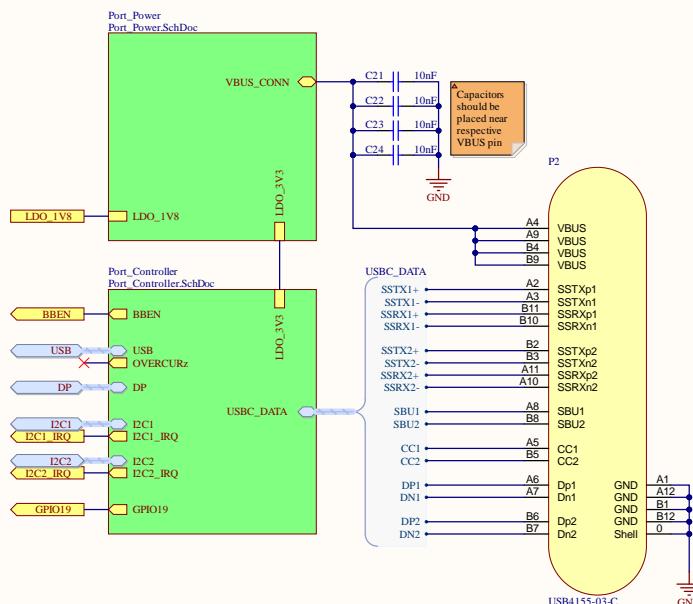
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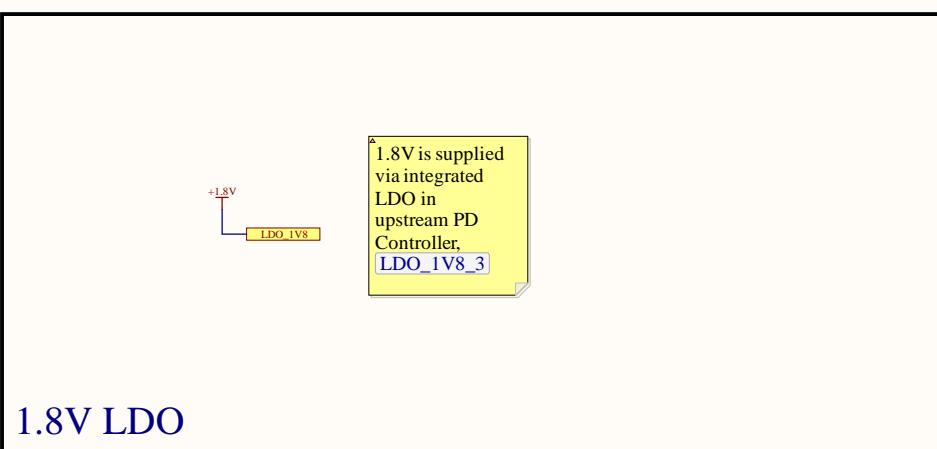
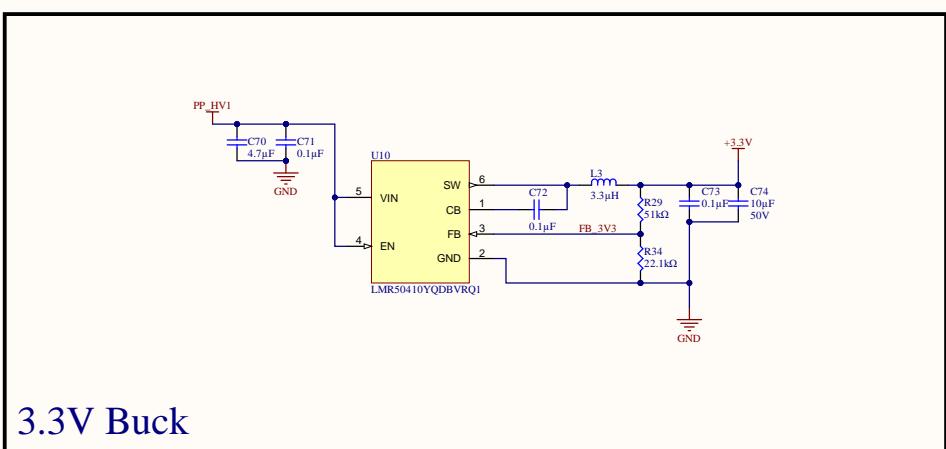
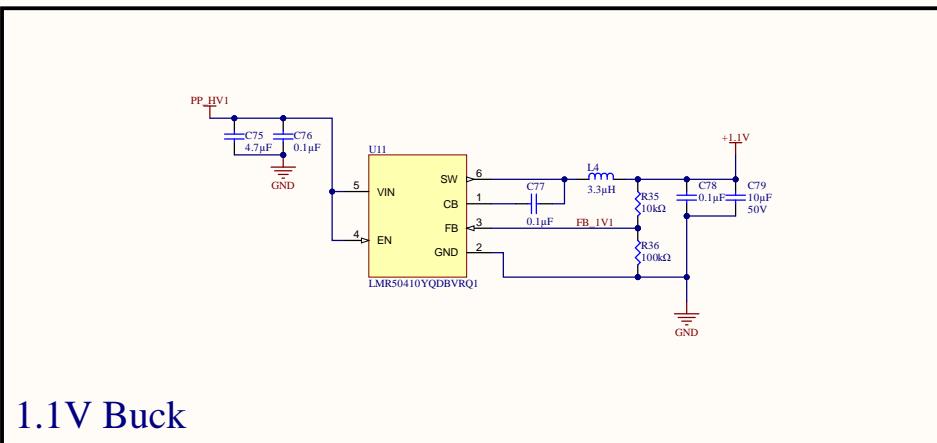
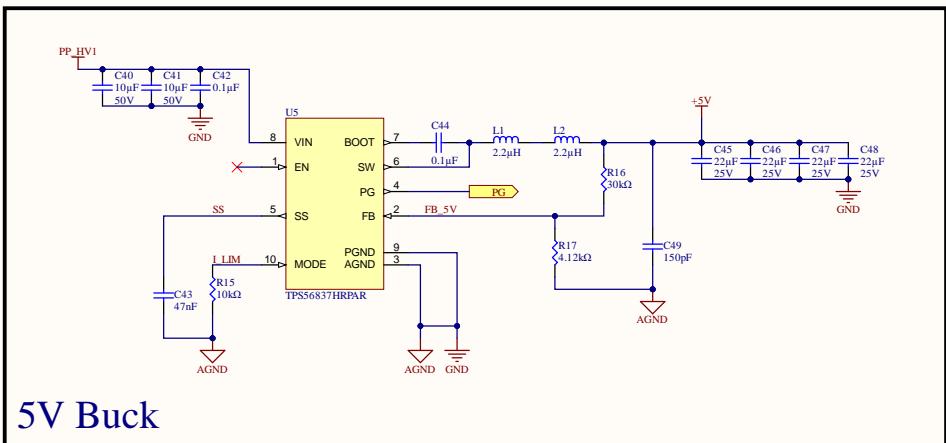
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| SIZE B | CAGE CODE ????? | DWG NO. <SCH DWG NO> | | REV | |
| SCALE: Upstream | FILENAME: Upstream_Port.SchDoc | SHEET 5 | OF 9 | | |

| 8 | 7 | 6 | 5 | 4 | 3 | <SCH DWG NO> | 6 | 2 | 1 |
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| REVISION | DESCRIPTION | DATE | APPROVED | | | | | | |

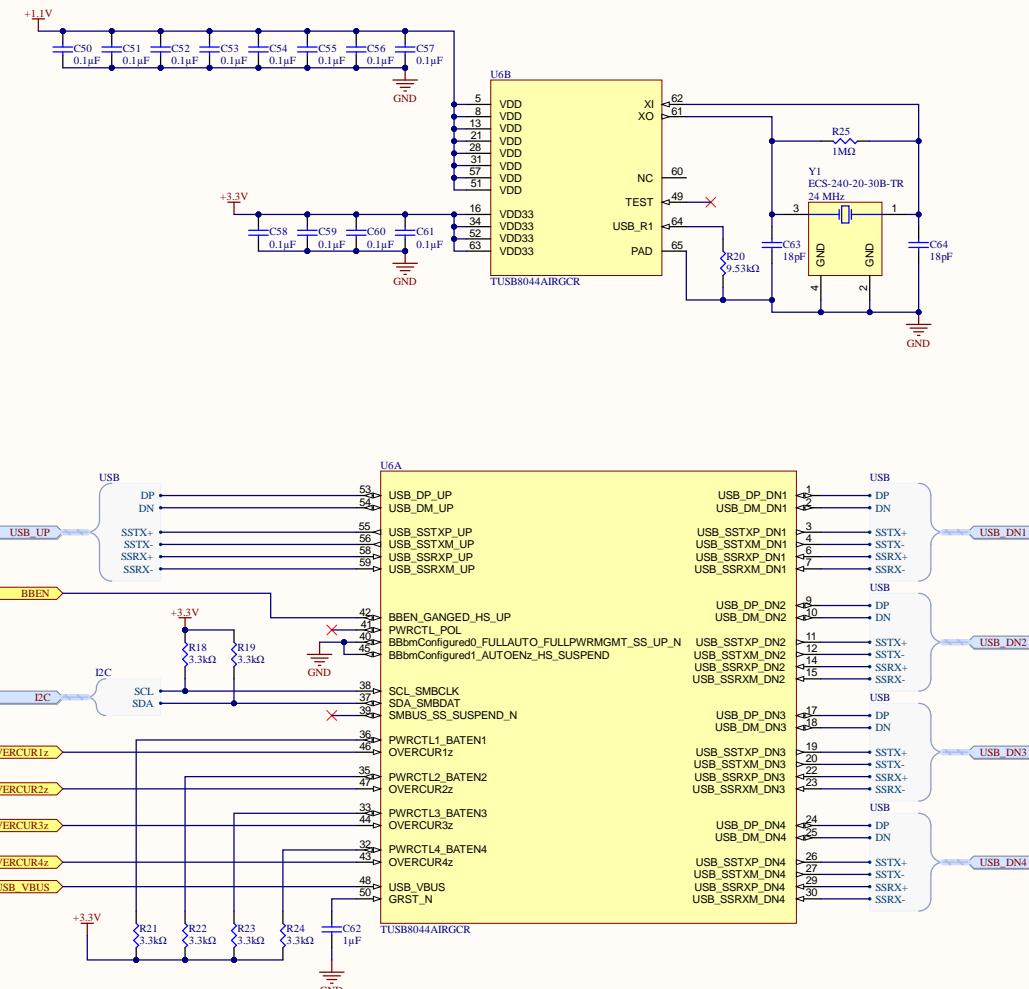
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| PCB DWG: <PCB DWG NO> | SCALE: | FILENAME | Board_Power.SchDoc | SHEET 6 OF 9 | |

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| ENG: . | | PROJECT REVISION: | DOCUMENT REVISION: | DESIGN ITEM |
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| REFERENCE DOCUMENTS | | USB Hub | | |
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| PCB DWG: <PCB DWG NO> | SCALE: | FILENAME | USB_Hub.SchDoc | SHEET 7 OF 9 |

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| 8 | 7 | 6 | 5 | 4 | 3 | <SCH DWG NO> dwg_no | 8 | 2 | 1 | | |
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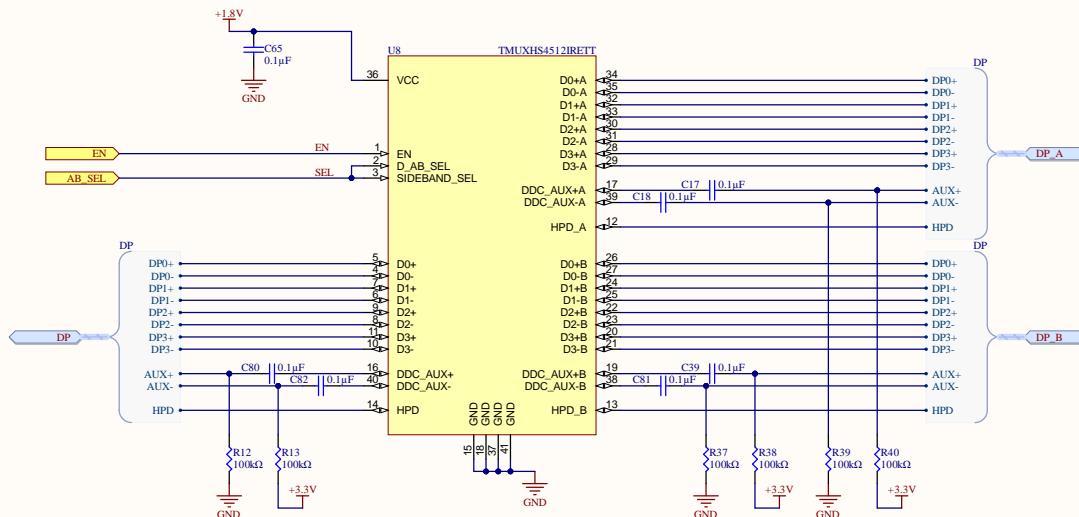
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| 8 | 7 | 6 | 5 | 4 | 3 | <SCH DWG NO> DWG NO. REV 9 SHEET | 2 | 1 |
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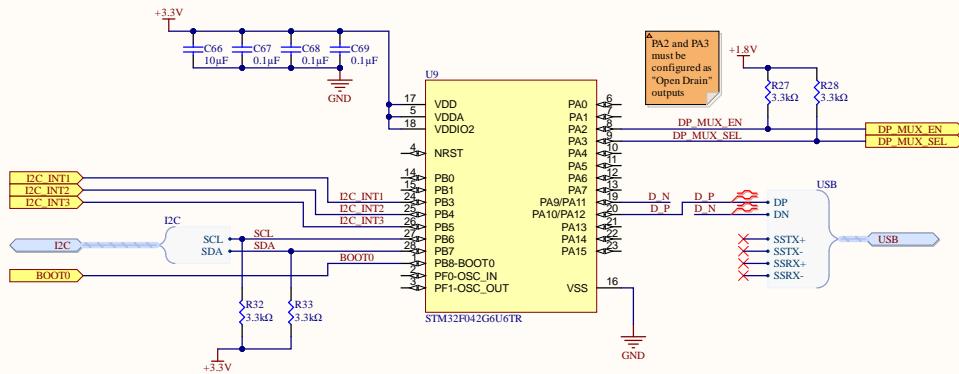
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| FAB DWG: <FAB DWG NO> | SCALE: | FILENAME | MCU.SchDoc | SHEET | 9 OF 9 |
| PCB DWG: <PCB DWG NO> | | | | | |

