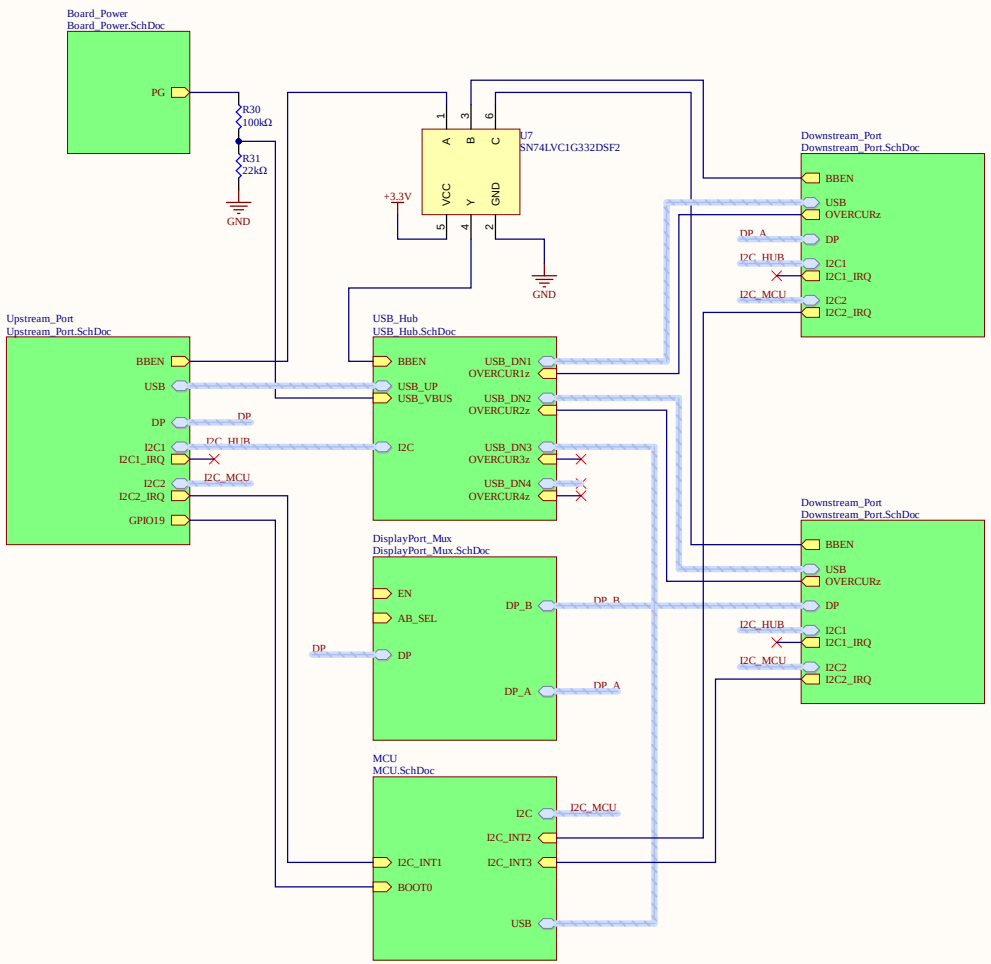
REVISION	DESCRIPTION	DATE	APPROVED



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CHK: *	

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ASSY DWG: <ASSY DWG NO>
FAB DWG: <FAB DWG NO>
PCB DWG: <PCB DWG NO>

PROJECT

Altium

PROJECT REVISION: 7fc4b7a9 [DOCUMENT REVISION: 7fc4b7a9 [Locally Modified]] [DESIGN ITEM:

TITLE

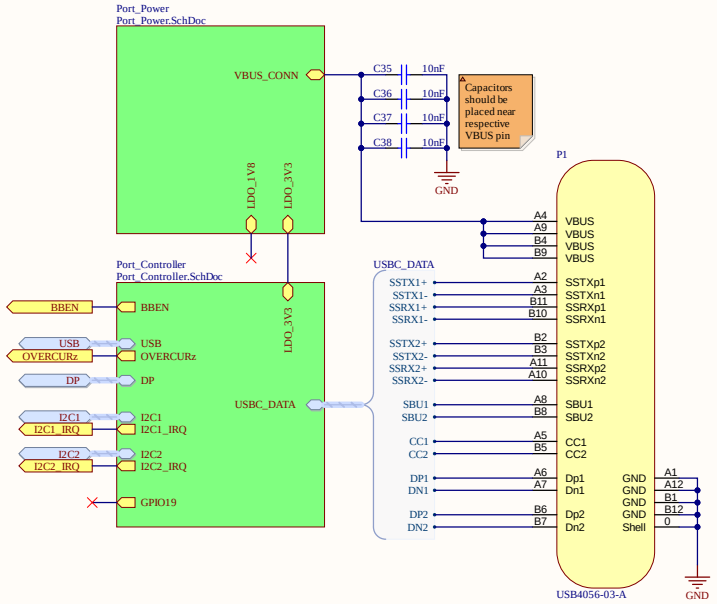
USBC Hub

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME Top.SchDoc SHEET 1 OF 9

<SCH DWG NO> DWG. NO. | REV | 1 SHT.

REVISION	DESCRIPTION	DATE	APPROVED



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PROJECT

PROJECT REVISION: 7fc4b7a8 [DOCUMENT REVISION: 5cc23ec5 [Locally Modified]] DESIGN ITEM:

TITLE

Downstream Port

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME Downstream_Port.SchDoc SHEET 2 OF 9

<SCH DWG NO> DWG. NO. REV 2 SHT.

REVISION	DESCRIPTION	DATE	APPROVED

+3.3V

C5 0.1µF, C6 0.1µF, C7 0.1µF, C8 0.1µF, C9 0.1µF, C10 0.1µF, C11 1µF, C12 10µF

GND

USB

DP

DN

SSTX+

SSTX-

SSRX+

SSRX-

DP0+

DP0-

DP1+

DP1-

DP2+

DP2-

DP3+

DP3-

AUX+

AUX-

HPD

C17 0.1µF, C18 0.1µF

R12 100kΩ, R13 100kΩ

U2

TMUXHS4446RETR

VCC

GND

CTX1+

CTX1-

CRX1+

CRX1-

CTX2+

CTX2-

CRX2+

CRX2-

SBU1

SBU2

CONF2/SDA

CONF1/SCL

CONF0/A1

A0

MODE1

MODE0

CONF_USB

CONF_DP

CONF_POL

C1 0.22µF, C2 0.22µF, C3 0.22µF, C4 0.22µF

USBC_DATA

R1 2.2MΩ, R2 2.2MΩ

C14 220pF, C15 220pF, C13 0.1µF, C16 1µF

U3

TPD6S300ARUKR

SBU1

SBU2

CC1

CC2

VBIAS

VPWR

FLT

C_SBU1

C_SBU2

C_CC1

C_CC2

RPD_G1

RPD_G2

D1

D2

N.C.

LDO_3V3

R26 100kΩ, R27 100kΩ, R28 100kΩ, R29 22kΩ

U1A

GPIO0

GPIO1

GPIO2

GPIO3 (HPD)

GPIO4

I2C3_SCL (GPIO5)

I2C3_SDA (GPIO6)

I2C3_IRQ (GPIO7)

SPI_POCI (GPIO8)

SPI_PICO (GPIO9)

SPI_CLK (GPIO10)

SPI_CS (GPIO11)

GPIO12

GPIO13

GPIO14 (PWM)

GPIO15 (PWM)

GPIO16 (PP_EXT1)

GPIO17 (PP_EXT2)

C_USB_P (GPIO18)

C_USB_N (GPIO19)

GPIO20

GPIO21

C_CC1

C_CC2

I2C1_SCL

I2C1_SDA

I2C1_IRQ

I2C2_SCL

I2C2_SDA

I2C2_IRQ

HRESET

ADCIN1

ADCIN2

I2C

SCL

SDA

I2C1

I2C1_IRQ

I2C2

I2C2_IRQ

DEAD_BAT_MODE

I2C1_ADR_SEL

R3 316kΩ, R10 22kΩ, R4 100kΩ, R11 100kΩ

TPS65987DDHRSHR

U4

W25Q80DVUXIE TR

VCC

DO (IO1)

DI (IO0)

CLK

/CS

/WP (IO2)

/HOLD (IO3)

GND

MISO

MOSI

CLK

CS

R5 3.3kΩ, R6 3.3kΩ, R7 3.3kΩ, R8 3.3kΩ, R9 0Ω

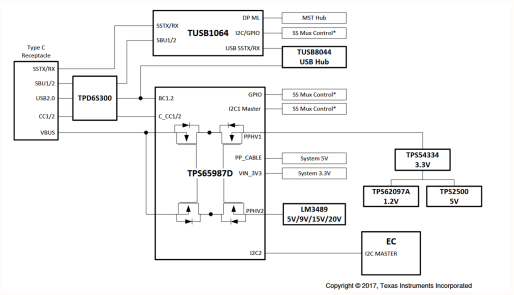
Exactly one of R7 or R9 should be attached (see Variants)

R10 must be changed for each PD Controller (See Datasheet for addresses)

GPIO19

BBEN

OVERCURz



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PCB DWG: <PCB DWG NO>

PROJECT

Altium

PROJECT REVISION: 7fc4b7a9 [DOCUMENT REVISION: 5cc23ec9 [Locally Modified]]

DESIGN ITEM:

TITLE

USBC Port Controller

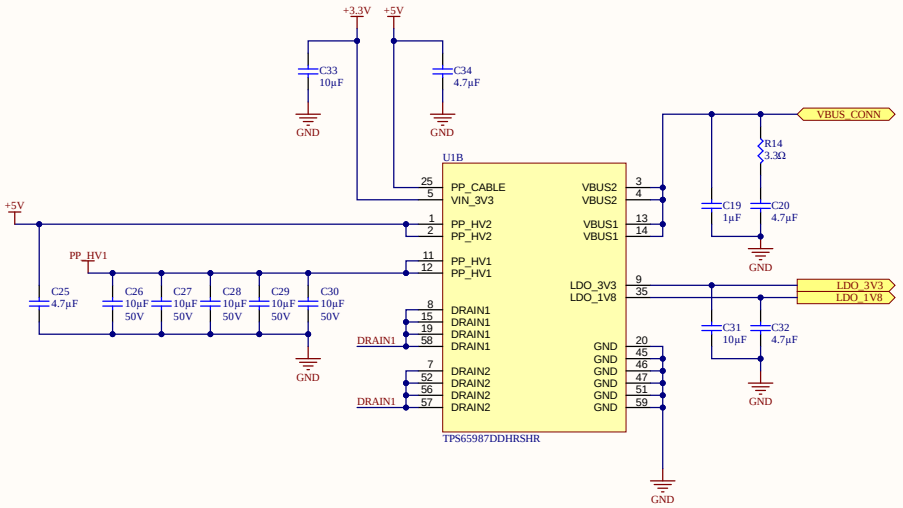
SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE:

FILE NAME Port_Controller.SchDoc

SHEET 3 OF 9

REVISION	DESCRIPTION	DATE	APPROVED



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PROJECT

Altium

PROJECT REVISION: 7fc4b7a9 | DOCUMENT REVISION: a2d2c34a | DESIGN ITEM:

TITLE

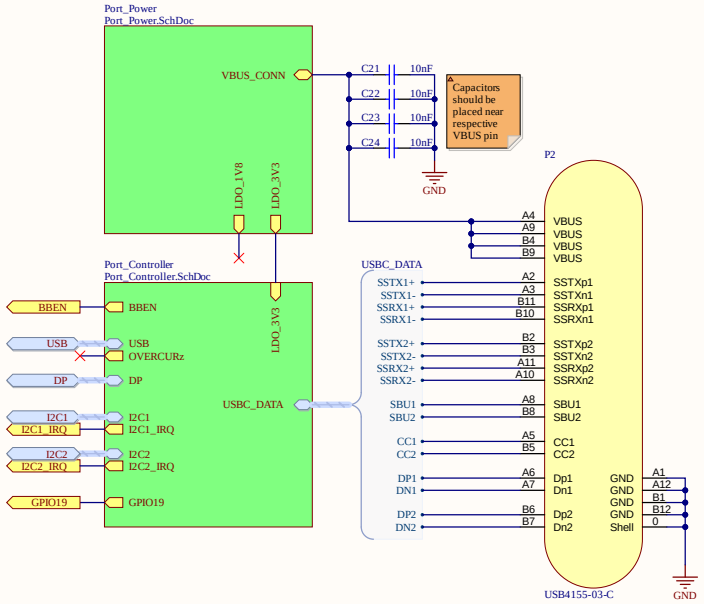
Port Power

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME Port_Power.SchDoc | SHEET 4 OF 9

<SCH DWG NO> DWG. NO. | 4 REV | SHT.

REVISION	DESCRIPTION	DATE	APPROVED



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BOM:	<BOM DOC NO>
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PCB DWG:	<PCB DWG NO>

PROJECT: Altium

PROJECT REVISION: 7fc4b7a8 [DOCUMENT REVISION: 5cc23ec5 [Locally Modified]] DESIGN ITEM:

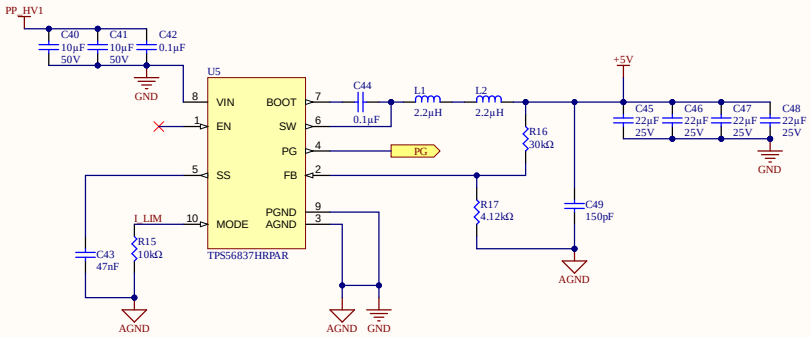
TITLE: Upstream Port

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME: Upstream_Port.SchDoc SHEET 5 OF 9

<SCH DWG NO> REV 5 SHT

REVISION	DESCRIPTION	DATE	APPROVED



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CHK: *	

REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
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PCB DWG:	<PCB DWG NO>

PROJECT

PROJECT REVISION: 7fc4b7a8 | DOCUMENT REVISION: adcba55b | DESIGN ITEM:

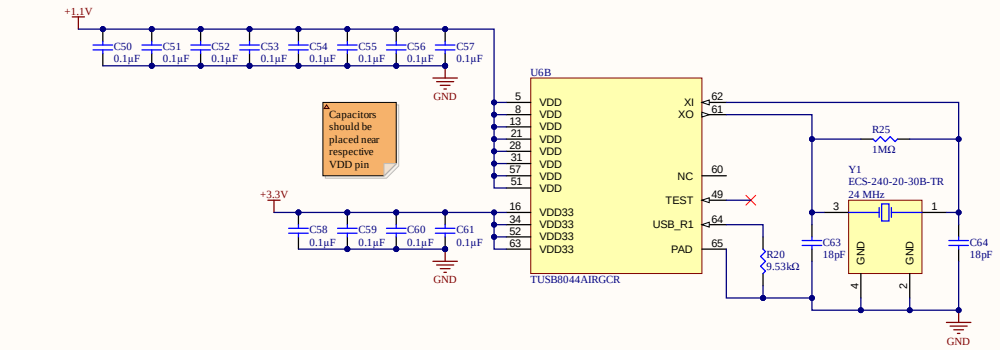
TITLE

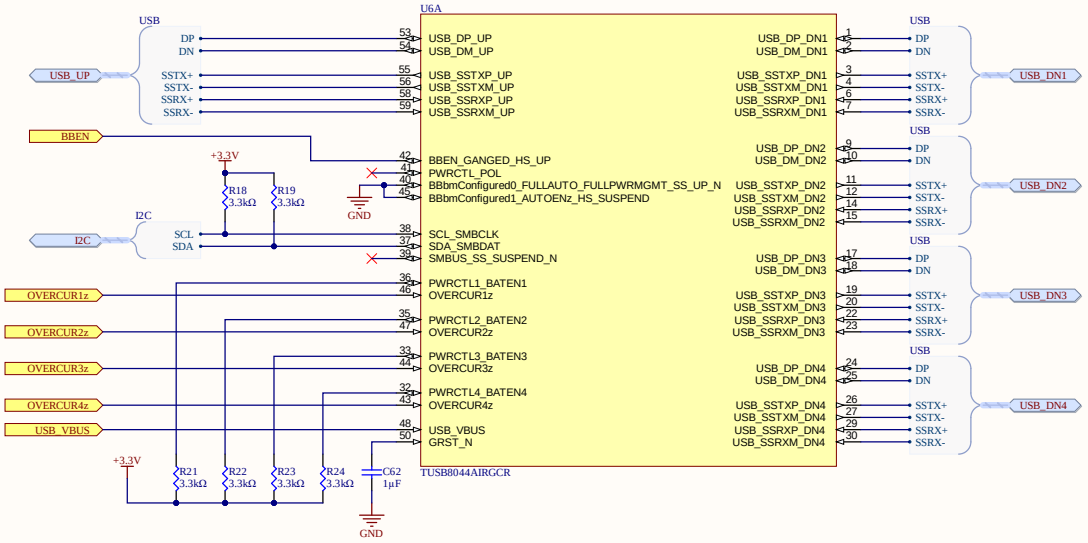
Board Power

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME Board_Power.SchDoc | SHEET 6 OF 9

REVISION	DESCRIPTION	DATE	APPROVED





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REFERENCE DOCUMENTS

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ASSY DWG: <ASSY DWG NO>
FAB DWG: <FAB DWG NO>
PCB DWG: <PCB DWG NO>

PROJECT

PROJECT REVISION: 7fc4b7a9 DOCUMENT REVISION: 5cc23cc5 DESIGN ITEM:

TITLE

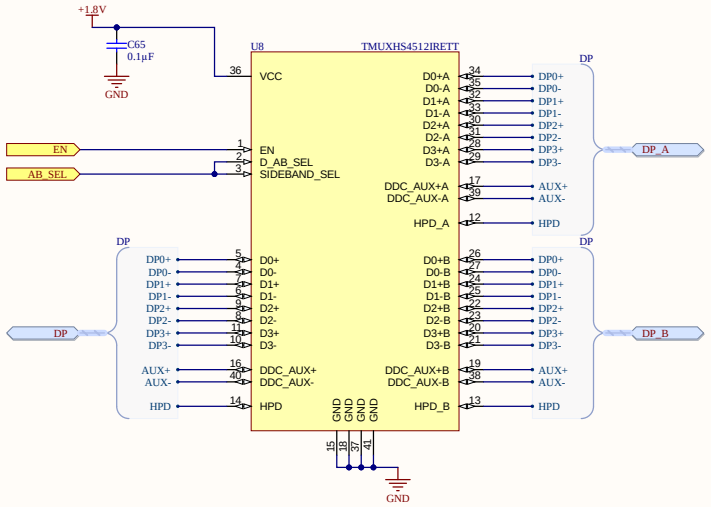
USB Hub

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME USB_Hub.SchDoc SHEET 7 OF 9

<SCH DWG NO> 7

REVISION	DESCRIPTION	DATE	APPROVED



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CHK: *	

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PCB DWG: <PCB DWG NO>

PROJECT

Altium

PROJECT REVISION: 7fc4b7a9 DOCUMENT REVISION: 36c1906e DESIGN ITEM:

TITLE

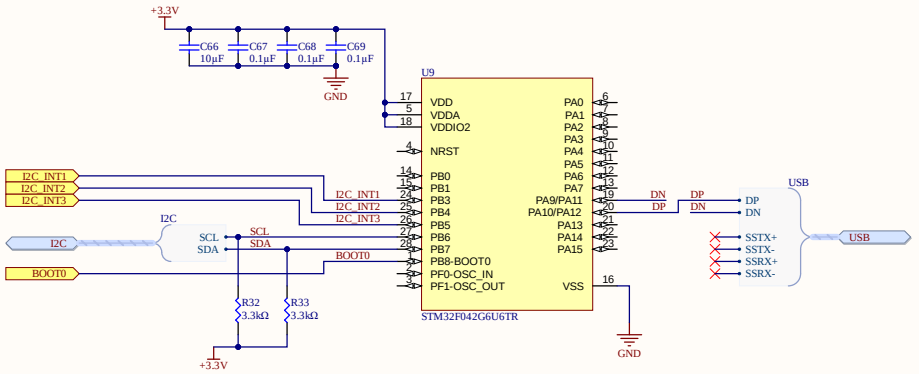
DisplayPort Mux

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME DisplayPort Mux.SchDoc SHEET 8 OF 9

<SCH DWG NO> 8

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
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REFERENCE DOCUMENTS

BOM:	<BOM DOC NO>
ASSY DWG:	<ASSY DWG NO>
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PCB DWG:	<PCB DWG NO>

PROJECT

PROJECT REVISION: 7fc4b7a8 | DOCUMENT REVISION: 5cc23cc5 | DESIGN ITEM:

TITLE: MCU

SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: | FILE NAME: MCU.SchDoc | SHEET 9 OF 9

<SCH DWG NO> DWG. NO. | REV | 9 SHT.