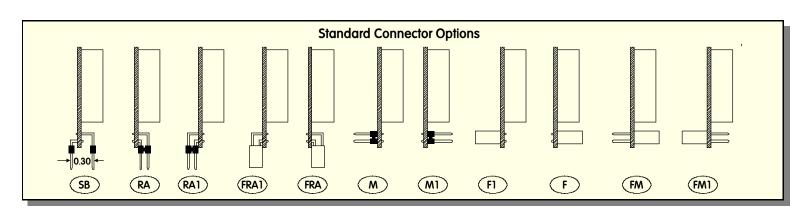


## Adapt912DT60 CONNECTOR PINOUTS (Rev. 2 board)

Addpi912D100 CONNECTOR PINOO13 (Rev. 2 bodia)							
HI				H2			
PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PS4/MISO	50	GROUND	1	PA7/ADDR15/DATA15	50	VCC (+5VDC)
2	PS5/MOSI	49	GROUND	2	PA6/ADDR14/DATA14	49	GROUND
3	PS6/SCK	48	PS0/RXD0	3	PA5/ADDR13/DATA13	48	PE7/DBE*
4	PS7/SS*	47	+5VDC	4	PA4/ADDR12/DATA12	47	PP7
5	PS1/TXD0	46	PE1/IRQ*	5	PA3/ADDR11/DATA11	46	PP6
6	PT7/IOC7	45	PE0/XIRQ*	6	PA2/ADDR10/DATA10	45	PP5
7	PT6/IOC6	44	RESET*	7	PA1/ADDR9/DATA9	44	PP4
8	PT5/IOC5	43	PE7/ECLK*/CAL/DBE*	8	PA0/ADDR8/DATA8	43	PP3/PW3
9	PT4/IOC4	42	PHO/KWHO	9	PB7/ADDR7/DATA7	42	PP2/PW2
10	PT3/IOC3	41	PH1/KWH1	10	PB6/ADDR6/DATA6	41	PP1/PW1
11	PT2/IOC2	40	PH2/KWH2	11	PB5/ADDR5/DATA5	40	PP0/PW0
12	PT1/IOC1	39	PH3/KWH3	12	PB4/ADDR4/DATA4	39	PCAN7
13	PT0/IOC0	38	PH4/KWH4	13	PB3/ADDR3/DATA3	38	PCAN6
14	PG7	37	PH5/KWH5	14	PB2/ADDR2/DATA2	37	PCAN5
15	PG6/KWG6	36	PH6/KWH6	15	PB1/ADDR1/DATA1	36	PCAN4
16	PG5/KWG5	35	PH7/KWH7	16	PB0/ADDR0/DATA0	35	PCAN3
17	PG4/KWG4	34	PS2/RXD1	17	R/W* PE2	34	PCAN2
18	PG3/KWG3	33	PE4/ECLK	18	ECLK/PE4	33	PCAN1/TxCAN
19	PG2/KWG2	32	PS3/TXD1	19	LSTRB*/PE3	32	PCANO/RxCAN
20	PG1/KWG1	31	VRLO	20	IRQ*/PE1	31	VRH1
21	PG0/KWG0	30	VRH0	21	PK3	30	VRL1
22	PAD00/AN00	29	PAD04/AN04	22	PAD10/AN10	29	PAD14/AN14
23	PAD01/AN01	28	PAD05/AN05	23	PAD11/AN11	28	PAD15/AN15
24	PAD02/AN02	27	PAD06/AN06	24	PAD12/AN12	27	PAD16/AN16
25	PAD03/AN03	26	PAD07/AN07	25	PAD13/AN13	26	PAD17/AN17

NOTES: \* indicates active low signal



Technological Arts

Module: #AD912DT60M-□-□
Starter Package: #AD912DT60SP(-□-□)
(default RA-M connectors unless otherwise specified)

©2001 Technological Arts Specifications subject to change without notice