Udit Gupta

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Education

Harvard University
PhD Computer Science *2016 - Present*

Cornell University
Bachelor of Science, GPA - 4.00 *2012-2016*
Suma Cum Laude, Dean's List (All Semesters)
Major: Electrical and Computer Engineering
Minor: Computer Science

Research Interests

Hardware / software co-design, design automation, hardware specialization, **cross-layer heterogeneous architectures** and **emerging computing platforms** focusing on improving programmability, energy efficiency and performance in the context of datacenter and embedded workloads.

Honors and Awards

Richard A. Newton Young Fellows Scholarship *May 2015 - June 2015*
Cornell ECE Early Research Career Scholarship *May 2013 - September 2013*
Eta Kappa Nu - Electrical Engineering Honor Society *October 2013 - Present*

Conference and Workshop Publications

Mingxing Tan, Steve Dai, **Udit Gupta** and Zhiru Zhang. *"Mapping-Aware Constrained Scheduling for LUT-Based FPGAs"*. 23^{rd} ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2015)

Udit Gupta, Steve Dai, Zhiru Zhang. *"Rosetta: A Realistic Benchmark Suite for Software Programmable FPGAs"*. Suite of Embedded Applications and Kernels (SEAK 2015)

Technical Articles and Presentations

Udit Gupta *"Software Programmable FPGAs"*. Circuit Cellar, "Tech the Future" series (July 2016)

Steve Dai, **Udit Gupta** and Ritchie Zhao. *"Towards High-Level Programming for FPGAs"*. Cornell Computer Systems Lab (November 2014)

Work Experience

Hardware Design and Verification Engineering Intern **Santa Clara, CA**
Algo-Logic Systems *May 2015 - August 2015*
Designed OpenCL board support package for clients to develop and integrate software kernels with existing low latency network IP for the Tick-to-Trade system. Developed software interface for configuring FPGA and OpenCL financial data parsers and trading algorithms.

Research Experience

Heterogeneous Parallel Computing using High Level Synthesis **Cornell University**
Professor Zhiru Zhang *December 2013 - Present*
Accelerated machine learning application (K-Nearest Neighbor) for handwritten digit recognition with OpenCL using SDAccel and C/C++ using Vivado HLS targeting Xilinx's Zynq 7000 Programmable SoC (ZC702 and Zedboard). Benchmarked handwritten RTL (Verilog) versus HLS generated RTL from C/C+ and OpenCL designs for optimizing latency, throughput and area. Integrated Xilinx AXI IP cores with HLS generated RTL cores and handwritten RTL cores.

Rosetta: A Realistic Benchmark Suite for Software Programmable FPGAs **Cornell University**
Professor Zhiru Zhang *December 2014 - Present*
Leading a group of 4 undergraduates to design a problem based reconfigurable benchmark suite targeting FPGAs using C/C++ and OpenCL driven HLS tools for applications spanning computer vision, finance, signal processing, security and machine learning domains.

Mitigating Timing Channels for Shared Hardware Accelerators **Cornell University**
Professor Zhiru Zhang *January 2015 - May 2015*
Developed, simulated and analyzed arbitration techniques to mitigate covert side channels for shared hardware accelerators using Vivado HLS targeting FPGAs.

Distributed Low-Cost Smart Power Sensors with Decentralized Control **Cornell University**
Professor Eilyan Bitar *May 2013 - August 2013*
Designed hardware for low cost, high sample rate, distributed power sensors with decentralized control. Implemented AMQP messaging framework in C for high frequency communication and a stratum 1 time server on the Raspberry Pi by synchronizing NTP with an interrupt based PPS coming from an off-chip GPS module. Interfaced the Raspberry Pi with hardware peripherals including multiple ADC's using SPI Bus and the off-chip GPS module. Aided with circuit design and algorithm development for characterizing power signal from outlets.

Teaching Experience

Undergraduate Teaching Assistant **Cornell University**
ECE 3140 - Embedded Systems *1 semester*

Undergraduate Teaching Assistant **Cornell University**
ECE 2300 - Digital Logic Design and Computer Organization *3 semesters*

Online Course Design - The Computing Inside Your Smart Phone **Cornell University**
Professor David H. Albonesi *May 2014 - September 2014*

Service

Student Chapter President, Corporate Director **Cornell University**
Cornell IEEE *October 2013 - Present*
Leading the Cornell IEEE executive board (25 students) to organize corporate and social events for the Cornell ECE community including: information sessions, technical talks, professor talks, corporate game nights with over 200 engineers and 8 companies, hardware hackathons, student socials and ECE department sponsored events.

Project Experience

Medi-Bot: Personalized Autonomous Medicine Delivery Robot **Cornell University**
Digital System Design using Microcontrollers Project *October 2015 - December 2015*
Designed and prototyped a personal robot that delivers medicines on a user programmable schedule. The user interfaces with Medi-Bot's processing core, PIC32 microcontroller, using an Android phone over Bluetooth. Integrated Bluetooth HC-05 module, external oscillator for high precision timing, motor controllers and LCD TFT screen with PIC32 microcontroller.

Modeling On-Die Termination Power Overhead of Encrypted Data **Cornell University**
Resilient Computer Systems Class Project *March 2015 - May 2015*
Modeled the effects of memory encryption on link termination and signal reflections for DDR4 memory technologies. Using MiBench and Pin, a dynamic binary instrumentation tool, we simulated the effects of encrypting data on Data-Bus Inversion memory systems.

Master Slave Batcher Network for Resolving Interleaved Memory Accesses **Cornell University**
Digital VLSI Design Class Project *April 2015 - May 2015*
Designed and implemented an 8-bit, 8-input master-slave batcher network with 2 input and 4 input sorting units for resolving sort order and inverse sort order for addresses. Implemented a Python based test generation system to automatically generate Verilog-A based test harness for Cadence (Virtuoso) Schematic Simulations.

Relevant Coursework

Advanced Computer Architecture, Resilient Computer Systems, Computer Architecture
Complex Digital ASIC Design, Digital VLSI Design
Digital Systems Design Using Microcontrollers, Emebedded Systems, Evolutionary Algorithms
Operating Systems, Data Structures and Functional Programming, Object Oriented Programming, Discrete Structures

Online and Audited Classes

High Level Design Automation, Machine Learning, Introduction to Parallel Programming
Six Sigma Yellow Belt Certification