Udit Gupta

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Education

Harvard University
PhD Computer Science, GPA - 3.87 *2016-Present*

Cornell University
Bachelor of Science, GPA - 4.00 *2012-2016*
Dean's List (All Semesters)
Major: Electrical and Computer Engineering
Minor: Computer Science

Research Interests

Hardware / software co-design and design automation for hardware specialized **deep learning** focusing on performance and energy efficiency in the context of datacenter and mobile systems

Honors and Awards

Harvard Smith Family Fellowship *2017*
National Science Foundation GRFP Honorable Mention *2016*
Richard A. Newton Young Fellows Scholarship *May 2015 - June 2015*
Cornell ECE Early Research Career Scholarship *May 2013 - September 2013*
Eta Kappa Nu - Electrical Engineering Honor Society *October 2013 - Present*

Conference and Workshop Publications

Steve Dai, Ritchie Zhao, Gai Liu, Shreesha Srinath, **Udit Gupta**, Christopher Batten, Zhiru Zhang.*Dynamic Hazard Resolution for Pipelining Irregular Loops in High-Level Synthesis*. 25^{th} ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2017)

Mingxing Tan, Steve Dai, **Udit Gupta** and Zhiru Zhang. *"Mapping-Aware Constrained Scheduling for LUT-Based FPGAs"*. 23^{rd} ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2015)

Technical Articles and Presentations

Udit Gupta *"Software Programmable FPGAs"*. Circuit Cellar, "Tech the Future" series (July 2016)

Steve Dai, **Udit Gupta** and Ritchie Zhao.. *"Towards High-Level Programming for FPGAs"*. Cornell Computer Systems Lab (November 2014)

Research Experience

Heterogeneous Parallel Computing using High Level Synthesis **Cornell University**
Professor Zhiru Zhang *December 2013 - Present*
Investigating irregular applications and hardware-software abstractions to accelerate designs on reconfigurable accelerators. Exploring high-level programming methodologies using architectures, languages and compilers to improve design productivity and efficiency of system-on-chips and polymorphic specialization of data structures and algorithms. Accelerating and analyzing key applications using OpenCL and C/C++ enabled high level synthesis tools with respect to latency, throughput and area utilization.

Mitigating Timing Channels for Shared Hardware Accelerators **Cornell University**
Professor Zhiru Zhang *January 2015 - May 2015*
Developed, simulated and analyzed arbitration techniques to mitigate covert side channels for shared hardware accelerators using Vivado HLS targeting FPGAs.

Professional Experience

Hardware Design and Verification Engineering Intern **Santa Clara, CA**
Algo-Logic Systems *May 2015 - August 2015*

Designed OpenCL board support package for clients to develop and integrate software kernels with existing low latency network IP for the Tick-to-Trade system. Developed software interface for configuring FPGA and OpenCL financial data parsers and trading algorithms.

Teaching Experience

Undergraduate Teaching Assistant — **Cornell University**
ECE 3140 - Embedded Systems — *1 semester*

Undergraduate Teaching Assistant — **Cornell University**
ECE 2300 - Digital Logic Design and Computer Organization — *3 semesters*

Online Course Design - The Computing Inside Your Smart Phone — **Cornell University (EdX)**
Professor David H. Albonesi — *May 2014 - September 2014*

Project Experience

Medi-Bot: Personalized Autonomous Medicine Delivery Robot — **Cornell University**
Digital System Design using Microcontrollers Project — *October 2015 - December 2015*
Designed and prototyped a personal robot that delivers medicines on a user programmable schedule. Published, "Medi-Bot: Your Personal Medicine Botler", in Circuit Cellar's December 2016 issue.

Modeling On-Die Termination Power Overhead of Encrypted Data — **Cornell University**
Resilient Computer Systems Class Project — *March 2015 - May 2015*
Modeled the effects of memory encryption on link termination and signal reflections for DDR4 memory technologies. Using MiBench and Pin, a dynamic binary instrumentation tool, we simulated the effects of encrypting data on Data-Bus Inversion memory systems.

Master Slave Batcher Network for Resolving Interleaved Memory Accesses — **Cornell University**
Digital VLSI Design Class Project — *April 2015 - May 2015*
Designed and implemented an 8-bit, 8-input master-slave batcher network with 2 input and 4 input sorting units for resolving sort order and inverse sort order for addresses. Implemented a Python based test generation system to automatically generate Verilog-A based test harness for Cadence (Virtuoso) Schematic Simulations.

Professional Activities

Student Chapter President, Corporate Director — **Cornell University**
Cornell IEEE — *October 2013 - Present*
Leading the Cornell IEEE executive board (28 students) to organize corporate and social events for the Cornell ECE community including information sessions, technical talks, professor talks, corporate game nights with over 200 engineers and 8 companies, hardware hackathons, student socials and ECE department sponsored events.

Executive Board Member — **Cornell University**
Cornell Eta Kappa Nu (HKN) — *October 2013 - Present*