An 86% efficiency Multi-Phase Buck Converter using Time-Domain Compensator and Adaptive Dead-Time Control for DVS Application

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***Abstract*—A high-frequency switching, multi-phase buck converter capable of nanosecond-scale Dynamic Voltage Scaling (DVS) is reported in this work. The proposed converter employs a time-domain compensator using VCOs and Voltage Controlled Delay Lines (VCDL). The closed loop bandwidth of the converter is scaled with the active number of phases by adjusting the control parameters in the compensator. In addition, this paper also proposes a digital-intensive adaptive dead-time controller that helps to minimize unwanted body diode conduction/short circuit losses occurring in the power switches. A test chip fabricated in 55nm CMOS technology generates an output voltage of 0.6-1.2V from a 1.8V supply. A thin-film magnetic inductor with an inductance of 38nH and a quality factor of 14 along with a 10nF capacitor, filters the switching pulses at the output. Proposed design achieves a peak efficiency of 86% and delivers an output power up to 1.8W. This work is able to produce higher output current up to 1.5A and a larger output slew-rate of >4Vμ/s than the state-of-the-art while switching at only 50MHz.**

I. Introduction

Integrated Voltage Regulators (IVR) are instrumental in implementing fast Dynamic Voltage and Frequency Scaling (DVFS) in SoCs [1],[2]. IVR necessitates the high frequency operation of the voltage regulators so that the size of the output filter could be reduced. To achieve a fast transient response IVR also requires a fast controller which can provide large closed-loop bandwidth well into the MHz range. Even though Op-amp based PI controllers and digital compensators are a popular choice in voltage regulators, using them in fast switching regulators require high speed analog circuitry/digital logic that makes the design more complex and power hungry [3]. Time-domain controllers that are analog in time and digital in voltage are good alternatives [4],[5]. In this work, we employed a time-domain controller for compensation as well as to generate multi-phase PWM pulses. In order to effectively minimize the output ripple, the PWM switching pulses are spaced according to the number of active phases. The free running frequency of the VCO and the loop coefficients are adjusted to maintain a constant switching frequency as well as to scale the closed loop bandwidth with different number of phases.

In switching regulators, the gate pulses for PMOS and

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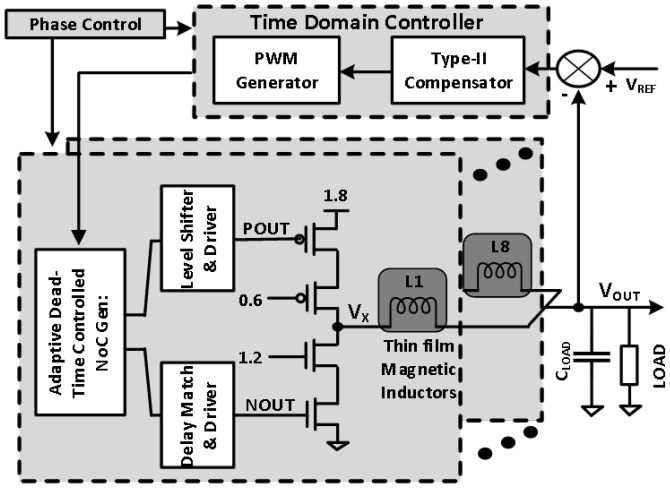

Fig. 1. Architectural block diagram for the proposed converter.

TABLE I
TARGET SPECIFICATIONS FOR BUCK CONVERTER

V_{IN}	V_{OUT}	I_{LOAD}	F_{SW}	L	C	BW
1.8V	0.6-1.2V	1.5A	50MHz	38nH	10nF	10MHz

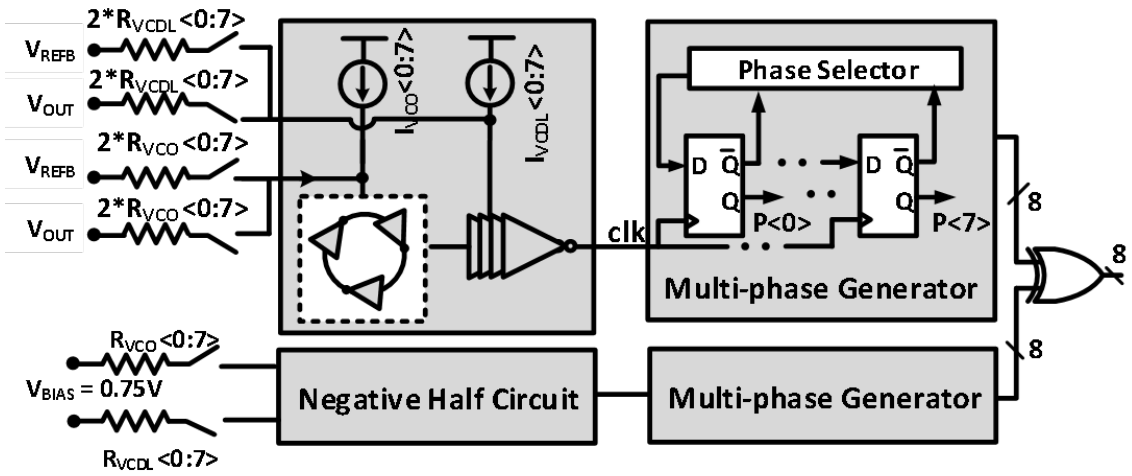

Fig. 2. Schematic diagram for time-domain compensator and multiphase generator.

NMOS switches are kept non-overlapping to avoid any short circuit loss. If the non-overlapping dead-time is too large, the body-diode of the NMOS starts conducting, leading to additional losses. On the other hand, if the dead-time is too small, it may result in short circuit losses due to any PVT variation. Thus an adaptive dead-time controller is desirable for efficient operation. In high frequency switching regulators, the dead-time is of the order of pico-seconds which require high-speed analog circuitry for adaptive dead-time generation. In this paper, we propose a digital-intensive, adaptive dead-time controller, which can adjust itself to PVT conditions thereby improving the conversion efficiency.

II. Proposed Buck Converter using Time-Domain Type-II Controller and Adaptive NOC

A. Architecture for the Multi-Phase Buck Converter

Fig. 1 shows the architectural block diagram of the proposed multi-phase buck converter, where the number of phases can be varied between 1 to 8 and the phases are magnetically decoupled. This topology offers several benefits such as uniform efficiency over the targeted load current range, smaller output filters, faster transient response, etc. The target specification of the converter is given in Table-I. Thin-film magnetic inductors are used since they provide higher quality factor and a larger inductance as compared to the air-core inductors. The measured frequency response for the in-house developed inductor is plotted in Fig. 3 [6],[7]. It has 38nH inductance and a peak quality factor of 14 in the frequency range of 50-80MHz. System simulations showed that maximum conversion efficiency is obtained for a per phase current of 125mA while switching at 50MHz. A 10nF output capacitor was chosen for maintaining the output ripple within 100mV. As the input voltage exceeds the VDS breakdown voltage of the switches during the off state, cascode devices biased with fixed voltage were added. At light loads, when only single phase is activated, LC pole frequency (8MHz) is comparable to that of the targeted loop bandwidth, a type-II compensator was chosen for improved phase margin. Time-domain controller using VCOs and VCDL not only realizes the integral and proportional control, but also generates the PWM switching pulses. Non-overlapping deadtime between the control pulses for the NMOS and PMOS switches is adaptively controlled by the proposed dead-time controller for improved efficiency.

B. Time-Domain Type-II Compensator

Fig. 2 illustrates the block diagram representation of the time-domain controller. The relationship between input voltage and output phase of the VCO is used

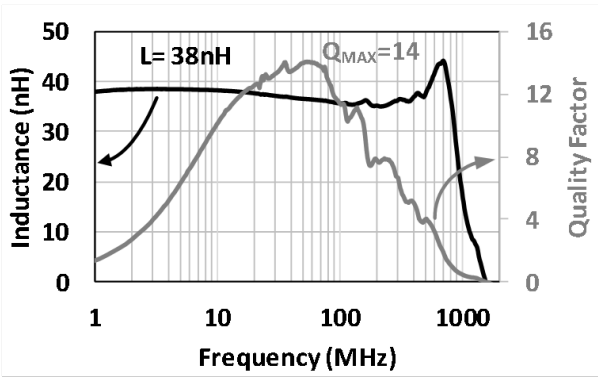

Fig. 3. Measured Inductance and Q factor for the thin film magnetic inductor vs. frequency.

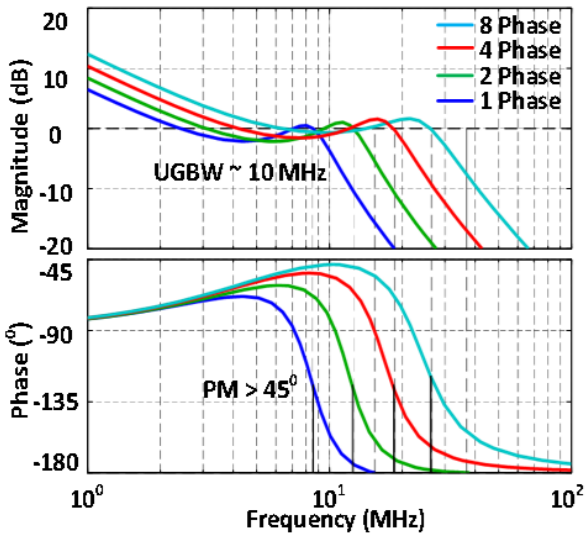

Fig. 4. Loop gain frequency response of the voltage regulator for different phases.

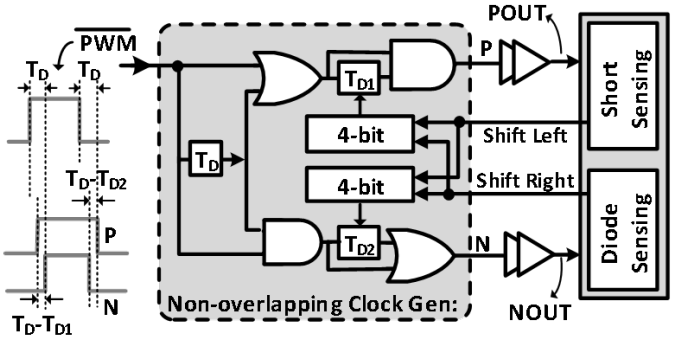

Fig. 5. Block diagram for adaptive dead-time controller and related waveforms.

for the integral control. The VCDL delays the VCO pulses according to the control voltage thus acting as the proportional control. The transfer function of the controller, H(s), is given as follows:

$$H(s) = (K_{VCO}/s + K_{VCDL})/(1 + s/\omega_p) \quad (1)$$

where K_{VCO} (rad/s/V) is the frequency gain of the VCO, K_{VCDL} (rad/V) is the gain in the phase and ω_p is a high frequency pole at the input of the VCO. One half of the controller consisting of a VCO and a VCDL generates the reference phase with a fixed input voltage of 0.75V. The other half of the controller, generates the feedback phase from a signal that is obtained from the resistive sum of a reference voltage and the feedback voltage. A phase detector (XOR gate) senses the difference between the reference phase and the feedback phase generating a PWM signal. In steady state, the closed loop feedback

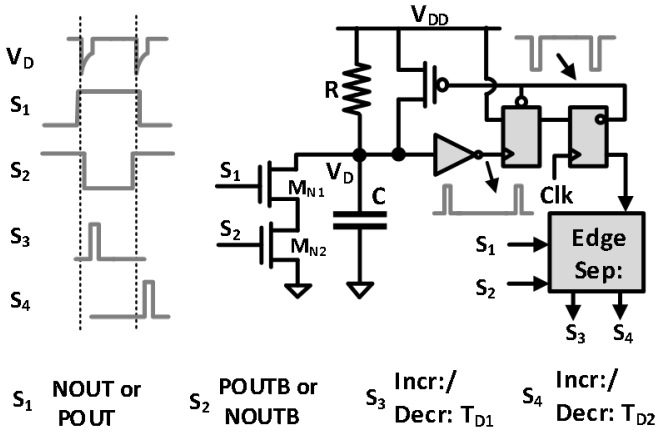

Fig. 6. Short circuit/body diode conduction sensing circuitry.

forces the mean value of the resistive sum, (V_{REFB} + V_{OUT})/2, to 0.75V.

VCO in Fig. 2 is a 3-stage ring oscillator made of CMOS differential inverters. Current source, I_{VCO}, sets the free running frequency of the oscillator and the input resistor, R_{VCO}, sets the K_{VCO}. R_{VCDL} and bias current I_{VCDL} together set the value of K_{VCDL}. Multi-phase generator divides the VCO frequency according to the number of phases enabled. This ensures that the PWM pulses are spaced equally for effective ripple reduction. For maintaining a constant switching frequency of 50MHz for different number of phases, the free running frequency of the VCO is scaled using current bias $I_{VCO}\langle 0:7\rangle$. As the number of phases increase, the effective inductance decreases, thereby pushing the LC output pole further to the right. The proportional and integral gain of the compensator is scaled with increase in number of phases in such a way that bandwidth of the converter increases while keeping phase margin intact. This is achieved by scaling the values of R_{VCO}, I_{VCDL} and R_{VCDL}, with different number of phases. The loop gain frequency response of the voltage regulator for different number of phases is shown in Fig. 4.

C. Proposed Adaptive Dead-Time Controller

Diode conduction or short circuit in the switches can be detected by monitoring the gate pulses for PMOS and NMOS devices (signals "POUT" / "NOUT" in Fig. 5). For instance, any overlap between POUT and NOUTB, indicates a diode conduction in the respective edge. Similarly, overlapping POUTB and NOUT indicates a short circuit conduction. The proposed architecture in Fig. 5 uses this principle to find the smallest possible dead-time that merely avoids any short circuit conduction.

As shown in Fig. 5, the Non-Overlapping Clock (NOC) block generates non-overlapping pulses 'P' and 'N'.

The non-overlap delays at respective rising and falling edges are $T_D - T_{D1}$ and $T_D - T_{D2}$, where T_D is a fixed delay and T_{D1} and T_{D2} are variable delays. Each delay element comprises of a pair of CMOS inverters having a delay of around 100ps. The variable delay elements are controlled by a 16-bit shift register that shifts left or right thereby decreasing or increasing delays, respectively. A novel sensing block (detailed schematic in Fig. 6) monitors the diode conduction/short-circuit using the overlap information from POUT and NOUT signals. For every diode conduction sensed, the dead-time is decreased and for every short circuit detected the dead time is increased. The non-overlapping pulses 'P' and 'N', propagates through level shifters and a series of drivers to obtain the gate signals 'POUT' and 'NOUT'. To mitigate the variations and mismatches in these propagation delays, range of non-overlap delays for 'P' and 'N' is set from -0.5ns to 1ns.

To detect the overlap in POUT and NOUT signals (which could be in pico-seconds) a novel short circuit and diode conduction circuitry is proposed (Fig. 6). The circuit operation for short circuit detection is as follows. Under normal conditions either one of the switches M_{N1} and M_{N2} are off and the capacitor C is fully charged to VDD through resistor R. In the event of diode conduction, the overlap between POUT and NOUTB causes M_{N1} and M_{N2} to conduct and discharge the capacitor momentarily, resulting in a narrow pulse at the node V_D. Since the width of the resulting pulse is undefined, a flipflop arrangement is used to latch the event and to generate a pulse with a finite width (1/Clk) as shown in Fig. 6. Edge separator block separates the edge event by drawing a bounding window between POUT rising and NOUTB rising and vice versa. These pulses shifts the 4-bit registers in Fig. 5 to the right thus decreasing the dead-time. A replica of this circuit is used for detecting body diode conduction by changing NMOS inputs to POUTB and NOUT. Sensitivity of short circuit detection is increased in comparison to diode conduction detection by choosing a larger value of R.

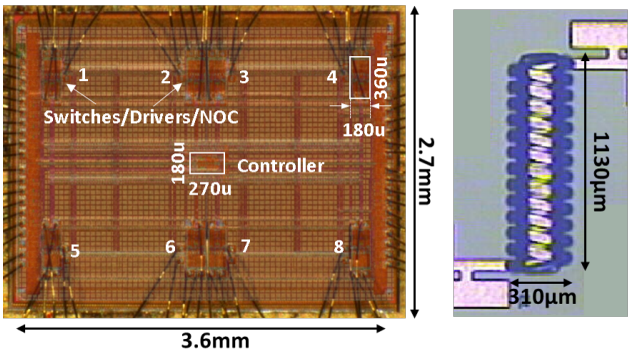

Fig. 7. Die photograph of the test chip and thin-film magnetic inductor.

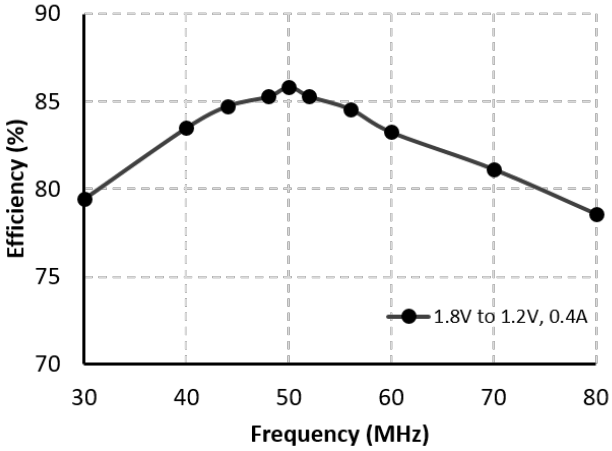

Fig. 8. Efficiency versus frequency for 1.8V to 1.2V conversion with a load of 0.4A.

III. Measurement Results

Die photograph of the test chip fabricated using 55nm CMOS technology and that of a thin-film magnetic inductor developed in-house is depicted in Fig 7. Total die size is 3.6mm x 2.7mm, however the active area occupied by controller and switches is only 0.64mm^2. Rest of the area is filled by decoupling capacitors for maintaining clean power supplies. Inductor occupies an area of 0.35mm^2. The test chip and eight inductors were wire-bonded to the PCB side by side using chip-on-board (COB) method. Input supply (1.8V) and supply for the drivers/control logic (1.2V/0.6V) were provided using external sources. Fig. 8 shows the efficiency at various switching frequencies of a 2-phase converter powering 0.4A load. It shows the peak efficiency is obtained at 50MHz switching, which is used for the subsequent characterization. Fig. 9(a) plots the measured conversion efficiency for the test chip against the load current for different output voltages. For a given load current and switching frequency, the efficiency reduces with the output voltage. For the given output voltage, the number of active phases are manually enabled/disabled depending on the load current. As multiple-phases are enabled/disabled, the efficiency is fairly flat across load currents from 0.1A to 1.5A.

The test chip measurements using a fixed deadtime were carried out to observe the effectiveness of the proposed adaptive deadtime controller. The fixed dead-time used was 0.75ns after considering the margins for

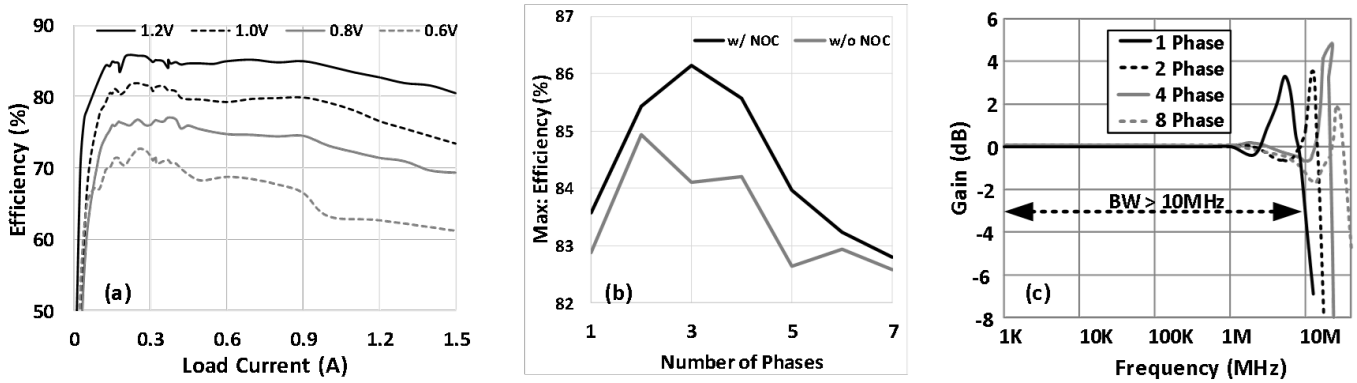

Fig. 9. (a) Efficiency vs Load Current for different output voltage, (b) Efficiency with and without adaptive NOC, and (c) Measured closed loop bandwidth.

TABLE II
COMPARISON WITH OTHER STATE-OF-THE-ART

Parameter		[8]	[3]	[5]	[9]	[10]	This Work
Process	(nm)	40	14	65	14	45	55
Inductor Technology	-	COTS (Interposer)	Magnetic (on-chip)	NA	Air-Core (package)	3D Interposer	Magnetic (Thin Film)
Input Voltage	(V)	3.3	1.5	1.8	1.6	1.66	1.8
Output Voltage	(V)	1.2-2.4	1.15	0.6-1.5	1.2	0.833	0.6-1.2
Switching Frequency	(MHz)	100	100	30-70	70	150	50
Output Filter	L(nH), C(nF)	60, 16	1.5, 5	90, 470	2.5, 160	7, 70	38, 10
Output Slew Rate	$(V/\mu s)$	NA	0.75	NA	2.5	5	$> 4^*$
Max Load Current	(A)	0.15	0.36	0.8	0.5	0.39	1.5
Max Efficiency	(%)	91.5	84	87	88	82	86

* Limited by the reference slew rate,

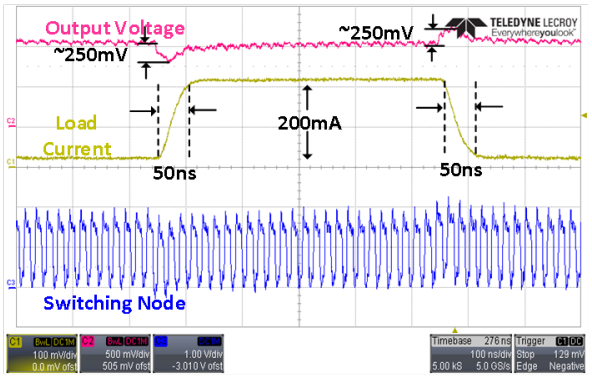

Fig. 10. Measured Load transient response.

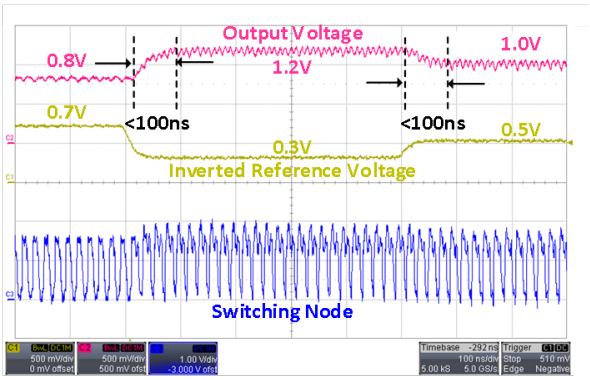

Fig. 11. Measured response to emulated DVS.

PVT variations. Fig. 9(b) plots the maximum conversion efficiency of the controller for different number of active phases with and without proposed scheme. It is evident from the measured results that the efficiency using the proposed scheme is better for any given number of phases. Fig.9(c) plots the closed loop bandwidth of the converter for multiple phases. The proposed design could attain bandwidth >10MHz for all the phases of operation. Upon enabling all the phases the regulator achieves a bandwidth of 25MHz. Due to limitations in the test setup, a transient of 200mA is obtained with 2 phases enabled. Fig. 10 shows the measured load transient of 200mA. Despite relying only on the on-chip output capacitor, the output voltage drop is within 20% of the output voltage. The voltage drop can be reduced by further optimizing the output filter. Fig. 11 illustrates

measured results for emulated DVS. The design achieves a transient time of less than 100ns for a change in output from 0.8V to 1.2V. Table II shows the comparison for the proposed regulator with that of other reported works. This work is able to produce higher output current, larger output slew-rate than the state-of-the-art while operating at a relatively lower switching frequency.

IV. Conclusion

We proposed a multi-phase buck converter switching at 50MHz that uses a time-domain compensator and adaptive deadtime controller. The converter achieved peak efficiency of 86% and an output slew rate of 4V/μs. The proposed voltage regulator and the thin-film magnetic inductors implemented using CMOS BEOL process could potentially be used for realizing IVRs in SoCs featuring DVFS.

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