A Max 2.3μA Quiescent Current External Capacitorless Low-Dropout Regulator

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***Abstract*—The paper presents an external capacitorless low-dropout regulator (LDO) with a ultra-low quiescent current for system-on-chip (SoC) in portable electronic applications. A sub-1-V, nanopower voltage reference ensures the low power consumption of the LDO system. The external capacitorless design allows the LDO to be fully integrated on chip, which not only saves area and cost, but also eliminates bond-wire effects. In order to compensate the lack of large off-chip output capacitor, a two-stage error amplifier with nested Miller compensation is applied to ensure system stability. Besides, a small on-chip output capacitor and a slew-rate enhancement circuit are attached to improve transient response. The proposed LDO is designed and simulated in 55 nm process. Compared with prior works, this LDO has the minimum output capacitor of 5pF and the ultra-low quiescent current of 2.3μA with load regulation of 0.41mV/mA and figure-of-merit (FOM) of 1.95.**

Keywords—low quiescent current; external capacitorless

I. INTRODUCTION

For portable applications like mobile phones, tablet computers, and sports bracelets, low power consumption is a very critical requirement to extend their battery life. Hence, low voltage and low quiescent current have been desirable in power management design. Among all kinds of power management chips, LDO plays an important role for its advantages of low noise, small ripple and no EMI interference. Conventional LDOs have off-chip output capacitors, which not only cost large chip area for the pads and ESD circuits needed, but also impact the output voltage performance due to bond-wire effects. While on-chip LDOs, on the contrary, not only reduces chip area and cost, but also eliminate the parasitic and antenna effects of thebonding wire. Furthermore, an on-chip LDO can be fully integrated as an IP for digital chips.

As for a LDO with a large off-chip output capacitor, say 1μF, small ripples due to load transients can be achieved and bandwidth can be extended using techniques like load-current dependent boost current [1], dynamically-biased buffer impedance attenuation (BIA) [2], adaptively-biased super current mirror [3], and multiple small-gain stages in nanometer processes [4]; and high PSR can be achieved using feed-forward ripple cancellation techniques [5]. However, for fully-integrated LDOs, large load capacitors are no longer available, and both transient response and PSR will degrade. Still small form factor and low cost are the driving forces for full integration. In recent years, removing the use of external components for fully integrated LDOs has been a key trend. Younghyun Lim [6] proposes an adaptive supply-ripple cancellation (ASRC) technique to achieve an external capacitorless LDO with high PSR from 10kHz to 1GHz. Somnath Kundu [7] implements a beat-frequency (BF) quantizer for a fully integrated digital LDO. Sau Siong Chong [8] presents a min 0.9μA quiescent current output-capacitorless LDO with adaptive power transistors.

This paper presents a max 2.3μA quiescent current external capacitorless low-dropout regulator for highly-integrated SoCs in portable applications. The proposed topology is shown in Fig. 1. A sub-1-V, nanopower bandgap voltage reference is implemented by using transistors with different threshold voltages. A two-stage structure with an error amplifier and an impedance attenuation buffer is adopted to guarantee the system stability. Also a small on-chip capacitor C_L and nested Miller compensation consisting of C_{m1} and C_{m2} are applied to compensate the lack of off-chip output capacitor. Moreover, a slew-rate enhancement circuit is applied to improve the transient response.

The rest of the paper is organized as follows. Section II presents the particular circuit implementation of the external capacitorless low-dropout regulator. Section III shows the system simulation results. Finally, Section IV draws the conclusions.

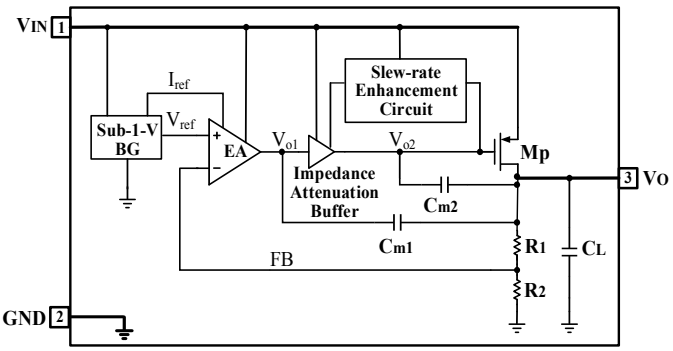


Fig. 1 Proposed topology of the external capacitorless low-dropout regulator

II. PARTICULAR CIRCUIT IMPLEMENTION

A. Sub-1-V Bandgap voltage reference

Conventional bandgap reference has good performance over process in supplying voltage and temperature (PVT) variations. However, its output voltage is fixed over 1.2V, which is too high for low-voltage applications [9]. A low-voltage structure providing sub-1-V output reference is presented in [10]. It contains a two-stage op-amp and large resistance, which is complicated and occupies large area . An

innovative way to implement voltage reference with nanopower consumption can be realized without resistor [11]. But it has good temperature characters in limited temperature range.

In this paper, a sub-1-V, nanopower and small-area CMOS voltage reference without resistor or BJT transistor is presented. The schematic of the proposed bandgap voltage reference is shown in Fig. 2, containing 3 parts as start-up, current generator and active load. The start-up circuit formed by $M_{1S} - M_{4S}$ is adopted to ensure the correct stable state. The circuit formed by transistors numbered from M_1 to M_{11} generates a current I_1, which is then copied to the active load to generate a temperature-compensated reference voltage V_{ref}.

As is known, the I-V characteristic of an NMOS transistor in saturation region can be approximated by the expression

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (1)$$

where μ is the electron mobility in the channel, C_{OX} is the oxide capacitance per unit area, V_{th} is the threshold voltage, and W and L are the channel width and length, respectively. Here we define $k_i \equiv \mu C_{ox}(W_i/L_i)$ where the subscript i associates any quantity to transistor Mi. Since the NMOS M_{15} works in saturation region, the output reference voltage V_{ref} can be obtained as

$$V_{ref} = V_{th15} + \sqrt{\frac{2I_1}{k_{15}}} \quad (2)$$

where I_1 is the bias current of M_{15}, V_{th15} is the threshold voltage of M_{15}. Since $V_{th} \propto$ (-T) and $k_{15} \propto \mu(T)$ [11], where T is the absolute temperature and $\mu(T)$ is the temperature-dependent mobility of transistor. In order to achieve a temperature-independent V_{ref}, a bias current proportional to mobility and to the temperature squared, that is, $I_1 \propto \mu(T)T^2$, is required.

So transistors with different threshold voltages are used in the proposed bandgap circuit to meet temperature characteristics. M_2 and M_4 have higher threshold voltage (0.64V) while other NMOS transistors are 0.43V threshold voltage. By enforcing $V_{GS1} = V_{GS2}$, $V_{GS3} = V_{GS4}$ by circuit, the gate voltages of M_1-M_4 are set between 0.43V and 0.64V, where a pair of transistors operating in subthreshold region and the other in saturation region are obtained. The I-V characteristic of M_1 and M_3 in saturation region adheres to (1) while M_2 and M_4 in subthreshold region follows

$$I_D = \mu C_{ox} V_T^2 \frac{W}{L}\exp(\frac{V_{GS}-V_{th}}{mV_T})[1 - \exp(-\frac{V_{DS}}{V_T})] \quad (3)$$

where V_T is the thermal voltage and m is the subthreshold slope parameter. Here goes

$$V_{th1} + mV_T\ln(\frac{I_1}{\mu C_{ox}V_T^2 W_1/L_1}) = V_{th2} + \sqrt{\frac{2I_2}{\mu C_{ox}W_2/L_2}} \quad (4)$$

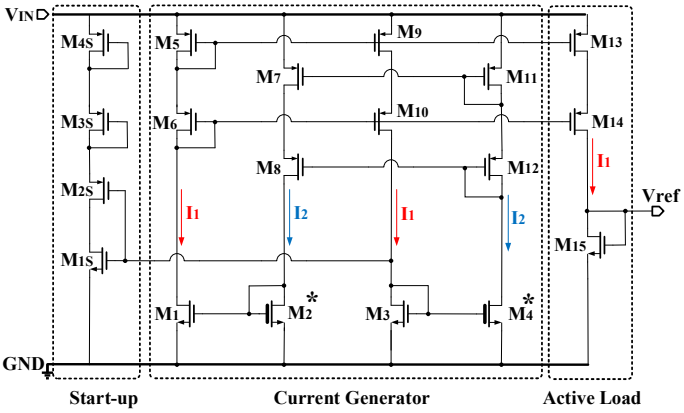
$$V_{th3} + mV_T\ln(\frac{I_1}{\mu C_{ox}V_T^2 W_3/L_3}) = V_{th4} + \sqrt{\frac{2I_2}{\mu C_{ox}W_4/L_4}} \quad (5)$$

By subtracting (4) from (5), the expression of the current I_1 can be extracted as

$$I_1 = \frac{\mu C_{ox}W_3/L_3}{2(N-1)^2} m^2 V_T^2 \ln^2(\frac{W_4/L_4}{W_2/L_2}) \quad (6)$$

where $N \equiv \sqrt{(W_3/L_3)/(W_1/L_1)}$. Hence the desired I_1 is obtained for the temperature-compensated voltage V_{ref}.

Fig. 3 shows the voltage reference V_{ref} when the temperature changes. V_{ref} is 656mV at room temperature. And the variation of V_{ref} is 29.7mV with temperature ranging from -50 ℃ to 100 ℃, whose temperature coefficient is 30ppm/℃. Also to reduce the input voltage impacts, cascode PMOS transistors are added in the proposed bandgap circuit for their shielding characteristics [12]. With input voltage V_{IN} changing from 1.4V to 2.4V, the variation of bandgap voltage reference Vref reduces from 43mV to 26mV after adding cascode transistors. The typical output voltage reference is 665mV at V_{IN} = 1.8V with 90nA supply current. This proposed sub-1-V, nanopower bandgap makes it feasible to build an ultra-low power LDO.



*: higher threshold voltage (0.64V), others: 0.43V

Fig. 2 Proposed sub-1-V bandgap voltage reference circuit

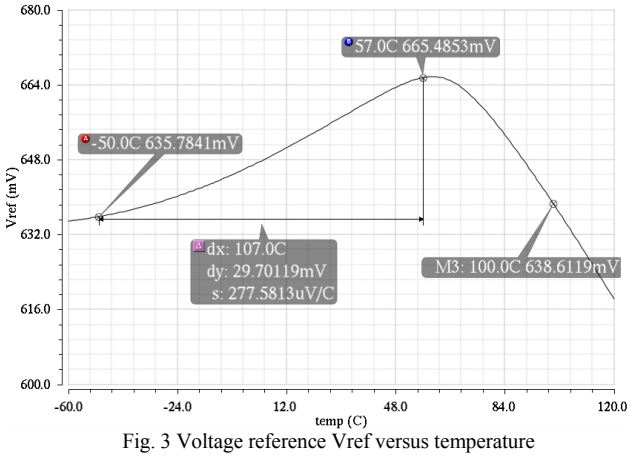


Fig. 3 Voltage reference Vref versus temperature

B. Two-stage error amplifier with slew-rate enhancement and nested Miller compensation

A two-stage structure with slew-rate enhancement and nested Miller compensation is adopted for the LDO error amplifier, as shown in Fig. 4. The first stage is a PMOS input pair differential amplifier. The second stage is an impedance attenuation buffer, which has a smaller output impedance in comparison with conventional buffer. Hence it can not only guarantee system stability by pushing the pole caused by the power gate away from the unit bandwidth, but also enhancing the transient response. As when the load current goes up, the node N_3, also the gate of power transistor M_P, will discharge through M_{27} with small output impedance, therefore M_P's gate

voltage decreases rapidly, speeding up the raise of the load current.

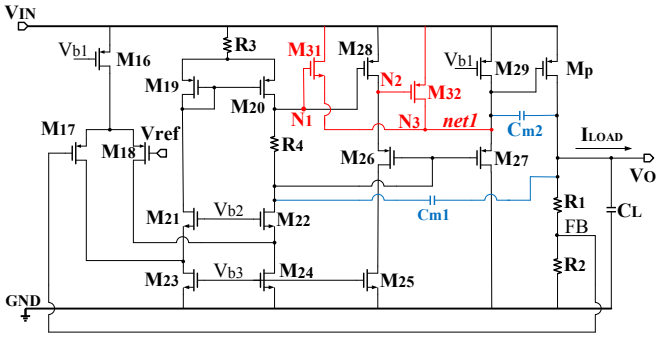


Fig. 4 The schematic of the two-stage error amplifier with slew-rate enhancement and nested Miller compensation

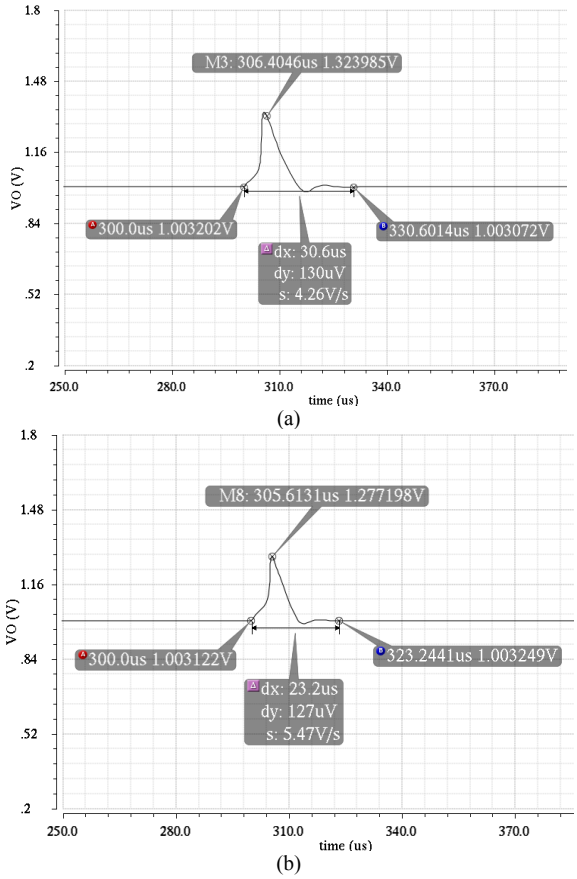


Fig. 5 Transient response of output voltage Vo when load current I_{LOAD} falls from 1mA to 0.02mA (a) without slew-rate enhancement circuit; (b) with slew-rate enhancement circuit

To improve transient performance when load current goes down without increasing quiescent current, a slew-rate enhancement circuit consisting of M_{31} and M_{32} is applied to the circuit. During steady state, M_{31} and M_{32} are shut down without additional quiescent current. When the load current falls, the voltage of node N_1 increases while N_2 decreases, which respectively turning on M_{31} and M_{32}, increasing the current flowing in *net1*. Thereby the node N_3, which is also the gate of the power transistor M_P, is charged quickly, helping reduce the load current recovery time. Fig. 5 shows the improvement of the slew-rate enhancement circuit, which shortens the recovery time from 30.6μs to 23.2μs as well as lowers the overshoot voltage from 323mV to 277mV when load current falls from 1mA to 0.02mA.

In addition, with nested Miller compensation of C_{m1} and C_{m2}, system stability is strengthened as it can lower the dominant pole and raise the two non-dominant roles at the same time compared with traditional one-capacitor Miller compensation. Here C_{m1}=1.5pF, C_{m2}=350fF.

III. System Simulation Results

The proposed low quiescent current and external capacitorless LDO is implemented in SMIC 55nm process, whose on-chip output capacitor C_L is only 5 pF.

The output voltage V_O is 1.0V with input voltage V_{IN} ranging from 1.4V to 2.4V. The maximum load current I_{LOAD} is 1.0mA. The maximum quiescent current Iq is 2.3μA at I_{LOAD}=1.0mA, shown in Fig. 6. Fig. 7 presents the curve of Vo versus I_{LOAD}, from which the load regulation of 0.41mV/mA can be calculated. Fig. 8 shows the variation of Vo with V_{IN} from 1.4V to 2.4V, with the line regulation of 47.6mV/V. Fig. 9 presents the transient response when I_{LOAD} jumps from 0.02mA to 1mA and from 1mA to 0.02mA. ΔV_O is 260mV with recovery time of 18μs.

Table I shows the performance comparison with prior arts. As can be seen, this work has the smallest output capacitor C_L, and the smallest quiescent current Iq. Also, its load regulation is the best among the on-chip LDOs. The figure-of-merit (FOM) as $C_L \cdot \Delta V_O \cdot Iq / \Delta I_{LOAD}^2$ can be calculated as 1.95.

TABLE I. Performance Comparison with the Prior Arts

	[13]	[14]	[15]	This work
Process (nm)	65	65	65	**55**
Output cap.	off chip	on chip	on chip	**on chip**
C_L(pF)	4700000	140	40	**5**
V_{IN} (V)	1.2	1.15	0.6-1.2	**1.4-2.4**
V_O (V)	1.0	1.0	0.4-1.1	**1.0**
Iqmax (μA)	40	90	1070	**2.3**
I_L (mA)	100	10	100	**1.0**
Load reg. (mV/mA)	0.01	1.1	0.638	**0.41**
Line reg. (mV/V)	/	37.1	168	**47.6**
ΔV_O (mV)@ ΔI_L(mA)	4(100)	82@(10)	108@(50)	**260@(1)**
FOM*(ps)	18.8	5.74	1.38	**1.95**

*FOM = $C_L \cdot \triangle V_O \cdot Iq / \triangle I_{LOAD}^2$. Smaller FoM is better.

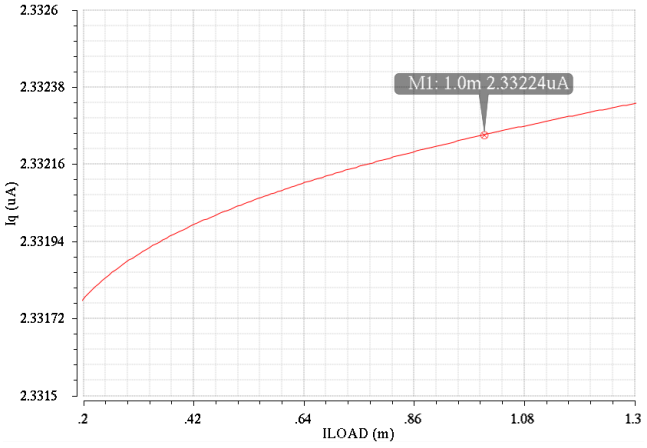


Fig. 6 Quiescent current Iq versus different load current I_{LOAD} @ V_{IN} = 2.4V

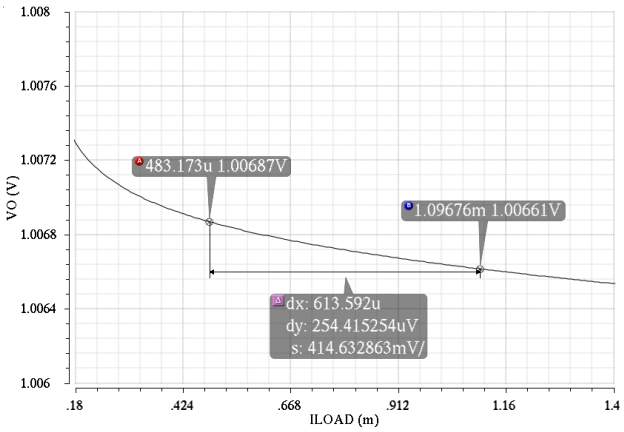


Fig. 7 LDO's output voltage V_O versus load current I_{LOAD}

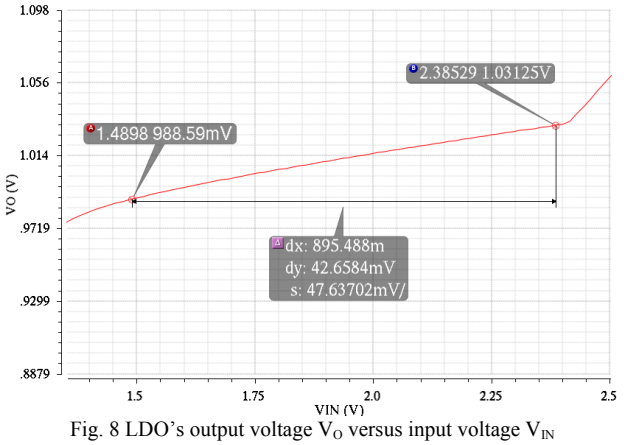


Fig. 8 LDO's output voltage V_O versus input voltage V_{IN}

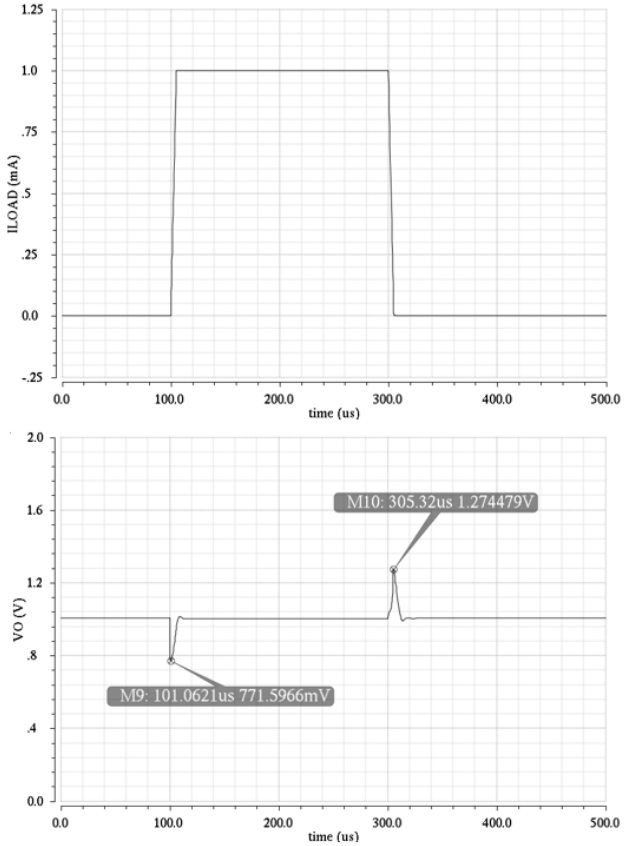


Fig. 9 LDO's transient response when the load current I_{LOAD} jumps from 0.02mA to 1mA and from 1mA to 0.02mA

IV. Conclusion

In this paper, an external-capacitorless LDO with low-quiescent-current in 55-nm CMOS process is presented. A sub-1-V, nanopower bandgap voltage reference without BJT or resistor is designed, saving both power and area. As a result, the maximum quiescent current of LDO is 2.3μA, ensuring ultra-low power consumption. What's more, a two-stage error amplifier with a PMOS input pair differential amplifier and an impedance attenuation buffer is adopted, where nested Miller compensation guarantees the system stability. And a slew-rate enhancement circuit is applied to improve transient response. The integrated on-chip output capacitor is only 5pF, which considerably saves the chip area and cost, making it appropriate for fully integrated SoCs in portable applications.

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