Thin-Film Magnetic Inductors on Silicon for Integrated Power Converters

Salahuddin Raju[1], Serine Soh, Peng Lulu, Don Disney, David Ho, Chui King Jien, Marco Stenger-Koob, Jerzy Wrona, Matthias Landmann, Berthold Ocker, Jürgen Langer, Susai Lawrence Selvaraj, M. A. Annamalai and Ravinder Pal Singh
Email: [1]salahuddin_raju@ime.a-star.edu.sg

***Abstract*—This work presents a silicon integrated high-performance thin-film inductor technology with improved magnetic core laminations. The deposition process parameters of the lamination material are tuned to obtain good quality lamination oxide, and its quality is verified by analyzing elemental composition through energy-dispersive X-ray (EDX) spectroscopy. Due to the high-quality lamination oxide, a peak quality factor of 21 and inductance to DC resistance (L/R_{DC}) ratio of 425 nH/Ohm are achieved in this inductor technology. These figure of merits represent more than 95% inductor switching efficiency in power converters, and significant improvements in quality factor (Q) and L/R_{DC} compared to other leading technologies.**

I. Introduction

The footprint of the traditional power converter is limited by the size of the energy storage devices, i.e. inductors and capacitors [1]. Increasing the switching frequencies into the 10-100MHz [2] range significantly reduces the size of these required passive components [3], such that these devices can be integrated along with the active components. Monolithically integrated air-core inductors have been proposed power conversion applications [4], [5], but such inductors suffers poor inductance density and high DC resistance. To overcome these issues, significant researches are focused on developing thin-film magnetic inductors on silicon for integrated power converters [6], [7]. For efficient power conversion, these inductors need to have high-quality factor (Q) and low DC resistance (R_{DC}). The R_{DC} can be decreased by employing thick and wide metal tracks. However, achieving high-Q for thin-film magnetic inductors is challenging due to the losses incurred in the magnetic core, especially at high switching frequencies. To improve Q, the laminated magnetic core is widely used. However, the impact of the lamination oxide quality on the inductor performance is not well understood.

This work describes the impact of magnetic core lamination on the inductor performance and developed a solution to reduce the loss incurred in the inductor core. Detailed fabrication and inductor characterization results are also presented to corroborate the proposed methodology.

This work was supported by A*STAR Science and Engineering Research Council (SERC) Grant #152 78 00039.

S. Raju, S. Soh, D. Ho, C. K. Jien, M. A. Annamalai, and R. P. Singh are with Institute of Microelectronics, A*STAR, Singapore.
P. Lulu, D. Disney, and S. L. Selvaraj are with GlobalFoundries, Singapore.
M. S. Koob, J. Wrona, M. Landmann, B. Ocker, and J. Langer are with Singulus Technologies AG, Kahl am Main, Germany.

II. Inductor Fabrication and Impact of Magnetic Core Lamination

The thin-film magnetic inductors were fabricated on 300 mm CMOS wafers using in-house fabrication facility. The fabrication starts with the Metal-1 formation via the electroplating process followed by the thick metal compatible dielectric deposition for passivation. Then the magnetic thin-film is deposited and patterned for the formation of the magnetic core. The second layer of dielectric was deposited to passivate the core followed by the contact opening for the connectivity in between Metal-1 and Metal-2. The Metal-2 is formed by the electroplating process, finishing the basic steps of the inductor formation. Another passivation layer was deposited on top of Metal-2 and, at last, selective PADs were opened for the outside connection or electrical characterization. The three-dimensional view and the cross-sectional micrograph the inductor is shown in Fig. 1. A multilayer amorphous CoZrTa thin-film was used as the magnetic core. Each layer of CoZrTa film is separated by the Cobalt Oxide (CoO), which works as the lamination oxide. The film has the relative permeability (μ_r) of >400, and resistivity of $\approx$ 100 μOhm-cm. A low coercivity (H_c) of $\approx$ 0.3 Oe and high anisotropy field (H_k) of $\approx$ 30 Oe is achieved [8], [9]. This low H_c

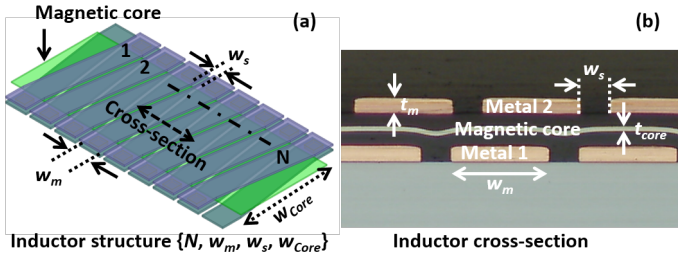


Fig. 1. (a) The three-dimensional view of a solenoidal inductor indicating the design parameters. (b) The cross-sectional image of the fabricated magnetic inductor on silicon.

ensures a negligible hysteresis loop when the inductor would be switching.

Since the magnetic core is electrically conducting, it can create a significant eddy current to reduce the performance of the inductor. The induced eddy current in the core will flow in an opposite direction to that of an inductor current, as illustrated in Fig. 2(a), and it reduces the induced magnetic field, as a result, the overall inductance reduces. This phenomenon is further illustrated using an equivalent circuit model, as shown in Fig. 2(d) [10], [11]. Here, the primary side embodies the ideal inductance and resistance of the inductor which is represented as series L_s and R_s, respectively. The secondary side embodies the eddy current induced inductance L_c and core resistance R_c. The primary and secondary side is coupled with a mutual inductance of M. Due to the induced eddy current in the core, the overall inductance reduces by $F_{eddy}L_c$, resulting in the equivalent inductance of $L_{eq} = L_s - F_{eddy}L_c$. Simultaneously, the overall resistance increases and the equivalent resistance can be expressed as $R_{eq} = R_s + F_{eddy}R_c$. Here, the eddy current loss factor F_{eddy} is the determining factor for the inductance decrement and resistance increment, and it can be represented as, $F_{eddy} = \omega^2 M^2/(R_c^2 + \omega^2 L_c^2)$. When R_c is large, F_{eddy} diminishes toward zero and the inductor will retain its ideal characteristics. This criteria can be

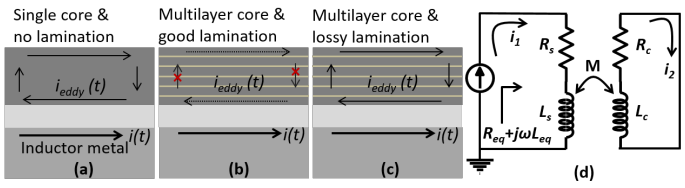
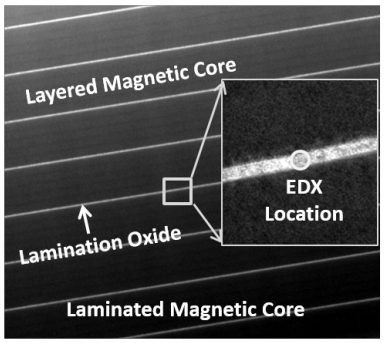


Fig. 2. A schematic illustration of eddy current flow (a) in a single layer magnetic core with no lamination, (b) in a multilayer core with good lamination, and (c) in a multilayer core with lossy lamination. (d) An equivalent circuit illustrating the impact of magnetic core lamination on the inductor performance.



Lossy Lamination Oxide

Element	Weight %	Atomic %
O K	05.50	**21.80**
Co K	61.50	66.00
Ta L	31.20	10.90
Zr K	01.90	01.30

Good Lamination Oxide

Element	Weight %	Atomic %
O K	10.70	**38.20**
Co K	48.00	46.70
Ta M	34.90	11.10
Zr L	06.40	04.00

Fig. 3. A TEM cross-sectional view of a laminated magnetic core. The inset is showing the location of EDX measurement, and the tables are showing the elemental composition of lossy and good quality lamination oxide.

fulfilled by using the laminated magnetic core where the lamination oxide blocks the eddy current conduction path in the core, as illustrated in Fig. 2(b). However, this argument does not hold true if the lamination oxide becomes lossy. The eddy current still flows through the lossy oxide, as shown in Fig. 2(c), eventually nullifying the effect of the lamination, and the effect become more severe at higher frequencies. Thus, the overall inductance and Q reduces drastically due to the poor lamination oxide.

III. Electrical Performance of the Inductor with Improved Magnetic Core Lamination

A TEM cross-sectional view of a laminated magnetic core is shown in Fig. 3. To investigate the quality of the lamination oxide, CoO, EDX measurement was performed and elemental composition is analyzed. A small percentage of oxygen implies that the Co is not fully oxidized, and there may be pinholes in the oxide, eventually, rendering a lossy lamination. In a good quality oxide, a high percentage of oxygen was observed, ensuring full oxidization of Co (Fig. 3) and this can serve as good lamination even though oxide thickness is less than 10 nm. At the beginning of the lamination process, a thin, 3 nm, layer of Co was deposited on top of the CoZrTa layer. Then the wafer was transferred into another chamber for oxygen plasma exposure to oxidize the Co. The power, gas composition, and plasma exposure time were tuned in the PVD tool during the deposition process. This isolated oxidation process helps to obtain good quality lamination oxide.

For electrical characterization, a library of inductors was fabricated with various layout parameters including N, w_m, w_s, and w_{core}, as referred to Fig. 1. The on-wafer 2-port S-parameter measurement was done using Keysight E5071C Vector Network Analyzer (VNA), then

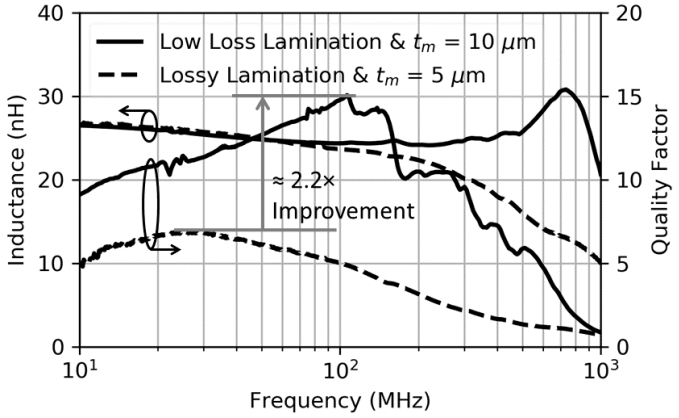


Fig. 4. Improvement of inductance performance due to good quality magnetic core lamination and thick metal process. It shows 2.2× improvement in the peak quality factor.

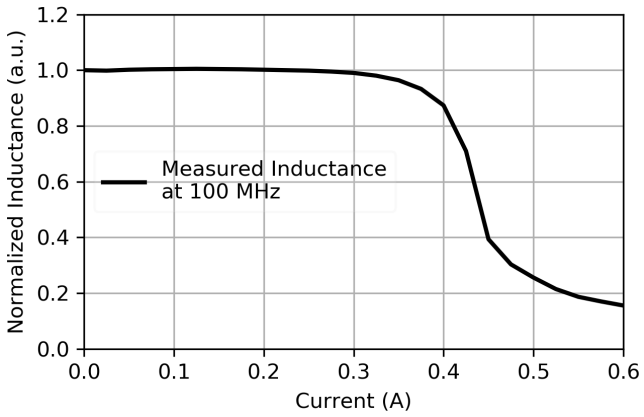


Fig. 6. The inductance at different DC bias conditions showing that a single inductor can sustain 0.4 A without reaching the magnetic saturation.

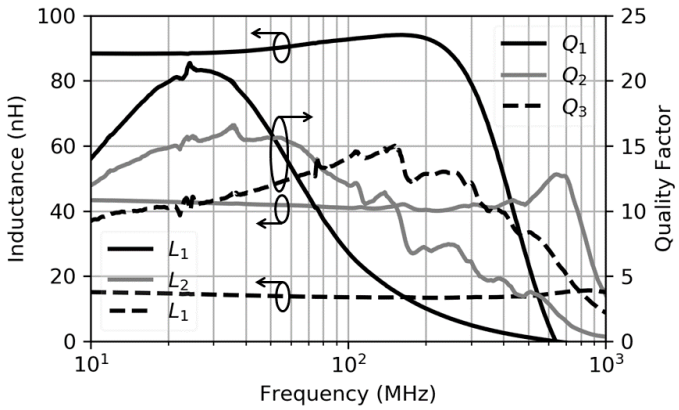


Fig. 5. The frequency response of inductors with different inductance values catered towards application needs.

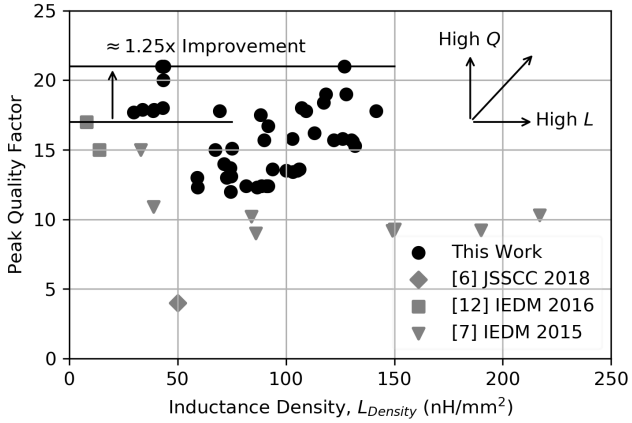


Fig. 7. The measured peak quality factor at different inductance densities. The inductors show a 1.25× improvement in quality factor compared to the leading technologies.

the S-parameter converted to Y-parameters ($Y11$, $Y12$, $Y21$, and $Y22$) for parameter extraction. At a specific frequency, the inductance, AC resistance, and quality factor were extracted as $Im(-1/Y21)/2\pi f$, $Re(-1/Y21)$, and $Im(-1/Y21)/Re(-1/Y21)$, respectively.

The impact of good lamination oxide is experimentally studied by comparing inductor parameters with respect to the lamination oxide quality, as shown in Fig. 4. A relatively flat inductance response was observed with the good quality lamination oxide, indicating the reduction of eddy current loss. In addition, a thick metal process was employed in the inductor fabrication process. Due to the thick metal, the quality factor in the low frequency range is almost doubled. And the good quality lamination oxide in the magnetic core helped to improve the quality factor at the high frequency range. The measurement results indicate that the overall peak quality factor Q improves by 2.2-times with the improved process conditions. Fig. 5 shows the performance of the inductors catered towards the requirements of different switching frequencies. The peak-Q ranges from 21 to 15 while operating from 25-150 MHz frequencies. The inductor saturation effect was characterized, and as seen from Fig. 6, a typical inductor can carry up to 0.4 A without reaching the magnetic core saturation behavior.

In a traditional power converters, the switching frequency is often low and a large value ($> \mu$H) inductance is used for the filtering purpose. At low frequencies, the eddy current, skin and proximity effect are not dominant, thus the AC resistance (R_{AC}) remains same as the R_{DC}. The designer has to worry about DC resistive loss and magnetic core loss. However, at higher frequency the R_{AC} become dominant, and this incurs a significant loss in the inductor. Hence, for high-efficiency and high-frequency power conversion, a high-Q inductor technology is desirable, and the figure of merit of the AC performance can be defined by the product of Q and L.

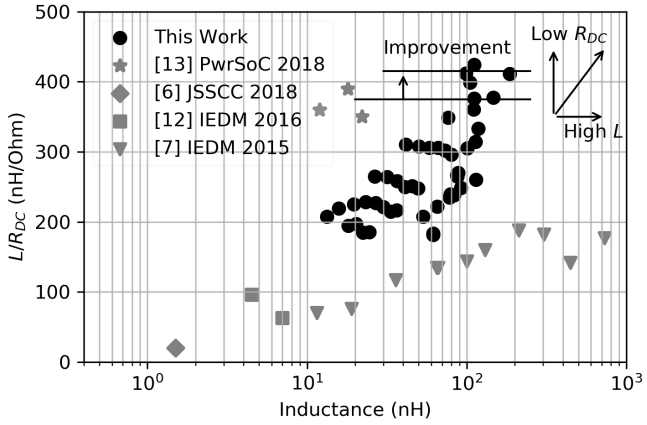


Fig. 8. The inductance to DC resistance ratio (L/R_{DC}) of different magnetic inductors.

The inductance per unit area ($L_{Density}$) should be as large as possible while keeping a high-Q. A comparison showing the peak quality factor at different inductance densities is shown in Fig. 7. According the figure of merit definition, the best results are in the top right corner of the Fig. 7. With the superior magnetic core lamination technique and thick metal processing, the reported inductors show a 1.25× improvement in Q as compared to the leading technologies [6], [7], [12]. The measured Q is as high as 21 at an $L_{Density}$ of 127 nH/mm^2. Another key parameter of the inductor structure contributing to the loss is the R_{DC}. The reported inductors have achieved an excellent L/R_{DC} performance as large as 425 nH/Ohm. The L/R_{DC} values of different inductors are shown in Fig. 8. It is evident that the overall performance has been improved compared to the leading technologies [6], [7], [12], [13] reported in the literature, and these results translate into an inductor switching efficiency more than 95% which is suitable for realizing fully integrated on-chip power conversion.

IV. Conclusion

This paper described a technique to improve the quality factor (Q) of thin-film magnetic inductors. A library of inductors was fabricated, and the proposed hypothesis is experimentally verified. With the improved magnetic core lamination, an area efficient, high-Q and low R_{DC} thin-film magnetic inductor technology is developed that can facilitate a wide range of on-chip power conversion applications, including the Fully Integrated Voltage Regulators (FIVR) and Power Supply On-Chip (PwrSoC).

Acknowledgement

This work was supported by A*STAR Science and Engineering Research Council (SERC) Grant #152 78 00039. We would like to thank Singulus Technologies AG for helping the deposition of high permeability anisotropic multilayer laminated films.

References

[1] C. Ó. Mathúna, N. Wang, S. Kulkarni, and S. Roy, "Review of integrated magnetics for Power Supply on Chip (PwrSoC)," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4799–4816, 2012.

[2] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. N. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 1–14.

[3] D. Hou, F. C. Lee, and Q. Li, "Very high frequency IVR for small portable electronics with high-current multiphase 3-D integrated magnetics," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8705–8717, 2017.

[4] R. Wu and J. K. O. Sin, "A novel silicon-embedded coreless inductor for high-frequency power management applications," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 60–62, 2011.

[5] S. Raju, Xing Li, Yan Lu, Chi-Ying Tsui, Ki Wing-Hung, Mansun Chan, and C. Patrick Yue, "Efficient wireless power transmission technology based on above-CMOS integrated (ACI) high quality inductors," in *2014 IEEE International Electron Devices Meeting*, 2014, pp. 12.4.1–12.4.4.

[6] H. K. Krishnamurthy, V. Vaidya, P. Kumar, R. Jain, S. Weng, S. T. Kim, G. E. Matthew, N. Desai, X. Liu, K. Ravichandran, J. W. Tschanz, and V. De, "A Digitally Controlled Fully Integrated Voltage Regulator with On-Die Solenoid Inductor with Planar Magnetic Core in 14-nm Tri-Gate CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, pp. 8–19, 2018.

[7] N. Sturcken, R. Davies, H. Wu, M. Lekas, K. Shepard, K. W. Cheng, C. C. Chen, Y. S. Su, C. Y. Tsai, K. D. Wu, J. Y. Wu, Y. C. Wang, K. C. Liu, C. C. Hsu, C. L. Chang, W. C. Hua, and A. Kalnitsky, "Magnetic thin-film inductors for monolithic integration with CMOS," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, pp. 11.4.1–11.4.4.

[8] A. A. Muthukumaraswamy, K. J. Chui, W. Y. Lim, J. Yu, S. Soh, L. Y. Wing, H. Lin, and S. Wickramanayaka, "Thin-film magnetic inductor for integrated power management," in *2017 IEEE 67th Electronic Components and Technology Conference (ECTC)*, 2017, pp. 1485–1490.

[9] S. Raju, S. Soh, L. Y. Wing, D. Ho, L. Huamao, M. Stenger-Koob, J. Wrona, M. Landmann, B. Ocker, J. Langer, and R. P. Singh, "Integrated Magnetic Inductor Technology on Silicon," in *2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)*, 2018, pp. 262–265.

[10] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp. 743–752, 1998.

[11] E. Sun, R. P. Singh, and S. Raju, "A physical model for thin-film magnetic inductors," in *2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)*, 2019, pp. 618–621.

[12] N. Wang, B. B. Doris, A. B. Shehata, E. J. O. Sullivan, S. L. Brown, S. Rossnagel, J. Ott, L. Gignac, M. Massouras, L. T. Romankiw, and H. L. Deligianni, "High-Q magnetic inductors for high efficiency on-chip power conversion," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, pp. 35.3.1–35.3.4.

[13] N. Sturcken, "Integrated power management with ferromagnetic thin-film power inductors," in *2018 International Workshop on Power Supply on Chip (PwrSoC)*, 2018.