CS39001 - COMPUTER ORGANIZATION LABORATORY

INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

Verilog Assignment 1 (Question 2)

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Date: August 31, 2022

2. Carry Look-ahead Adder

(a) Design

The Carry Look-ahead Adder (CLA) reduces the reduces the propagation delay of the carry values by introducing more complex hardware.

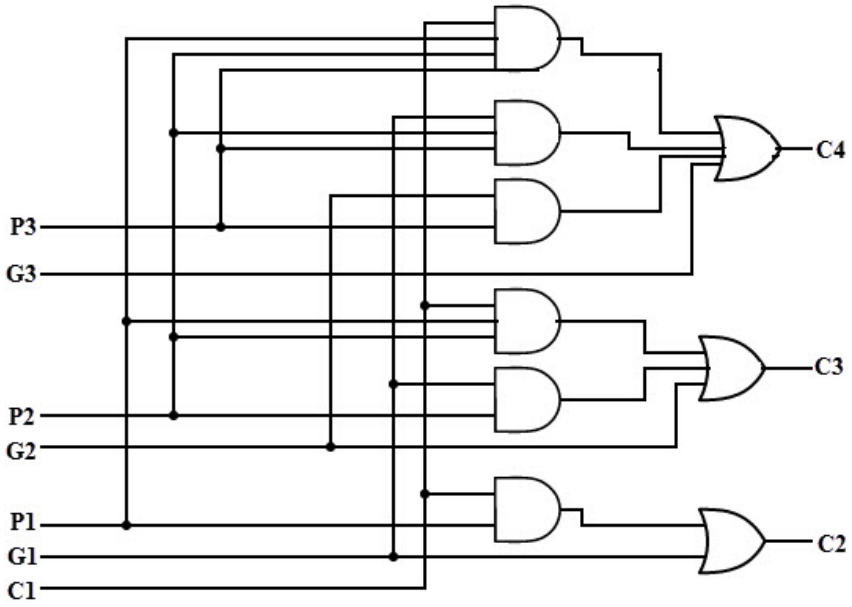

Figure 1: Circuit Diagram of a Carry Look-ahead Adder

We define two variables G[3:0] (carry generate) and P[3:0] (carry propagate)

$$G_i = A_i \cdot B_i \quad \text{for} \quad 0 \leq i \leq 3$$

$$P_i = A_i \oplus B_i \quad \text{for} \quad 0 \leq i \leq 3$$

The output sum S[3:0] and carry output C[3:0] is defined as

$$C_0 = c_{in}$$

$$C_{i+1} = G_i + (P_i \cdot C_i) \quad \text{for} \quad 0 \leq i \leq 2$$

$$S_i = P_i \oplus C_i \quad \text{for} \quad 0 \leq i \leq 3$$

We can expand this to get the simplified equations

$$C_0 = c_{in}$$

$$C_1 = G_0 + (P_0 \cdot C_0)$$

$$\therefore C_1 = G_0 + (P_0 \cdot c_{in})$$

$$C_2 = G_1 + (P_1 \cdot C_1)$$

$$\therefore C_2 = G_1 + (P_1 \cdot G_0) + (P_1 \cdot P_0 \cdot c_{in})$$

$$C_3 = G_2 + (P_2 \cdot C_2)$$

$$\therefore C_3 = G_2 + (P_2 \cdot G_1) + (P_2 \cdot P_1 \cdot G_0) + (P_2 \cdot P_1 \cdot P_0 \cdot c_{in})$$

$$c_{out} = G_3 + (P_3 \cdot C_3)$$

$$\therefore c_{out} = G_3 + (P_3 \cdot G_2) + (P_3 \cdot P_2 \cdot G_1) + (P_3 \cdot P_2 \cdot P_1 \cdot G_0) + (P_3 \cdot P_2 \cdot P_1 \cdot P_0 \cdot c_{in})$$

(b) Correctness and speed of 4-bit CLA.

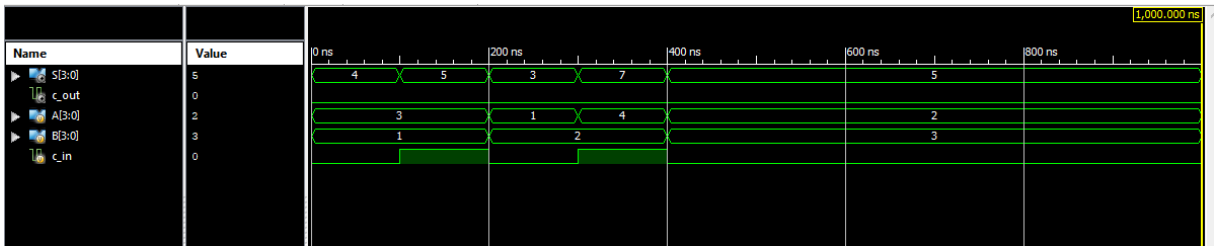

Figure 2: Simulation of 4-bit CLA

Best case achievable time of a 4-bit CLA is **2.432 ns**
Best case achievable time of a 4-bit RCA is **3.090 ns**
Hence we observe that CLA is faster than RCA.

(c) 16-bit adder in hierarchial fashion

(i) Augmented 4-bit adder

Equations:

$$P_{prop} = P_0 \cdot P_1 \cdot P_2 \cdot P_3$$

$$G_{prop} = G_3 + (P_3 \cdot C_3) = G_3 + (P_3 \cdot G_2) + (P_3 \cdot P_2 \cdot G_1) + (P_3 \cdot P_2 \cdot P_1 \cdot G_0)$$

Best case achievable time of augmented 4-bit CLA: **2.498 ns**

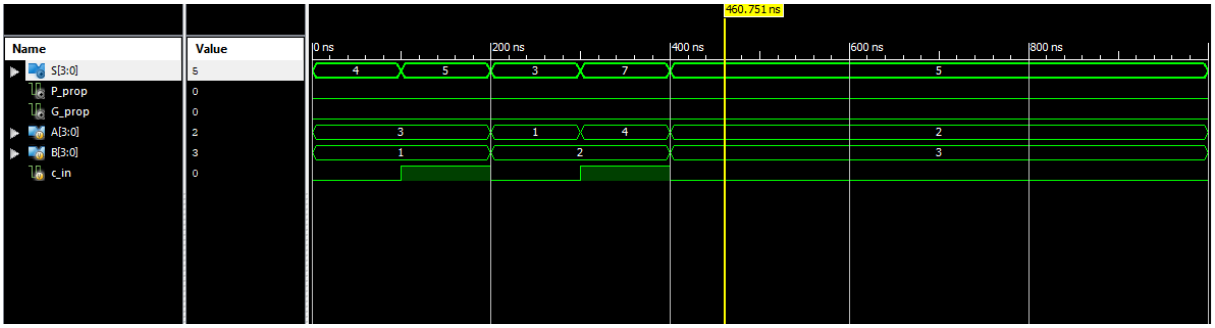

Figure 3: Simulation of augmented 4-bit CLA

(ii) Design of Look-ahead Carry Unit

Equations:

$$P = P_3 \cdot P_2 \cdot P_1 \cdot P_0$$

$$G = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot G_0$$

Best case achievable time of a 16-bit LCU Adder: **3.090 ns**

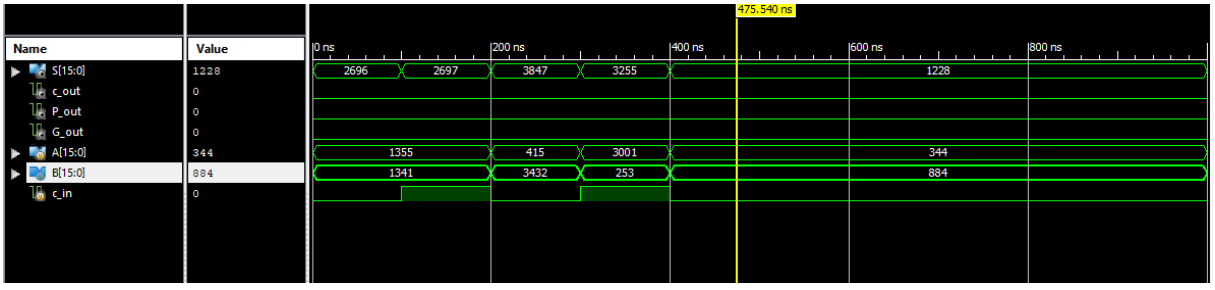

Figure 4: Simulation of 16-bit LCU Adder

(iii) 16-bit Ripple CLA vs 16-bit LCU CLA

Best case achievable time of a 16-bit Ripple CLA: **4.235 ns**, with 28 LUTs used.
Best case achievable time of a 16-bit LCU CLA: **3.090 ns**, with 8 LUTs used.

(iv) Comparison with 16-bit RCA

Best case achievable time of a 16-bit RCA: **9.461 ns** with 28 LUTs used.