CS39001 - Computer Organization Laboratory

Indian Institute of Technology Kharagpur

Department of Computer Science and Engineering

Verilog Assignment 1

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1 Design of a Ripple Carry Adder

A Ripple Carry Adder (RCA) is a circuit that adds two binary numbers. It is made out of a cascading series of Full Adders.
We begin by studying the simplest of adders: Half Adder.

(a) Half Adder Circuit

A Half Adder is a simple circuit which takes in two binary inputs a and b, and calculates their sum with a sum bit s and a carry bit c.

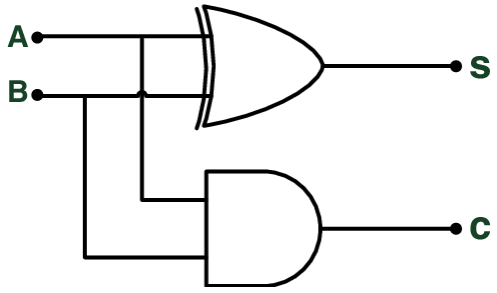

Figure 1: Circuit Diagram of Half Adder

a	b	s	c	Sum
0	0	0	0	00
0	1	1	0	01
1	0	1	0	01
1	1	0	1	10

Table 1: Truth Table of Half Adder

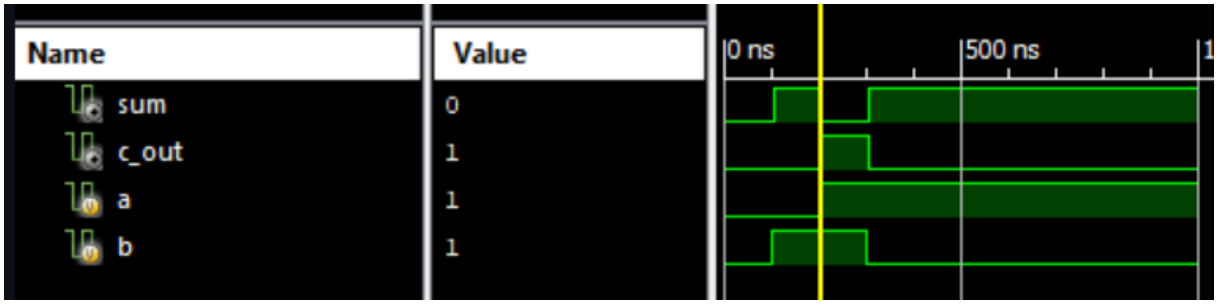

Figure 2: Simulation of Half Adder

(b) Full Adder Circuit

A Full Adder builds upon the design of a Half Adder by also considering a carry-in bit as input. Hence it takes three inputs a, b and c_0, calculates their sum into a sum bit s and carry bit c.

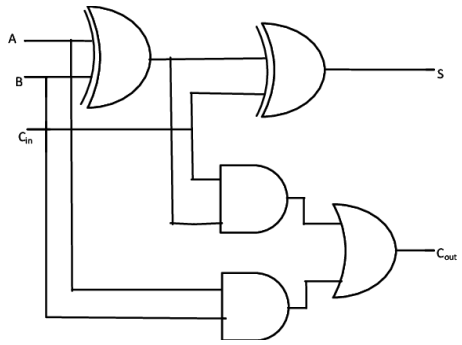

Figure 3: Circuit Diagram of Full Adder

a	b	c_0	s	c	Sum
0	0	0	0	0	00
0	0	1	1	0	01
0	1	0	1	0	01
0	1	1	0	1	10
1	0	0	1	0	01
1	0	1	0	1	10
1	1	0	0	1	10
1	1	1	1	1	11

Table 2: Truth Table of Full Adder

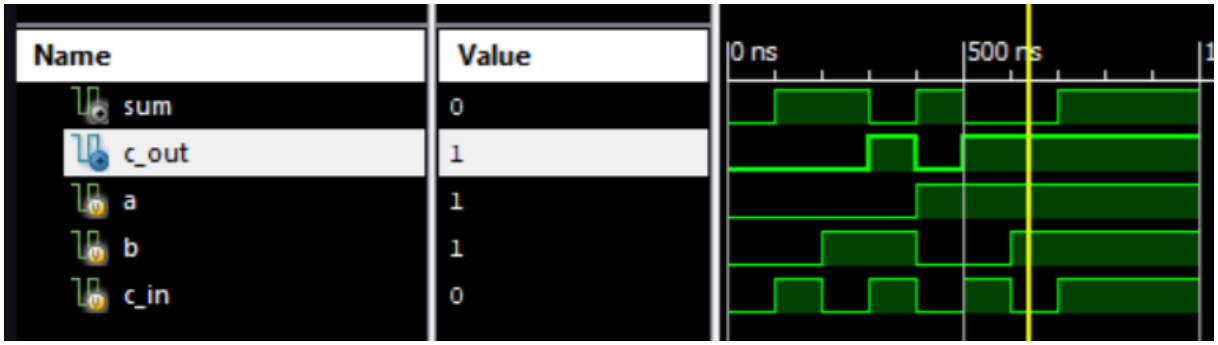

Figure 4: Simulation of Full Adder

(c) Ripple Carry Adder using Full Adders

Ripple Carry Adders can add N-bit binary numbers using a series of N Full Adders. The carry bit of each adder cascades (or ripples) to the next adder.

(i) 8-bit RCA

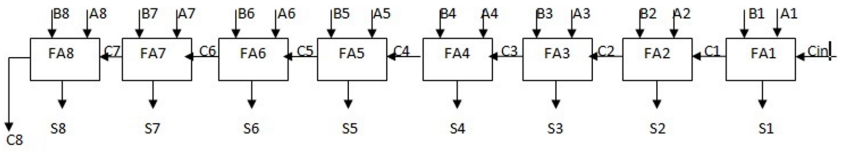

Figure 5: Circuit Diagram

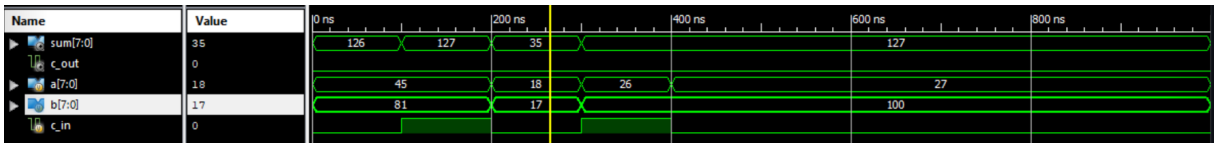

Figure 6: Simulation of 8-bit RCA

Maximum combinational path delay: **3.471 ns**

(ii) 16-bit RCA

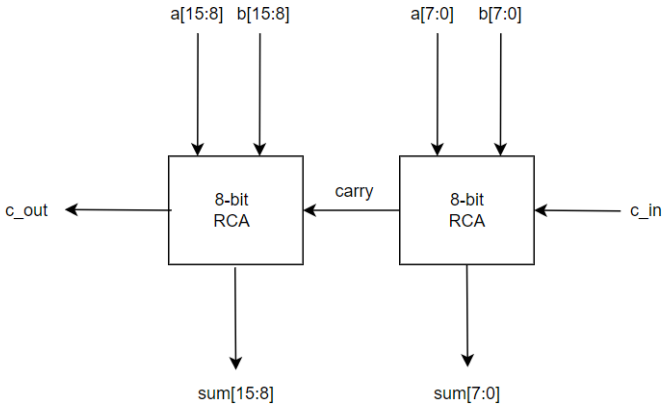

Figure 7: Circuit Diagram

Maximum combinational path delay: **6.167 ns**

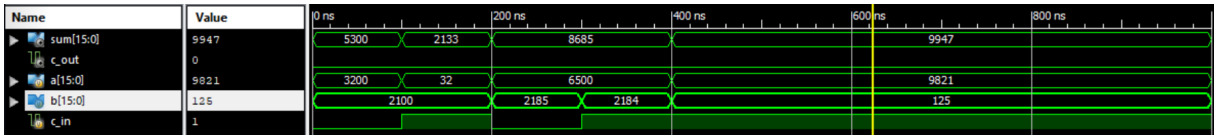

Figure 8: Simulation of 16-bit RCA

(iii) 32-bit RCA

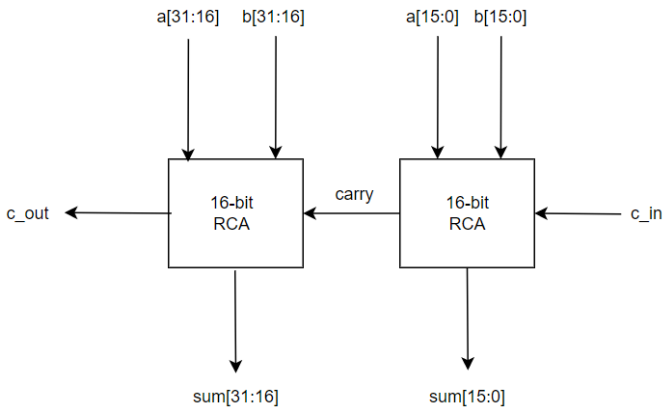

Figure 9: Circuit Diagram

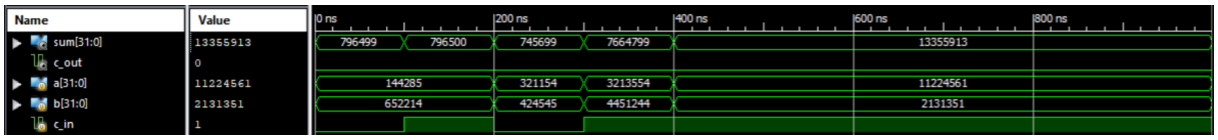

Figure 10: Simulation of 32-bit RCA

Maximum combinational path delay: **11.559 ns**

(iv) 64-bit RCA

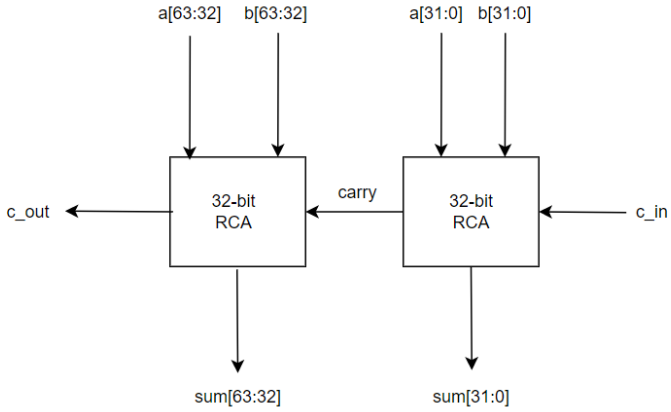

Figure 11: Circuit Diagram

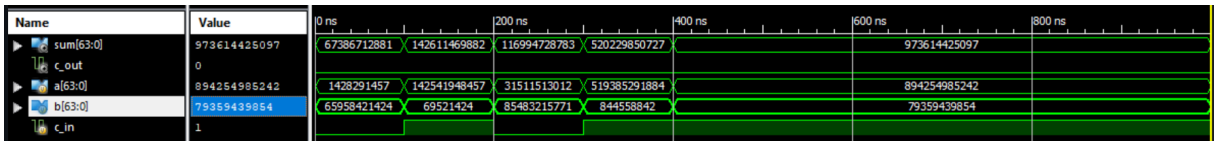

Figure 12: Simulation of 64-bit RCA

Maximum combinational path delay: **22.343 ns**

(d) Subtraction using RCA

To calculate $a - b$, the idea is to add the 2's complement of b to a with an RCA. To get 2's complement of b, we first flip the bits of b to get $\overline{b}$. Next we set c_{in} of the adder to 1. This will transform b to $\overline{b} + 1$ which is the 2's complement of b. Finally we feed a, $\overline{b}$, and 1 (as c_{in}) to the RCA. This will yield the desired result.