Miracle QL MIDI interface V3 A13 --- nc A12 --- nc A11 --- nc =1 Select 6264 Ram A10 --- nc =1 Select 6850 UART 6264 Z80 =0 WAIT on QL Vdd A8 - nc (swap with A0 to use with ZA11 A10 40 ZA10 Gold card & modified S/W) ZA12 - A12 WR 27 WR 7A12 - A12 A9 39 ZA9 ZA15 ZA14 ZA13 Z80 Address map: ZA7 -3 CS ZA15 ZA13 - A13 - ZA8 .374 WAIT on QL (Read/Write) ZA6 -4 A6 A8 ²⁵—ZA8 ZA14 - A14 A7 37 ZA7 ZA7 Read status on D7 \$00xx Read/Write data to QL ZA5 -5 A5 ²⁴—ZA9 ZA15 -5 A15 A6 36 ZA6 D6 ZA6 A9 invalid (WAIT & 6850) Q5 \$2000 Read status on D7 A11 23 ZA11 CLK - CLK A5 35 ZA5 ZA5 Read/Write 6850 UART 6850 control register write \$6000 ZA3 -7 A3 ŌĒ 22 RD A4 34 ZA4 ZD4 -7 invalid (WAIT & 6264) 6850 data register write \$6001 ZA3 ZA2 -8 A10 21 ZA10 ZD3 -8 D3 A3 33 ZA3 A2 0 Read/Write 6264 Ram \$6002 6850 status register read 0V -7A2 ZA1 — A1 CS ZD5 -9 D5 A2 32 ZA2 invalid (WAIT & 6850+6264!) \$6003 6850 data register read ZA0 -10 ¹⁹ ZD7 ZD6 -10 D1 ZA1 – ZA1 ΑO QL ROM port invalid (6850+6264!) \$A000 to \$BFFF 6264 8K ram _¹¹ D0 +5V -11 Vdd ZA0 ZD0 D6 18 ZD6 30 ZA0 Α0 OF CLK ZD1 -12 D1 D5 17—ZD5 ZD2 -12 D2 Vss 29 0V ZD7 -13 D7 CLK ZD2 -13 D2 D4 ZD4 RFSH 10M 14 Vss M₁ D3 +5V 5—ZD3 ZD0 -14 nc 74#2 ZD1 -15 RESET RESET D1 374 R4 > 16 INT ZD7 +5V **BUSRQ** X1 8MHz D O -+5V +5V -17 WAIT ZD6 WAIT $\overline{0}$ D5 Ω5 ZD5 nc ______18 HALT ²³— nc **BUSAK** Q4 MREQ $\overline{\mathsf{WR}}$ 22 WR ZD4 nc C3 nc 20 IORO **^**Q3 $\overline{\mathsf{RD}}$ 21 RD +5V +5V 33pF D2 ZD2 Q2 ZD1 Q1 0V Q0 ZD0 CLK TIL-111 171 (see A8) ≥R10 2K2 Vss 6850 CTS 24 OV RESET +5V 74#1 DCD 23 0V RxD D0 22 ZD0 12 D O 2 D O RxClk A15 ²¹—ZD1 TxClk D1 RTS D2 20 ZD2 D1 ROMOEH R11 180 R5 180 D3 19 ZD3 ZD7 TxD D4 -8 ZD4 R2 10K +5V -CS₀ D5 17 ZD5 ZA13 0V - ° CS2 D6 -ZD6 R7 15 ZD7 ZA14 -10 CS1 D7 3**O O**1 30 O¹ 3**O** O1 4K7 ZA0 D2 low: nothing C1 33uF C2 33uF +5V Vdd R/W 13—ZA1 RESET - WAIT $\overline{\mathsf{RD}}$ IN **THRU** OUT 10 $\overline{\mathsf{WR}}$ +5V