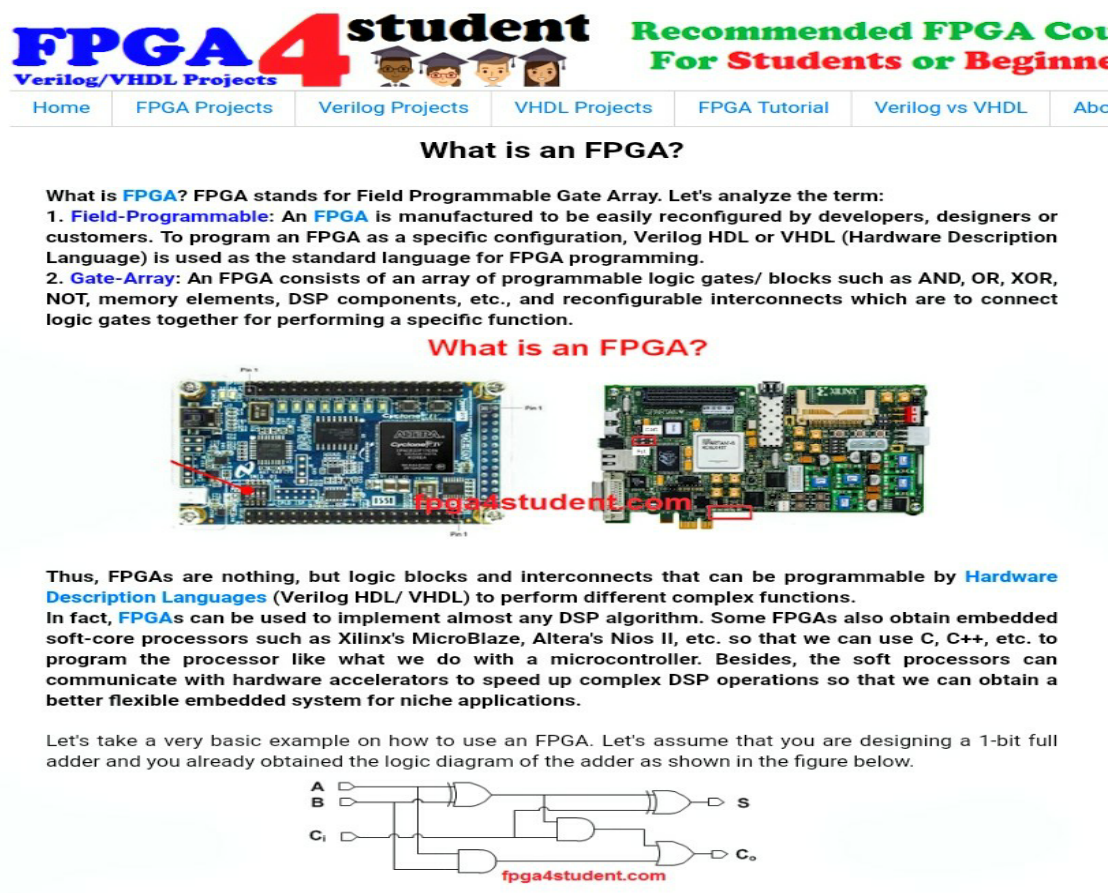
DAILY ASSESSMENT FORMAT

Date:	05-06-2020	Name:	Abhishek
Course:	DIGITAL DESIGN USING HDL	USN:	4al17ec001
Topic:	1]Verilog Tutorials and practice programs 2]Building/ Demo projects using FPGA 3]Task	Semester & Section:	6 & 'A'
Github Repository:	Abhishek-online-courses		

FORENOON SESSION DETAILS
Image of session



FPGA4student Verilog/VHDL Projects

Recommended FPGA Cou For Students or Beginne

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What is an FPGA?

What is FPGA? FPGA stands for Field Programmable Gate Array. Let's analyze the term:
1. Field-Programmable: An FPGA is manufactured to be easily reconfigured by developers, designers or customers. To program an FPGA as a specific configuration, Verilog HDL or VHDL (Hardware Description Language) is used as the standard language for FPGA programming.
2. Gate-Array: An FPGA consists of an array of programmable logic gates/ blocks such as AND, OR, XOR, NOT, memory elements, DSP components, etc., and reconfigurable interconnects which are to connect logic gates together for performing a specific function.

What is an FPGA?

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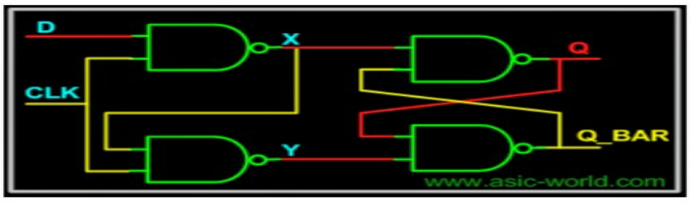
Thus, FPGAs are nothing, but logic blocks and interconnects that can be programmable by Hardware Description Languages (Verilog HDL/ VHDL) to perform different complex functions.
In fact, FPGAs can be used to implement almost any DSP algorithm. Some FPGAs also obtain embedded soft-core processors such as Xilinx's MicroBlaze, Altera's Nios II, etc. so that we can use C, C++, etc. to program the processor like what we do with a microcontroller. Besides, the soft processors can communicate with hardware accelerators to speed up complex DSP operations so that we can obtain a better flexible embedded system for niche applications.

Let's take a very basic example on how to use an FPGA. Let's assume that you are designing a 1-bit full adder and you already obtained the logic diagram of the adder as shown in the figure below.

Report –

Verilog Tutorials and practice programs :

D–Flip flop from NAND Gate



Verilog Code

```
module dff_from_nand();
wire Q,Q_BAR;
reg D,CLK;

nand U1 (X,D,CLK) ;
nand U2 (Y,X,CLK) ;
nand U3 (Q,Q_BAR,X);
nand U4 (Q_BAR,Q,Y);

// Testbench of above code
initial begin
   $monitor( "CLK = %b D = %b Q = %b Q_BAR = %b" ,CLK, D, Q, Q_BAR);
   CLK = 0;
   D = 0;
   #3 D = 1;
   #3 D = 0;
   #3 $finish;
end

always #2 CLK = ~CLK;

endmodule
```

Building/ Demo projects using FPGA :

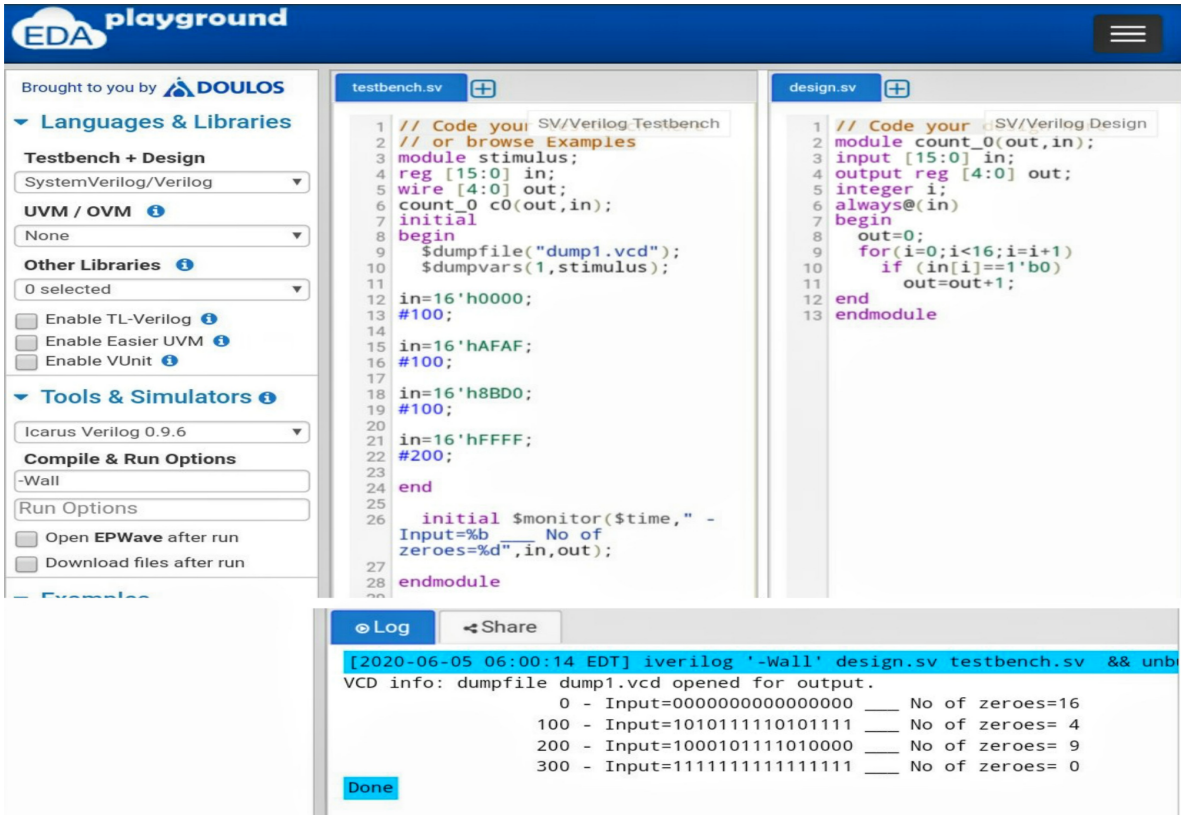
Some of the FPGA projects can be FPGA tutorials such as What is FPGA Programming, image proc on FPGA, matrix multiplication on FPGA Xilinx using Core Generator, Verilog vs VHDL: Expl Examples and how to load text files or images into FPGA. Many others FPGA projects provide st with full Verilog/ VHDL source code to practice and run on FPGA boards. Some of them can be us another bigger FPGA projects.

Following are the FPGA projects on fpga4student.com:

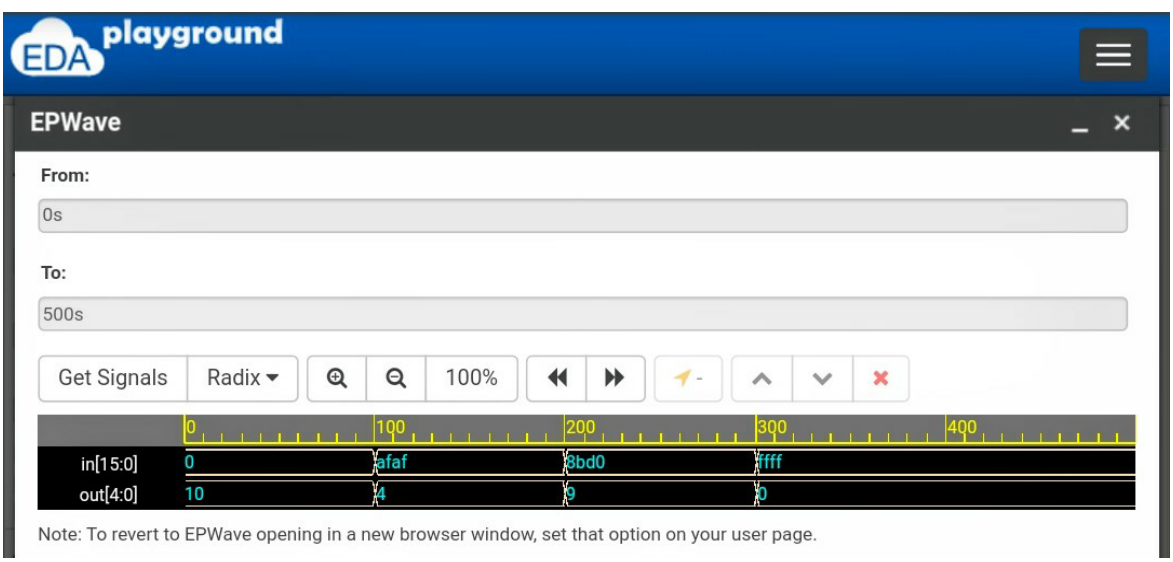
1. What is an FPGA? How does FPGA work?
2. Basys 3 FPGA OV7670 Camera
3. How to load text file or image into FPGA
4. Image processing on FPGA using Verilog
5. License Plate Recognition on FPGA
6. Alarm Clock on FPGA using Verilog
7. Digital Clock on FPGA using VHDL
8. Simple Verilog code for debouncing buttons on FPGA
9. Traffic Light Controller on FPGA
10. Car Parking System on FPGA in Verilog
11. VHDL code for comparator on FPGA
12. Verilog code for Multiplier on FPGA
13. N-bit Ring Counter in VHDL on FPGA
14. Verilog implementation of Microcontroller on FPGA
15. Verilog Carry Look Ahead Multiplier on FPGA
16. VHDL Matrix Multiplication on FPGA Xilinx
17. Fixed Point Matrix Multiplication on FPGA using Verilog
18. Verilog Divider on FPGA
19. VHDL code for Microcontroller on FPGA
20. VHDL code for FIR Filter on FPGA
21. Verilog code for Digital logic components on FPGA
22. Delay Timer Implementation on FPGA using Verilog
23. Single-Cycle MIPS processor on FPGA using Verilog
24. FIFO Verilog Implementation on FPGA
25. FIFO VHDL Implementation on FPGA
26. Verilog D Flip Flop on FPGA
27. Comparator Design on FPGA using Verilog
28. D Flip Flop on FPGA using VHDL
29. Full Adder Design on FPGA using Verilog
30. Full Adder Design on FPGA using VHDL

Task : Implement a verilog module to count number of 0's in a 16 bit number in compiler.

- **Verilog code :**



- **Output :**

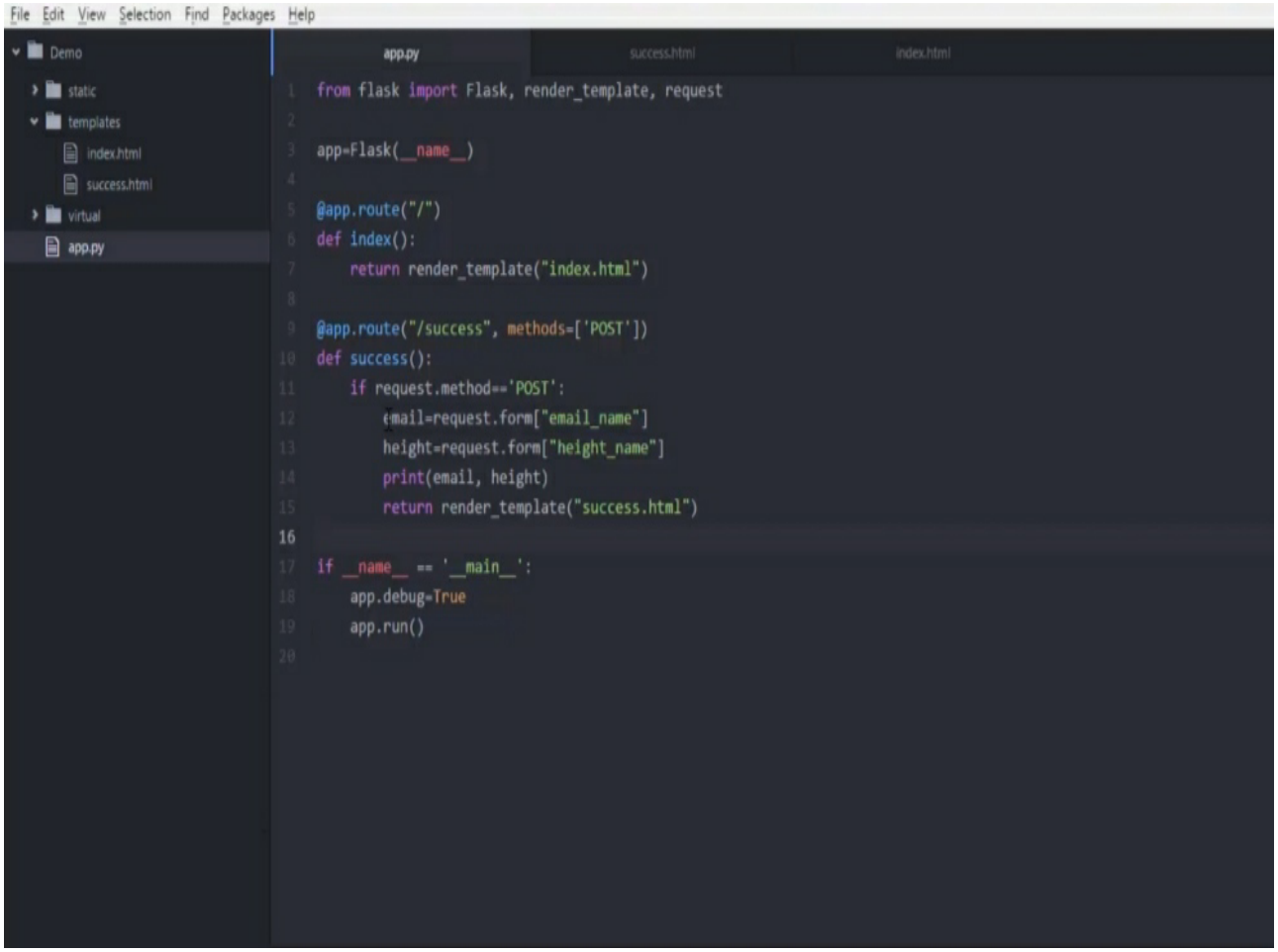


Note : The values displayed in EPWave output are in hexadecimal base.

Date:	05-06-2020	Name:	Abhishek
Course:	The Python Mega Course: Build 10 Real World Applications	USN:	4al17ec001
Topic:	Application 10: Build a Data Collector Web App with PostGreSQL and Flask	Semester & Section:	6 & 'A'

AFTERNOON SESSION DETAILS

Image of session



Report –

Application 9: Build a Data Collector Web App with PostGreSQL and Flask

- **SQLAlchemy** is the Python SQL toolkit and Object Relational Mapper that gives application developers the full power and flexibility of SQL.
- **email.mime** module can create a new object structure by creating Message instances, adding attachments and all the appropriate headers manually.
- The **smtplib** module defines an SMTP client session object that can be used to send mail to any Internet machine with an SMTP or ESMTP listener daemon.
- **Extended HELO (EHLO)** is an Extended Simple Mail Transfer Protocol (ESMTP) command sent by an email server to identify itself when connecting to another email server to start the process of sending an email.
- **Starttls ()** is mainly used as a protocol extension for communication by e-mail, based on the protocol's SMTP, IMAP and POP.