

DAILY ASSESSMENT FORMAT

Date:	01-06-2020	Name:	Abhishek
Course:	DIGITAL DESIGN USING HDL	USN:	4al17ec001
Topic:	1] Industry Applications of FPGA 2] FPGA Business Fundamentals 3] FPGA vs ASIC Design Flow 4] FPGA Basics – A Look Under the Hood	Semester & Section:	6 & 'A'
Github Repository:	Abhishek-online-courses		

FORENOON SESSION DETAILS	
Image of session	

Report – Report can be typed or hand written for up to two pages

Industry Applications of FPGA :

- A field-programmable gate array is an integrated circuit designed to be configured by a customer or a designer after manufacturing.
- **Application :**
 - ✓ Automotive
 - ✓ Broadcast
 - ✓ Consumer
 - ✓ Embedded Vision
 - ✓ Medical
 - ✓ Military / Aerospace / Government
 - ✓ Wireless & Wireline

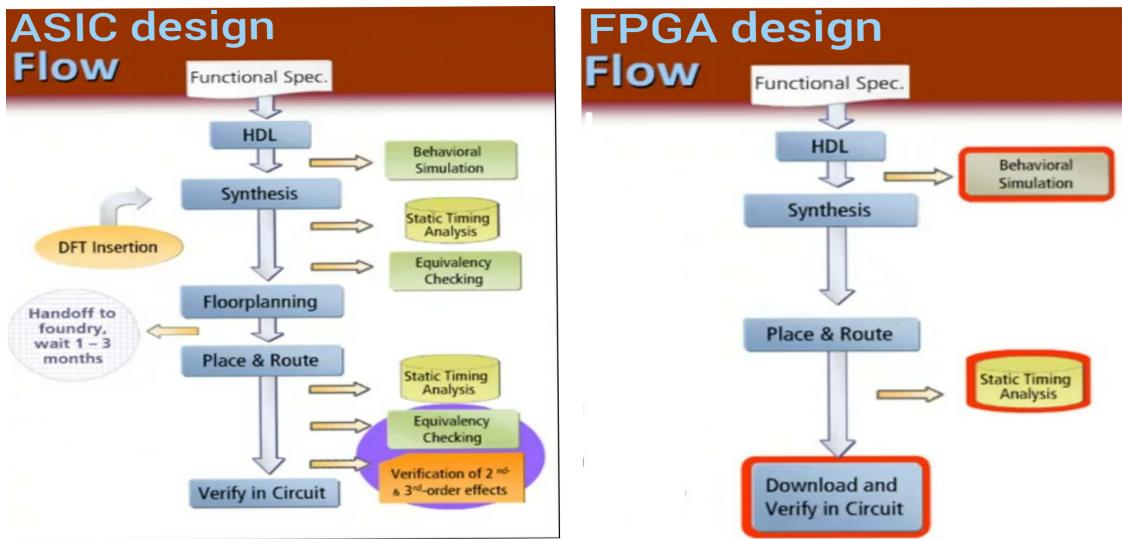
FPGA Business Fundamentals :

- FPGA is usually compared with ASIC & ASSP.
- The main difference between them is FPGA is reprogrammable and others are one time programmable device.

Why FPGA?

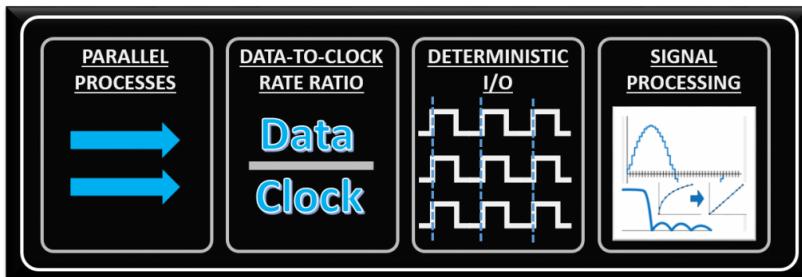


FPGA vs ASIC Design Flow :

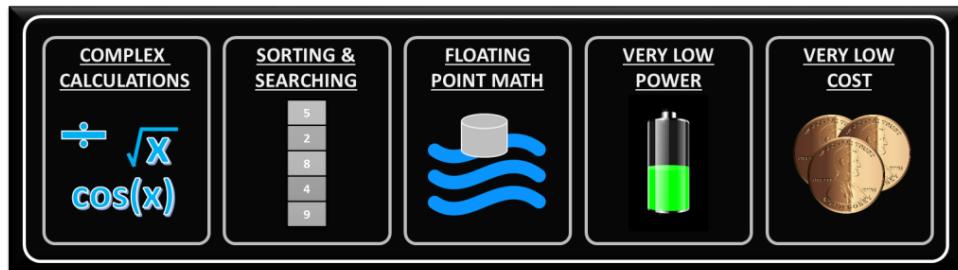


FPGA Basics – A Look Under the Hood :

- FPGA Strengths / best suited for ,



- FPGA Weaknesses / not optimal for ,



Core components in FPGA :

- **LUT (Look-Up Table)** – The obvious use of a LUT is as a logic lookup table generally with 4 to 6 inputs and 1 to 2 outputs to specify any logical operation that fits within those bounds. The two common uses of a LUT are,
 - ✓ *LUT as a shift register* – shift registers are very useful for things like delaying the timing of an operation to align the outputs of one algorithm with another.
 - ✓ *LUT as a small memory* – we can configure the LUT logic as a VERY small volatile random-access memory block.
- **FF (Flip-flop)** – Flip-flops store the output of a combinational logic calculation. They can be used to register data every clock cycle, latch data, gate off data, or enable signals.
- **Block Memory** – This memory block is generally on the order of thousands of bits of memory, is configurable in width and depth, and multiple blocks of memory can be chained together to create larger memory elements.
- **Multipliers or DSP blocks** – Some architectures have recognized the utility of digital signal processing taking place, and have taken it a step further with dedicated DSP blocks, which can not only multiply, but add and accumulate as well.
- **I/O (Input/Output)** – FPGAs will include I/O blocks that allow for various voltage standards as well as timing delay elements to help align multiple signals with one another.
- **Clocking and routing** –
 - ✓ An external oscillator is fed into clocking resources that can multiply, divide, and provide phase-shifted versions of your clock to various parts of the FPGA.
 - ✓ Routing resources not only route your clock to various parts of the FPGA, but also your data.

Task : Write a verilog code to implement NAND gate in all different styles.

- **Verilog code for NAND gate using gate-level modeling :**

```
module NAND_2_gate_level(output Y, input A, B);
    wire Yd;
    and(Yd, A, B);
    not(Y, Yd);
endmodule
```

- **Verilog code for NAND gate using data-flow modeling :**

```
module NAND_2_data_flow (output Y, input A, B);
    assign Y = ~(A & B);
endmodule
```

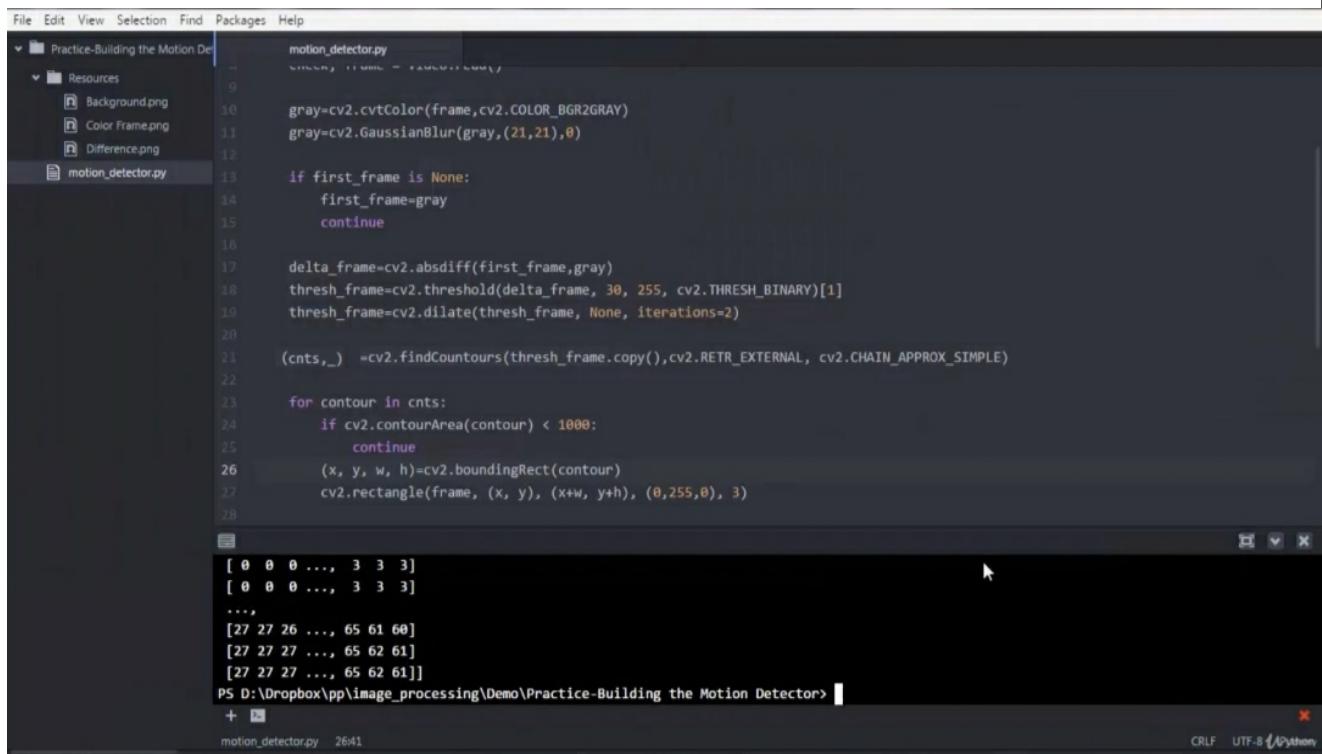
- **Verilog code for NAND gate using behavioral modeling :**

```
module NAND_2_behavioral (output reg Y, input A, B);
    always @ (A or B) begin
        if (A == 1'b1 & B == 1'b1) begin
            Y = 1'b0;
        end
        else
            Y = 1'b1;
    end
endmodule
```

Date:	01-06-2020	Name:	Abhishek
Course:	The Python Mega Course: Build 10 Real World Applications	USN:	4al17ec001
Topic:	1] Application 6: Build a Webcam MotionDetector	Semester & Section:	6 & 'A'

AFTERNOON SESSION DETAILS

Image of session



The screenshot shows a terminal window with the following content:

```

File Edit View Selection Find Packages Help
v Practice-Building the Motion De motion_detector.py
v Resources
  Background.png
  Color Frame.png
  Difference.png
  motion_detector.py
gray=cv2.cvtColor(frame,cv2.COLOR_BGR2GRAY)
gray=cv2.GaussianBlur(gray,(21,21),0)

if first_frame is None:
    first_frame=gray
    continue

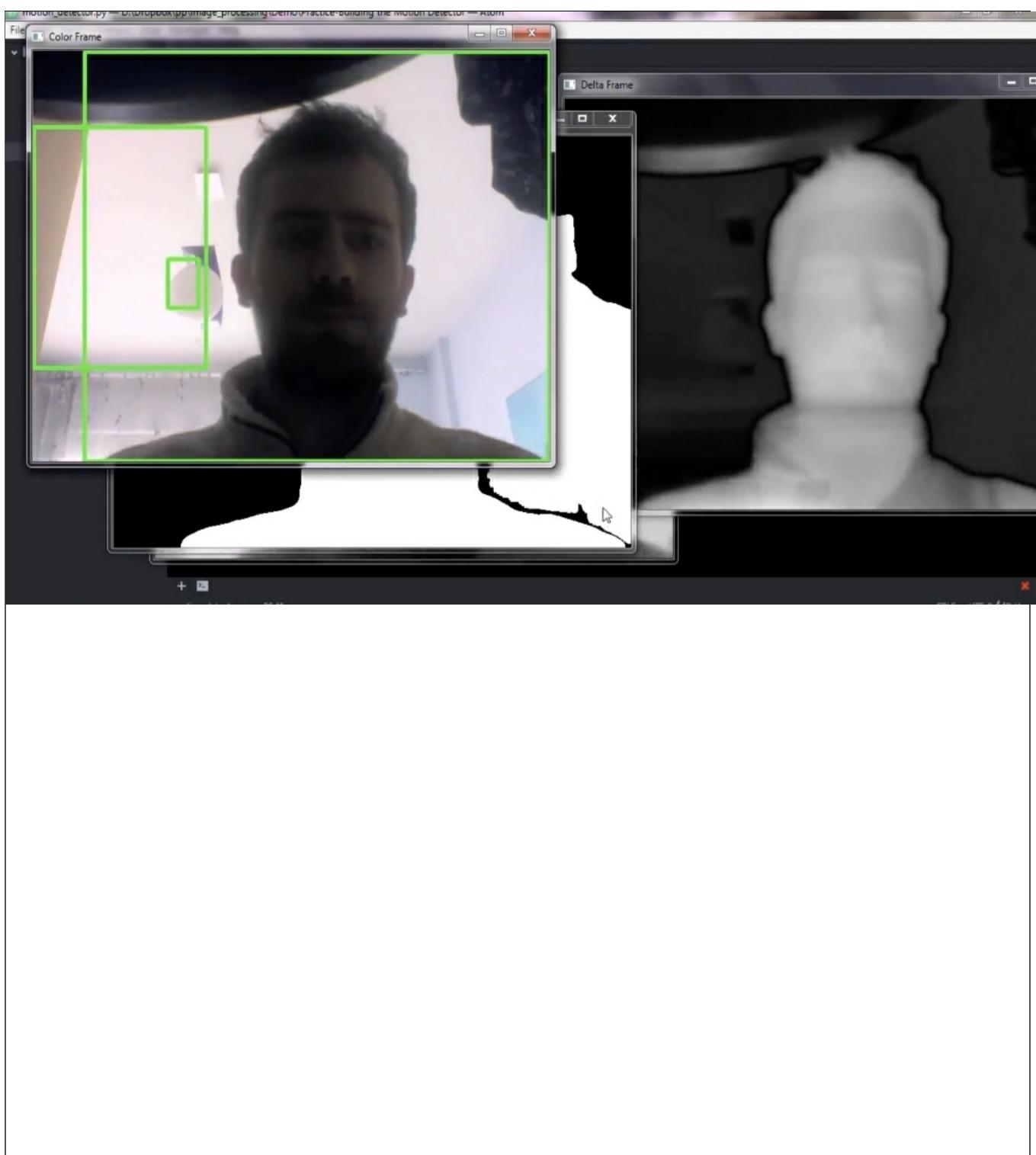
delta_frame=cv2.absdiff(first_frame,gray)
thresh_frame=cv2.threshold(delta_frame, 30, 255, cv2.THRESH_BINARY)[1]
thresh_frame=cv2.dilate(thresh_frame, None, iterations=2)

(cnts,_) =cv2.findContours(thresh_frame.copy(),cv2.RETR_EXTERNAL, cv2.CHAIN_APPROX_SIMPLE)

for contour in cnts:
    if cv2.contourArea(contour) < 1000:
        continue
    (x, y, w, h)=cv2.boundingRect(contour)
    cv2.rectangle(frame, (x, y), (x+w, y+h), (0,255,0), 3)

[ 0  0  0 ...,  3  3  3]
[ 0  0  0 ...,  3  3  3]
...
[27 27 26 ..., 65 61 60]
[27 27 27 ..., 65 62 61]
[27 27 27 ..., 65 62 61]]
```

PS D:\Dropbox\pp\image_processing\Demo\Practice-Building the Motion Detector>



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Application 6: Build a Webcam Motion Detector

- Build a webcam motion detector using **OpenCV** (cv2 module) library for video capturing, datetime module for noting down the time and pandas library for storing data in a csv file.
- OpenCV provides **cv2.GaussianBlur ()** function to apply Gaussian Smoothing on the input source image.
- The function **cv2.absdiff ()** calculates the per-element absolute difference between two arrays or between an array and a scalar.
- The **cv2.dilate ()** function dilates an image by using a specific structuring element.
- The **cv2.boundingRect ()** function of OpenCV is used to draw an approximate rectangle around the binary image.
- Pandas **pandas.DataFrame ()** function is a two-dimensional size-mutable, potentially heterogeneous tabular data structure with labeled axes (rows and columns).
- Pandas DataFrame consists of three principal components, the data, rows, and columns.
- To write DataFrame to a csv file **pandas.to_csv ()** function is used.