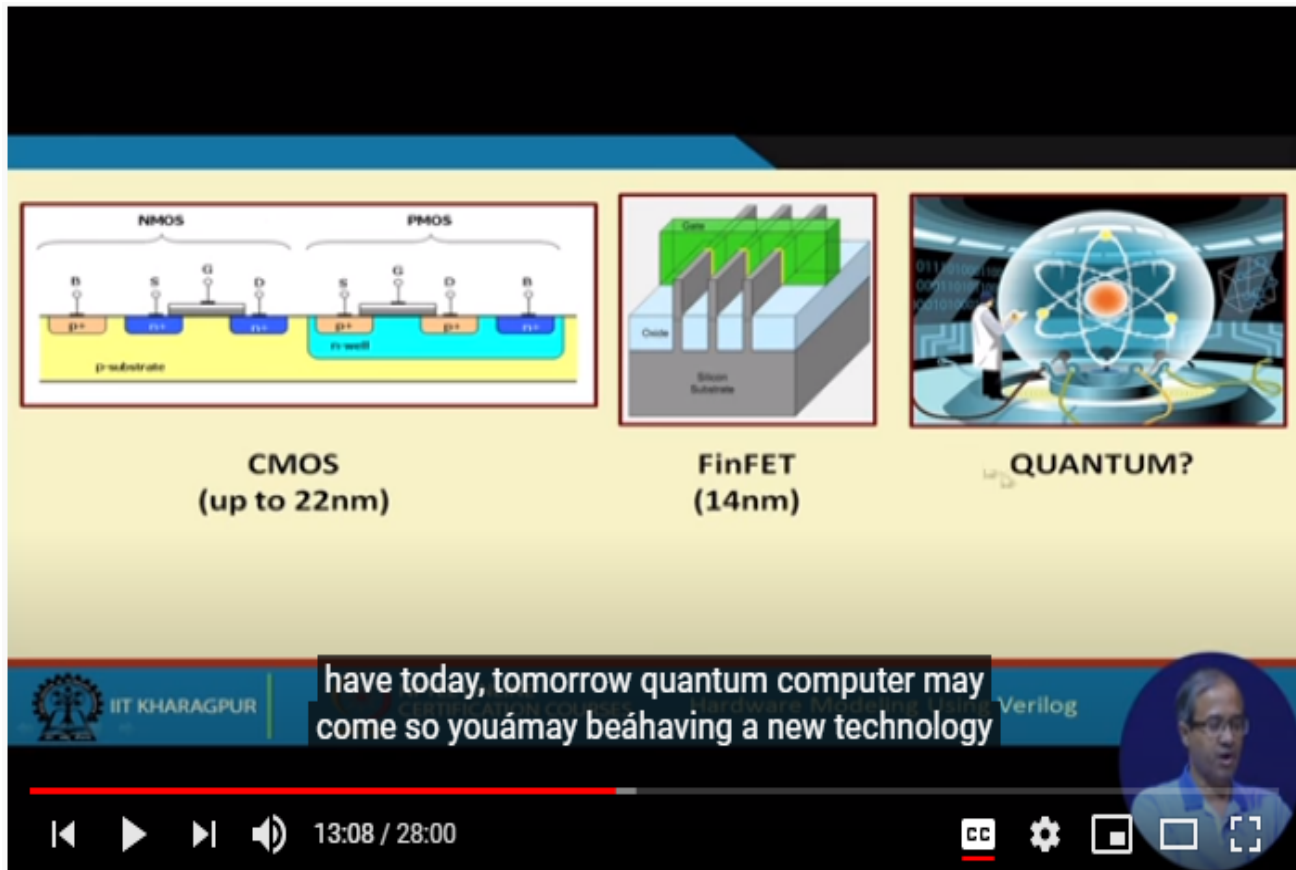


# DAILY ASSESSMENT FORMAT

Date:	4/06/2020	Name:	Akshatha M Deshpande
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC006
Topic:	Hardware modelling using verilog,FPGA and ASIC Interview questions	Semester & Section:	6th Sem A sec
Github Repository:	AkshathaDeshpande		

## FORENOON SESSION DETAILS

Image of session



**Report – Report can be typed or hand written for up to two pages.**

### **VLSI DESIGN FLOW:**

1. Standardized design Procedure.
2. Starting from the design idea down to the actual implementation.
3. Encompasses many steps:
  - ◆ Specification
  - ◆ Synthesis
  - ◆ Simulation
  - ◆ Layout
  - ◆ Test ability Analysis

### **VLSI DESIGN PROCESS:**

1. Design Complexity increasing rapidly:
  - ◆ Increased size and complexity
  - ◆ Fabrication Technology improving
  - ◆ CAD tools are essential
  - ◆ Conflicting requirements like area, speed and energy consumption.
2. The present trend:
  - ◆ Standardize the design flow
  - ◆ Emphasis on low power design, and increased performance.

**Implement a simple T Flipflop and test the module using a compiler:**

```
module tff ( input clk,
input rstn,
input t,
output reg q);
always @ (posedge clk) begin
if (!rstn)
q <= 0;
else
if (t)
q <= ~q;
else
q <= q;
end
endmodule
```

**Test bench:**

```
module tb;
reg clk;
reg rstn;
reg t;
tff u0 ( .clk(clk),
.rstn(rstn),
.t(t),
.q(q));
always #5 clk = ~clk;
initial begin
{rstn, clk, t} <= 0;
```



```

$monitor ("T=%0t rstn=%0b t=%0d q=%0d", $time, rstn, t, q);

repeat(2) @(posedge clk);

rstn <= 1;

for (integer i = 0; i < 20; i = i+1)

begin

reg [4:0] dly = $random;

#(dly) t <= $random;

end

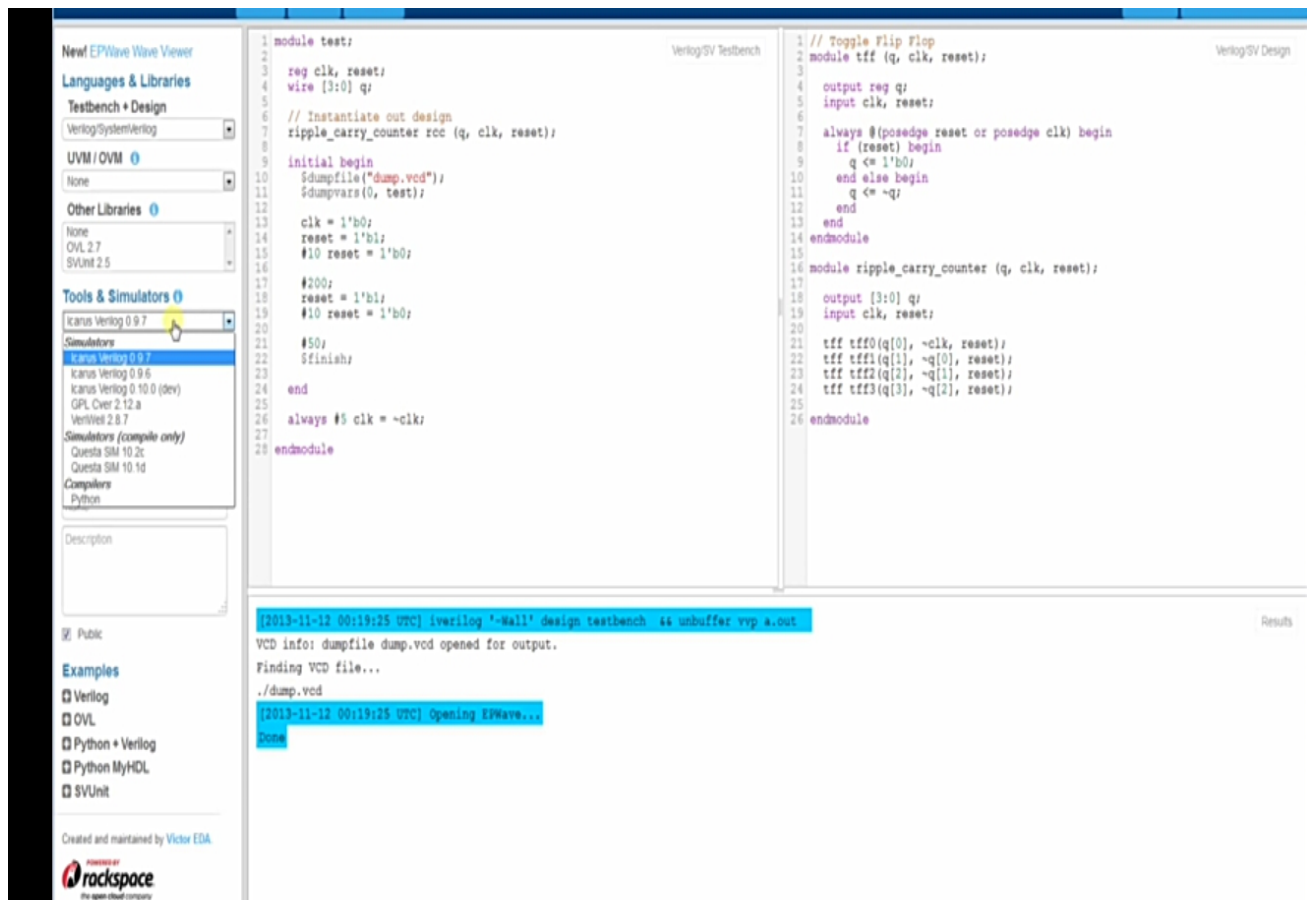
#20 $finish;

end

endmodule

```

Picture:

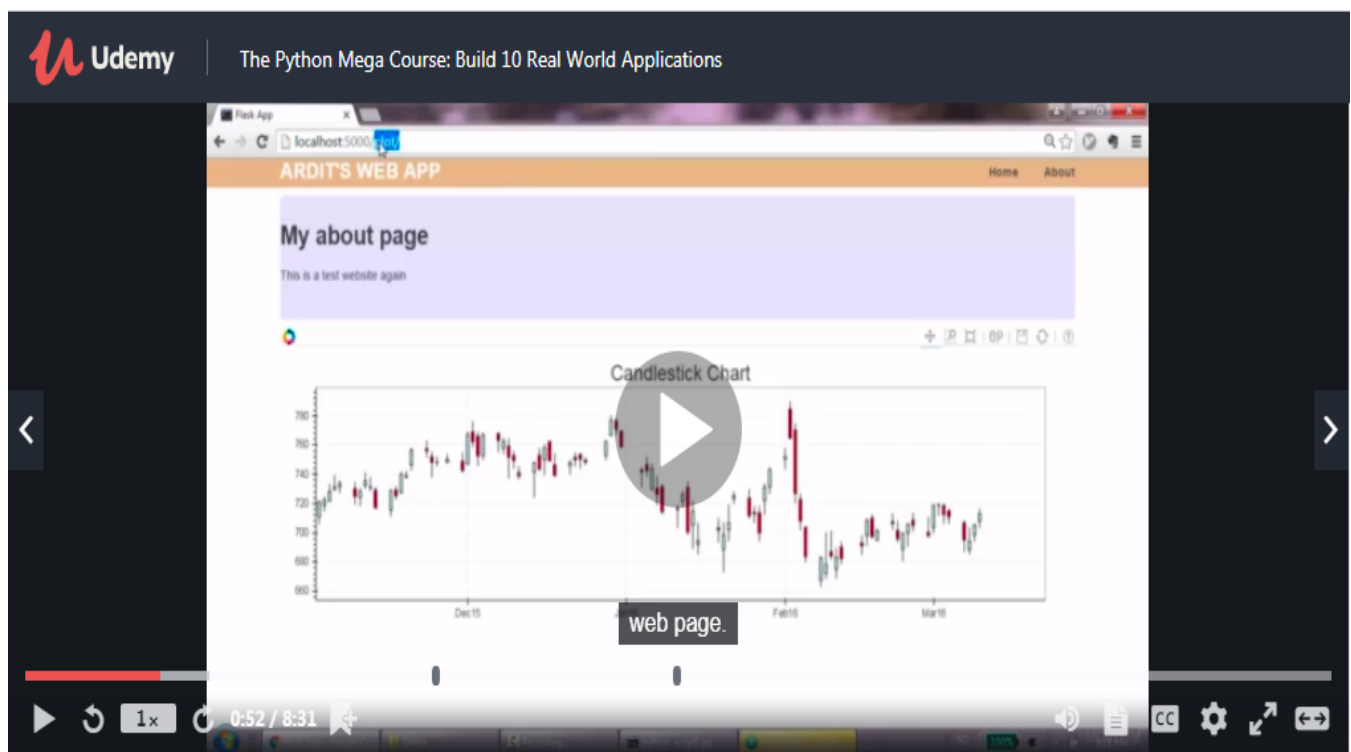


Date: 4/06/2020  
Course: Python  
Topic: Application 9: Build a Web-based Financial Graph

Name: Akshatha M Deshpande  
USN: 4AL17EC006  
Semester & Section: 6th Sem A sec

## AFTERNOON SESSION DETAILS

Image of session




Report – Report can be typed or hand written for up to two pages.

### Application 9: Build a Web-based Financial Graph:

- ◆ Web-based Financial Graph - How The Output Will Look Like
- ◆ Downloading Datasets with Python
- ◆ Stock Market Data
- ◆ Stock Market Data Candlestick Charts
- ◆ Candlestick Charts with Bokeh Quadrants
- ◆ Candlestick Charts with Bokeh Rectangles
- ◆ Candlestick Segments
- ◆ Stylizing the Chart
- ◆ The Concept Behind Embedding Bokeh Charts in a Flask Webpage
- ◆ Embedding the Bokeh Chart in a Webpage
- ◆ Deploying the Chart Website to a Live Server



Date:	4/06/2020	Name:	Akshatha M Deshpande
Course:	Bonus lecture on electrical engineering	USN:	4AL17EC006




# What is Electrical Engineering?

S. Aniruddhan

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Department of Electrical Engineering  
Indian Institute of Technology, Madras  
Chennai, 600036, India

3 June 2020



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What is Electrical Engineering?

