DAILY ASSESSMENT FORMAT

Date:	3/6/2020	Name:	Akshay
Course:	Python	USN:	4AL17EC008
Topic:	Build a Web-based Financial Graph	Semester & Section:	6th-'A'
Github Repository:	Akshay-Online-Course	E-mail:	

FORENOON SESSION DETAILS

Image of session

Betalyzer is a fully function web app that uses some key Python libraries to create a financial technology application in 200 lines of code. Betalyzer makes use of the modern financial data and web stack including pandas, Flask, Quandl, and Jupyter.

Procedure:

1. Save status of the whole board weekly as a CSV file.

2. Read all historical CSV files into a Pandas DataFrame.

3. Sort, filter, group and manipulate the data into agreed formats of how we want to track progress (by the status of activity, workstream, etc.).

4. Write the output to an Excel file with the data from each analysis within its own sheet, formatted in such a way that it can be simply copied and pasted into think-cell charts.
5. Create tables and charts for the reporting package for the monthly steering committee meeting.

6. Scrape data of real estate listings, including address, size, number of rooms, asking price, and other features, for a given area; a few hundred to perhaps a thousand lines in total.

7. Save into a Python data structure.

8. Connect to the Google Maps API and, for each listing, retrieve the distance between the property and key landmarks such as the sea, the city center, nearest train station, nearest airport, etc.

9. Export the data to an Excel file.

10. Use standard Excel functionality to run regressions, calculate statistics and create charts on standard metrics such as price per square meter and distance to landmarks.

All Tickers

Show 10 entries

Search:

Ticker	Name	Last Price	Market Cap ($mm)	IPO Year	Sector	Industry	Beta
AAPL	Apple Inc.	120	630,938	1980.0	Technology	Computer Manufacturing	1.11
GOOG	Alphabet Inc.	805.02	554,851	2004.0	Technology	Computer Software: Programming, Data Processing	1.13
MSFT	Microsoft Corporation	62.74	487,825	1986.0	Technology	Computer Software: Prepackaged Software	1.21
AMZN	Amazon.com, Inc.	808.33	384,091	1997.0	Consumer Services	Catalog/Specialty Distribution	1.18
CSCO	Cisco Systems, Inc.	30.1	151,095	1990.0	Technology	Computer Communications Equipment	1.06
AMGN	Amgen Inc.	154.67	115,062	1983.0	Health Care	Biotechnology: Biological Products (No Diagnostic Substances)	1.22
GILD	Gilead Sciences, Inc.	71.01	93,553	1992.0	Health Care	Biotechnology: Biological Products (No Diagnostic Substances)	1.15
QCOM	QUALCOMM Incorporated	62.88	92,918	1991.0	Technology	Radio And Television Broadcasting And Communications Equipment	0.85
CELG	Celgene Corporation	112.66	87,334	1987.0	Health Care	Major Pharmaceuticals	1.42
SBUX	Starbucks Corporation	57.66	83,918	1992.0	Consumer Services	Restaurants	1.05

Showing 1 to 10 of 255 entries

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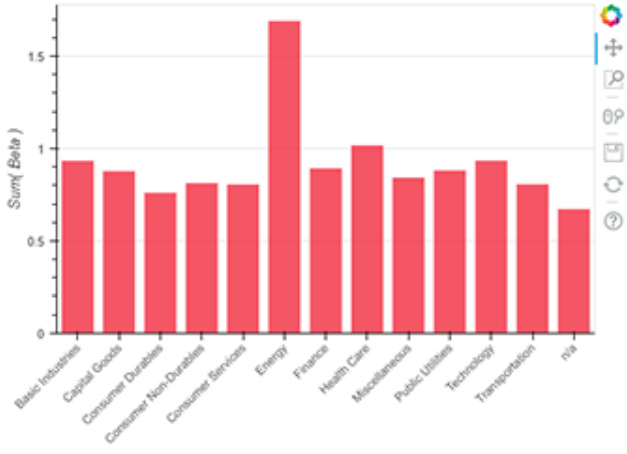
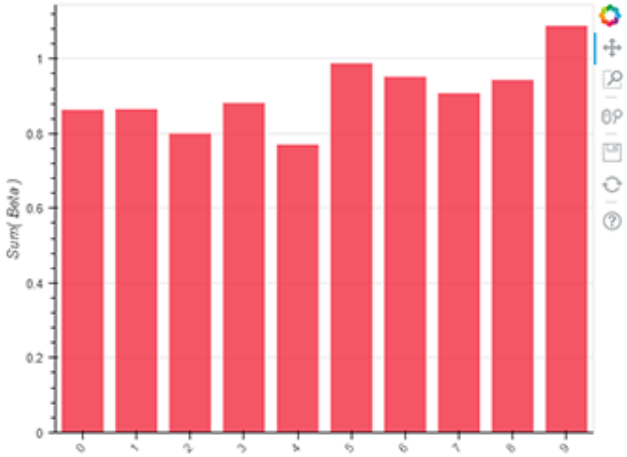
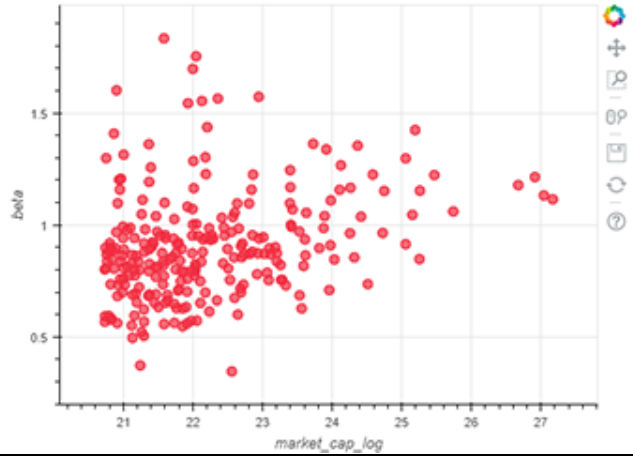
Beta by Sector



Beta by Market Cap Decile



Scatter: Beta v Market Cap (log)

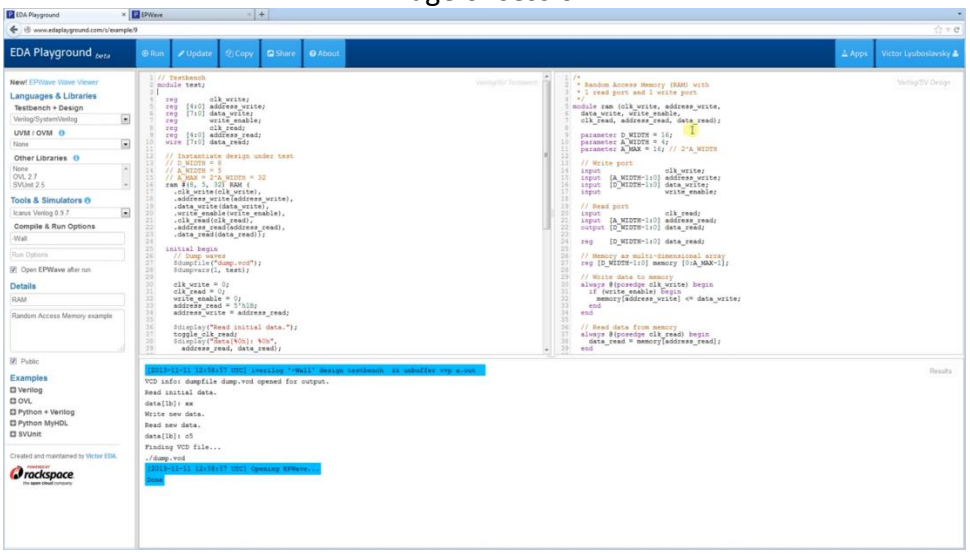


Top Three Stocks Beta Timeseries

Date:	3/6/2020	Name:	Akshay
Course:	Digital Design using HDL	USN:	4AL17EC008
Topic:	1. EDA Playground Online complier 2. EDA Playground Tutorial Demo Video 3. How to Download And Install Xilinx Vivado Design Suite 4. Vivado Design Suite for implementation of HDL code	Semester & Section:	6th-'A'
Github Repository:	Akshay-Online-Course	E-mail:	

AFTERNOON SESSION DETAILS

Image of session



Report – Report can be typed or hand written for up to two pages.

EDA Playground is a web browser-based integrated development environment (IDE) for simulation of System Verilog, Verilog, VHDL, C++/System C and other HDLs. EDA Playground is a free web application that allows users to edit, simulate, share, synthesize, and view waves for hardware description language (HDL) code.

About Xilinx Vivado

Vivado Design Suite is a software suite produced by Xilinx for synthesis and analysis of HDL designs, superseding Xilinx ISE with additional features for system on a chip development and high-level synthesis. Vivado represents a ground-up rewrite and re-thinking of the entire design flow (compared to ISE), and has been described by reviewers as "well-conceived , tightly integrated, blazing fast, scalable, maintainable, and intuitive".

Like the later versions of ISE, Vivado includes the in-built logic simulator ISIM. Vivado also introduces high-level synthesis, with a toolchain that converts C code into programmable logic. Vivado has been described as a "state-of-the-art comprehensive EDA tool with all the latest bells and whistles in terms of data model, integration, algorithms, and performance".

Implement 4 to 1 MUX using structural modelling style and
test the module in an online/offline compiler.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux2_1 is
   port(A,B : in STD_LOGIC;
   S: in STD_LOGIC;
   Z: out STD_LOGIC);
   end mux2_1;
architecture Behavioral of mux2_1 is
begin
process (A,B,S) is
begin
 if (S ='0') then
  Z <= A;
  else
  Z <= B;
 end if;
end process;
end behavioral;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux4_1 is
```

```
port(
A,B,C,D : in STD_LOGIC;
S0,S1: in STD_LOGIC;
Z: out STD_LOGIC
);
end mux4_1;
architecture Behavioral of mux4_1 is
 component mux2_1
  port( A,B : in STD_LOGIC;
  S: in STD_LOGIC;
  Z: out STD_LOGIC);
 end component;
 signal temp1, temp2: std_logic;
 begin
 m1: mux2_1 port map(A,B,S0,temp1);
 m2: mux2_1 port map(C,D,S0,temp2);
 m3: mux2_1 port map(temp1,temp2,S1,Z);
end behavioral;
```