DAILY ASSESSMENT FORMAT

Date:	05/06/2020	Name:	Akshay
Course:	Digital Design Using HDL	USN:	4AL17EC008
Topic:	Verilog Tutorials and Demo projects	Semester	6 [™] & A
	using FPGA	& Section:	
Github	Akshay-Online-Course		
Repository:			

FORENOON SESSION DETAILS



Report:

What is HDL

A hardware description Language Is a language used to describe a digital system, for example, a network switch, a microprocessor or a memory or a simple flip-flop. This just means that, by using a HDL one can describe any hardware (digital) at any level.

One can describe a simple Flip flop as that in above figure as well as one can describe a complicated designs having 1 million gates. Verilog is one of the HDL languages available in theindustry for designing the Hardware. Verilog allows us to design a Digital design at

Behavior Level,

Register Transfer Level (RTL), Gate level and at switch level. Verilog allows hardware designers to express their designs with behavioral constructs, deterring the details of implementation to a later stage of design in the final design.

Design Styles:

- Top Up Design
- Bottom Up Design

Abstract Level of Verilog

• Behavioral Level

This level describes a system by concurrent algorithms (Behavioral). Each algorithm itself is sequential, that means it consists of a set of instructions that are executed one after the other. Functions, Tasks and Always blocks are the main elements. There is no regard to the structural realization of the design.

• Register Transfer Level

Designs using the Register-Transfer Level specify the characteristics of a circuit by operations and the transfer of data between the registers. An explicit clock is used. RTL design contains exact timing possibilities, operations are scheduled to occur at certain times. Modern definition of a RTL code is "Any code that is synthesizable is called RTL code".

Gate Level

Within the logic level the characteristics of a system are described by logical links and their timing properties. All signals are discrete signals. They can only have definite logical values ('0', '1', 'X', 'Z'). The usable operations are predefined logic primitives (AND, OR, NOT etc gates). Using gate level modeling might not be a good idea for any level of logic design. Gate level code is generated by tools like synthesis tools and this netlist is used for gate level simulation and for backen

```
Verilog module to count number of 0's in a 16-bit number. module num_zeros_for( input [15:0] A, output reg [4:0] ones ); integer i; always@(A) begin ones = 0; for(i=0;i<16;i=i+1) if(A[i] == 0'b1) ones = ones + 1; end
```

end module

output

Input = "1010_0010_1011_0010" => Output = "01001" (9 in decimal)

Input = "0011_0110_1000_1011" => Output = "01000" (8 in decimal)

DAILY ASSESSMENT FORMAT

Date:	05/06/2020	Name:	Akshay
Course:	Python	USN	4al16ec008
Topic:	Data analysis with pandas	Semester	6 th A
		& Section:	
Github	Akshay_Online-Course		
Repository:			

AFTERNOON SESSION DETAILS Image of session 101. Making the App password = "ardit700_student", database = "ardit700_pmldatabase" < pes.'), ('line', 'The descendants of one individual.'), ('line', 'A succession of notes forming a distinctive sequence.'), ('line ength equal to one twelfth of an inch.'), ('line', 'An infinitely long, infinitely thin, not bent line in geometry.'), ('line', 'J meardit exercise-project-mysql % python3 exercise.py ('line', 'Term used in GIS technologies in the vector type of internal data organization: spatial data are divided into point, lin es.') ('line', 'The descendants of one individual.') ('line', 'A succession of notes forming a distinctive sequence.') ('line', 'A measure of length equal to one twelfth of an inch.') ('line', 'An infinitely long, infinitely thin, not bent line in geometry.') meandit exercise-project-mysql *

```
Making the app:
import mysql.connector
con=mysql.connector.connect(
user="ardit700_student",
password="ardit700_student",
host=108.167.140.122",
database='ardit700_pm1database".
cursor=con.cursur()
query=cursor.execute("SELECT*FROM dictionary WHERE expression='inlay'")
result=cursor.fetchall()
print(results)
output:
>>python3 exercise.py
[('inlay' 'something filling up a gap or covering up a (small) distance')]
Data analysis with pandas:
   • Pandas is a important python library
   • Pandas is a library that providing data structure and data analysis tools within python
import pandas
df1=pandas.dataframe([[2,4,6],[10,20,30]])
df1
For deleting any column we need to use drop command
Ex:df7.drop("city")
This will delete the column named city in the data.
```



