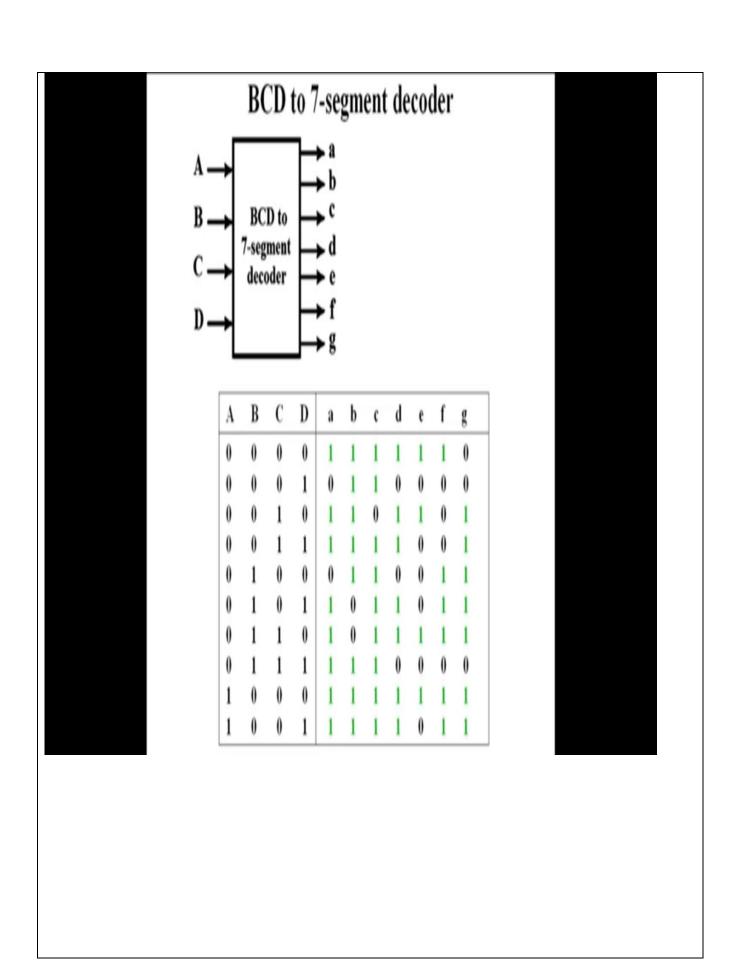
DAILY ASSESSMENT FORMAT

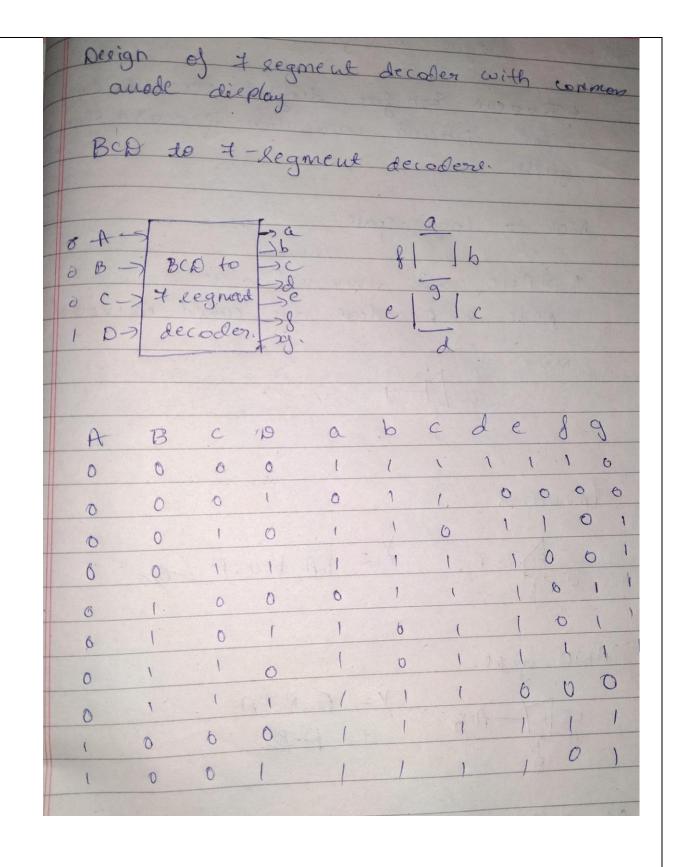
Date:	27-5-2020	Name:	Bhavana.B
Course:	Logic Design	USN:	4AL18EC009
Topic:	1.Boolean equations for digital circuits. Combinational circuits: Conversion of MUX and Decoders to logic gates. 2.design of 7 segment decoder with common anode display	Semester & Section:	4th sem A section
Github Repository :	Bhavana-b		

	FORENOON SESSION DETAILS	
Image of session		



Report:	

Logic delign & Boolean Egn for digital circuil combin alional circuit convention of max da acodex gatte. Max to logic ceate. * NAND, NOR: universal gates. + prat o pecodeou are called cuivoual get MUX A-1-1-12 (nvortors Y= 1,A + 0, A =A/ AND gate. Y= O, R+A = A-B/ OR gate. EX-CE ET - WOR -A+B



Date: 27-5-2020 Name: Bhavana.B

Course: Python USN: 4al18ec009

Topic: 1.Application 5: Build a Semester & Section: 4th sem A section

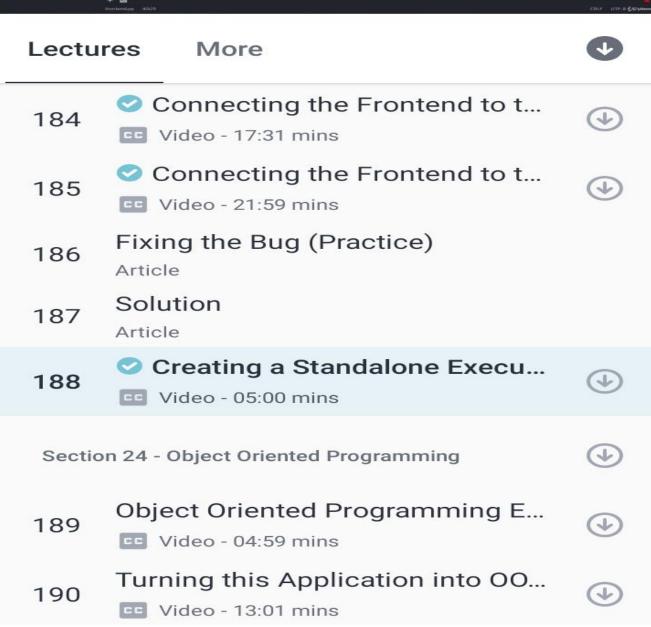
Desktop Database

Application

AFTERNOON SESSION DETAILS

Image of session





Report:

Date
section: -23.
Application 5
* Desktop Database app
2 frontend Enterface Design
+ Backend
to connecting the frontend to backend t (earn how to fixing the Bug
+ Orealing a standard Exceutable verse
of the program.