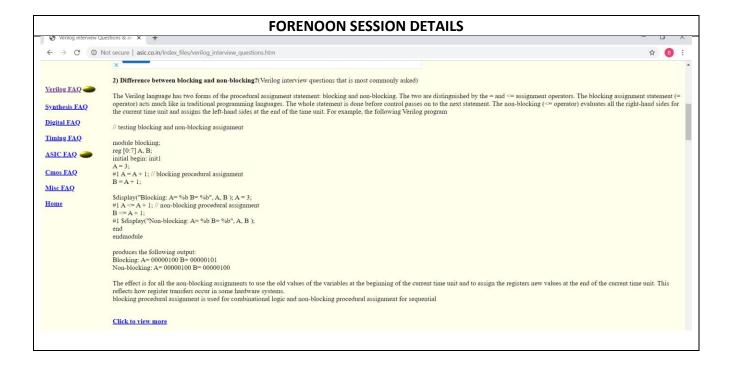
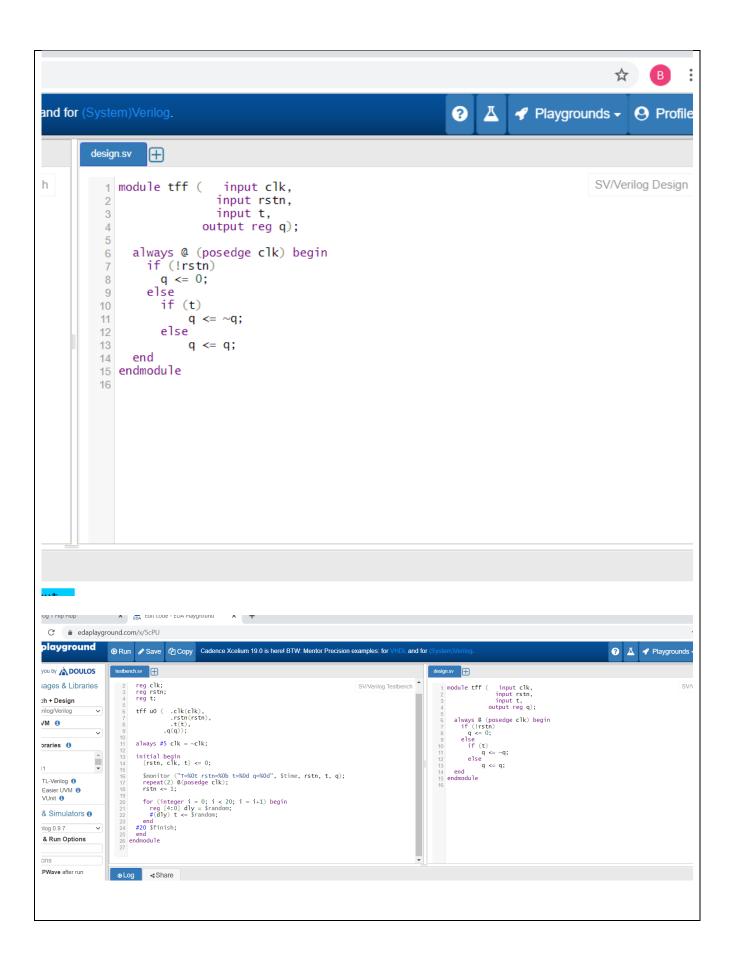
DAILY ASSESSMENT FORMAT

Date:	4-06-2020	Name:	BINDUSHRI
Course:	Digital design using HDL	USN:	4AL17EC011
Topic:	1.hardware modeling using Verilog 2.interview questions 3.TASK		6 th A
Github	Bindushri		
Repository:			





Day-4 Hardware modeling using warrang. - Design composity invaring rapidly - Increased sig & complexity - Kapircason technology simplexing - CAO tooks are essential moores laces Exponounce growth Destyn complexely extense rapidly Standard 201 de 189 n Procedure - starting from the deign foles diouen to the actual 9 mpermentation - Generate a neteror of gates / thep-fops or standard coop - Interuleur question 1) were long code to snow contents of twee regasters worth of without a temporary register? asways @ (poudge clock) began temp=b; b=a; a=temp; end without temp reg; acuars @ Gosoage Clock) begin ac=b; b <= a;

end

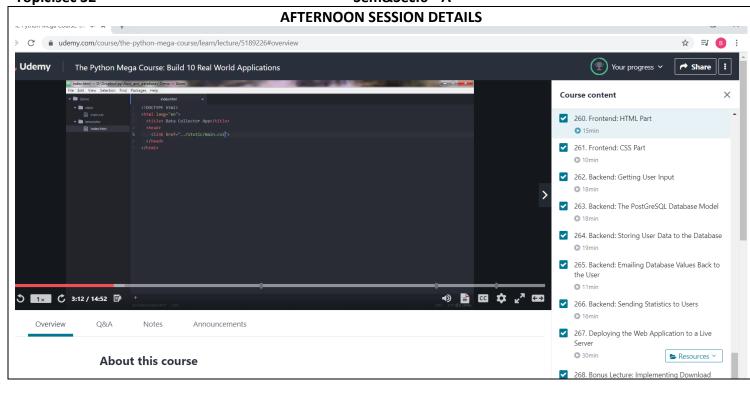
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Date:4june2020

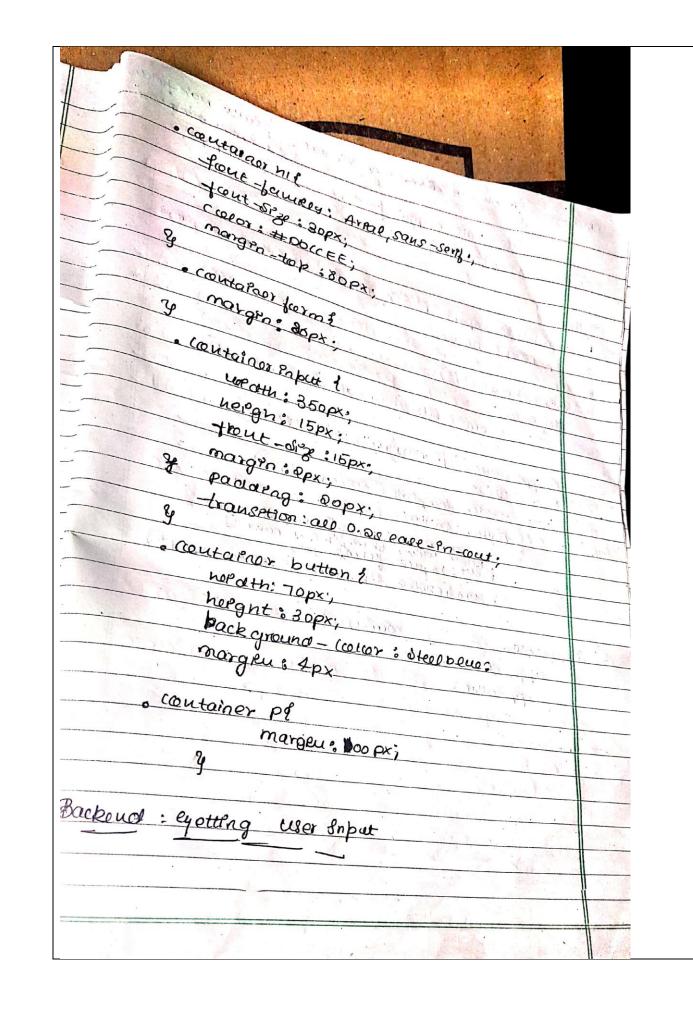
Course: python Topic:sec 32

Name:Bindushri USN:4AL17EC011 Sem&Sec:6th A



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