

DAILY ASSESSMENT FORMAT

Date:	2-06-2020	Name:	BINDUSHRI
Course:	Digital design using hdl	USN:	4AL17EC011
Topic:	1.fpga basics architechture,application and uses. 2.verilog hdl basics 3.test bench waveform 4.task2	Semester & Section:	6 th A
Github Repository:	Bindushri		

FORENOON SESSION DETAILS

youtube.com/watch?v=F65QSRMfh1o

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```

module testbench;
  reg a, b, c; wire sum, cout;
  full_adder FA (sum, cout, a, b, c);

  initial
  begin
    $monitor ($time, " a=%b, b=%b, c=%b, sum=%b, cout=%b",
              a, b, c, sum, cout);
    #5 a=0; b=0; c=1;
    #5 b=1;
    #5 a=1;
    #5 a=0; b=0; c=0;
    #5 $finish;
  end
endmodule

```

It this is the first approach and this kind of test bench you have already seen earlier

0	a=x	b=x	c=x	sum=x	cout=x
5	a=0	b=0	c=1	sum=1	cout=0
10	a=0	b=1	c=1	sum=0	cout=1
15	a=1	b=1	c=1	sum=1	cout=1
20	a=0	b=0	c=0	sum=0	cout=0

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Intel FPGA

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An Example Verilog Test Bench

CompArchIllinois

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Verilog System Tasks (\$display, \$monitor, \$strobe, \$time, \$writeb, \$writew, \$writec, \$writexl, \$writexs, \$writexd, \$writexw, \$writexh, \$writexl, \$writexs, \$writexd, \$writexw, \$writexh)

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Hardware Modeling using Verilog

Computer Science and Engineering

The Art of Code - Dylan Beattie

NDC Conferences

WRITING VERILOG TEST BENCHES

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X — X — X — X

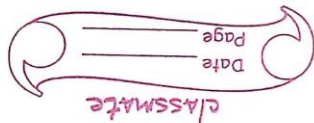
2-06-2020 :- "FPGA Basics Architecture, applications and uses."

FPGA is an internal circuit that consists of external hardware blocks with the user programmable interconnects to customize operation for a specific application.

→ FPGA has 200K → PROMs & PLDs

→ FPGA architecture consists of thousands of fundamental elements called configurable logic blocks.

→ FPGA uses the high speed search: MPOROS using EPDS in its data centre - known as search algorithm.



Verilog HDL Basics

RTL \rightarrow type of behavioural modeling for the purpose of synthesis

module module_name(port_list);

Port declarations

data type declarations

Circuit functionality

timing specifications

endmodule

variable data type \rightarrow element to store data temporarily

net data type \rightarrow physical interconnect b/w structure

\rightarrow type
 \rightarrow wire

ex: module clr_reg

{

output reg clr

};

initial clr = 1'b0;

always

#(period) clr = ~clr;

initial #100 \$finish

endmodule

Procedural assignments: ① Blocking (=) ② Non blocking (<=)

\rightarrow Verilog test bench code to verify the design under test

module full_adder(S, (o, a, b, c);

input a, b, c;

output S, Co;

assign S = a ^ b ^ c;

assign Co = (a & b) | (b & c) | (c & a);

endmodule

module testbench

reg a, b, c; wire sum, cout;

full_adder FA(sum, cout, a, b, c);

initial

begin

\$monitor(\$time, "a=%b, b=%b,

c=%b, sum=%b, cout=%b",

a, b, c, sum, cout);

#5 a=0, b=0, c=1;

#5 b=1;

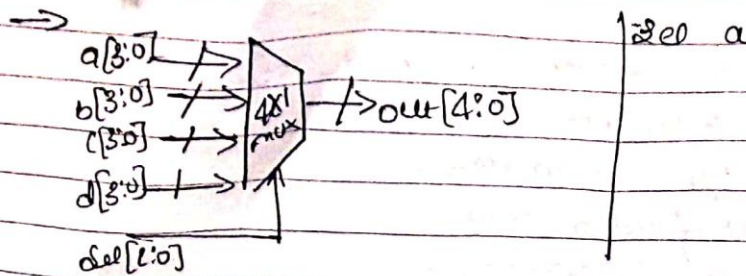
#5 a=1;

#5 a=0, b=0, c=0;

\$stop

endmodule

Task day 2 Implement a 4:1 mux and write the test bench code to verify the module



• using assign statement

```
module mux_4to1_assign(input [3:0] a,
                      input [3:0] b,
                      input [3:0] c,
                      input [3:0] d,
                      input [1:0] sel,
                      output [3:0] out);
```

```
    out[3:0] = sel[1] ? (sel[0] ? a : c) : (sel[0] ? b : d);
endmodule.
```

using case statement

```
module mux_4to1_case(input [3:0] a,
                    input [3:0] b,
                    input [3:0] c,
                    input [3:0] d,
                    input [1:0] sel,
                    output reg [3:0] out);
```

always @(a or b or c or d or sel) begin.

case (sel)

2'b00: out <= a;

2'b01: out <= b;

2'b10: out <= c;

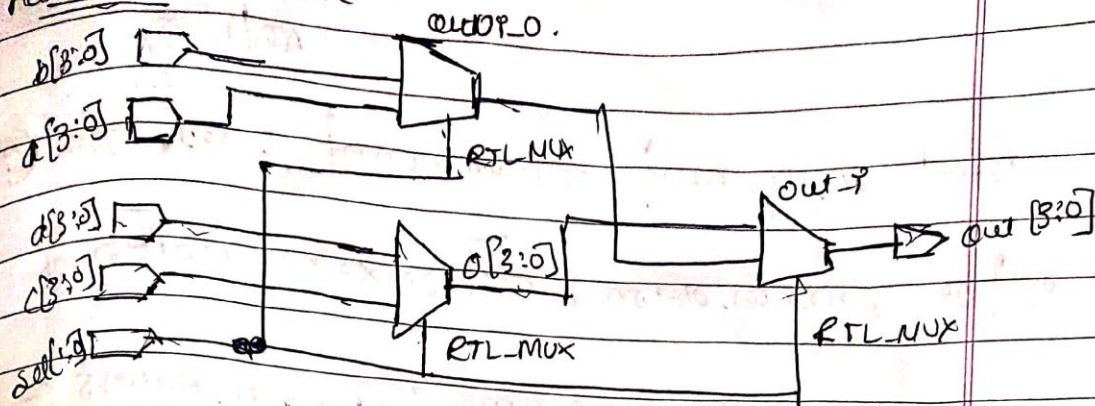
2'b11: out <= d;

endcase

end

endmodule.

Hardware Schematic



module tb_4to1_mux;

reg [3:0] a;

reg [3:0] b;

reg [3:0] c;

reg [3:0] d;

wire [3:0] out;

reg [1:0] sel;

integer i;

mux_4to1_rtl_mux0 (.a(a),
 .b(b),
 .c(c),
 .d(d),
 .sel(sel),
 .out(out);

RTL-Testbench

\$monitor ("[0:0] sel = 0x%0h a = 0x%0h b = 0x%0h c = 0x%0h

d = 0x%0h out = 0x%0h, \$time, sel, a,

sel <= 0;

a <= \$random;

b <= \$random;

c <= \$random;

d <= \$random;

for (i = 1; i < 4; i = i + 1) begin

end

#5 finish;

endmodule

Date: 2 June 2020

Course: python

Topic: sec30

Name: Bindushri

USN: 4AL17EC011

Sem & Sec: 6th A

AFTERNOON SESSION DETAILS

Image of session

The screenshot displays the Udemy interface for the course 'The Python Mega Course: Build 10 Real World Applications'. The main video player shows a Jupyter Notebook with Python code for web scraping. The course content sidebar on the right lists lessons 248 through 254, with lesson 253 'Saving the Extracted Data in CSV Files' highlighted. The 'About this course' section describes it as a complete Python course for beginners and intermediates.

Course content

- 248. Request Headers (1min)
- 249. Loading the Webpage in Python (7min)
- 250. Extracting "div" Tags (12min)
- 251. Extracting Addresses and Property Details (15min)
- 252. Extracting Elements without Unique Identifiers (12min)
- 253. Saving the Extracted Data in CSV Files (8min)
- 254. Crawling Through Webpages (17min)

Section 31: Application 8: Build a Web-based Financial Graph
0 / 12 | 1hr 40min

Section 32: Application 9: Build a Data Collector Web App with PostGreSQL and ...
0 / 11 | 2hr 47min

About this course

A complete Python course for both beginners and intermediates! Master Python 3 by making desktop, web, and mobile apps.

2-06-2020 Sec: 30. Scrape Real Estate property
Data from the web

→ Jupyter Notebook

1. Import request
2. from bs4 import BeautifulSoup

```
In[7] r = requests.get("http://www.century21.com/real-estate/  
rock-spring-wy/LEWYROCKSPRING")  
c = r.content
```

```
In[7] Soup = BeautifulSoup(c, "html.parser")  
print
```

```
In[3] all = Soup.find_all("div", {"class": "propertyRow"})
```

```
In[7] all[0].find("div", {"class": "prop Price"}).text.replace  
("\n", "").replace(" ", "")
```

\$725,000


```

In[]: for item in all:
    print(item.find("h4", {"class": "PropPico"}).
          text.replace("\n", " ").replace(" ", "&nbsp;")

```

```

print(item.find_all("span", {"class": "PropAddress"}).
      [0].text)

```

```

print(item.find_all("span", {"class": "PropAddress"}).
      [0].text)

```

try:

```

print(item.find("span", {"class": "RefObj"}).
      find("b").text)

```

except:

```

print(" ") print("none")

```

Print(" ")

↳ Extracting elements without unique.

```

for column_group in item.find_all("div", {"class":
  "column-dropt"}):

```

```

    print(column_group)

```

```

- for feature_group, feature_name in zip(
  column_group.find_all("span", {"class":
    "feature-dropt"}), column_group.find_all(
    "span", {"class": "feature-name"}):

```

```

    print(feature_group.text, feature_name.text)

```

```

- If "hot size" in feature_group.text:

```

```

    print(feature_name.text)

```

```

- Print(" ")

```


Summary

learnt extract Real estate property data from the web.

using the BeautifulSoup, Pandas.

* learnt on scrolling through webpage.

also saving the Extracted Data in CSV file.

X — X — X — X

Python excersise program:

```
import cv2, time
```

```
first_frame = None
```

```
video = cv2.VideoCapture(0)
```

```
while True:
```

```
    check, frame = video.read()
```

```
    gray = cv2.cvtColor(frame, cv2.COLOR_BGR2GRAY)
```

```
    gray = cv2.GaussianBlur(gray,(21,21),0)
```

```
    if first_frame is None:
```

```
        first_frame = gray
```

```
delta_frame = cv2.absdiff(first_frame, gray)
thresh_frame = cv2.threshold(delta_frame, 30, 255, cv2.THRESH_BINARY)[1]
thresh_frame = cv2.dilate(thresh_frame, None, iterations = 2)
```

```
(cnts, _) = cv2.findContours(thresh_frame.copy(), cv2.RETR_EXTERNAL,
cv2.CHAIN_APPROX_SIMPLE)
```

```
for contour in cnts:
    if cv2.contourArea(contour) < 1000:
        continue
    (x, y, w, h) = cv2.boundingRect(contour)
    cv2.rectangle(frame, (x, y), (x + w, y + h), (0, 255, 0), 3)
```

```
cv2.imshow("Gray Frame", gray)
cv2.imshow("Delta Frame", delta_frame)
cv2.imshow("Threshold Frame", thresh_frame)
cv2.imshow("Color Frame", frame)
```

```
key = cv2.waitKey(1)
print(gray)
print(delta_frame)
```

```
if key == ord('q'):
    break
```

```
video.release()
cv2.destroyAllWindows
```

