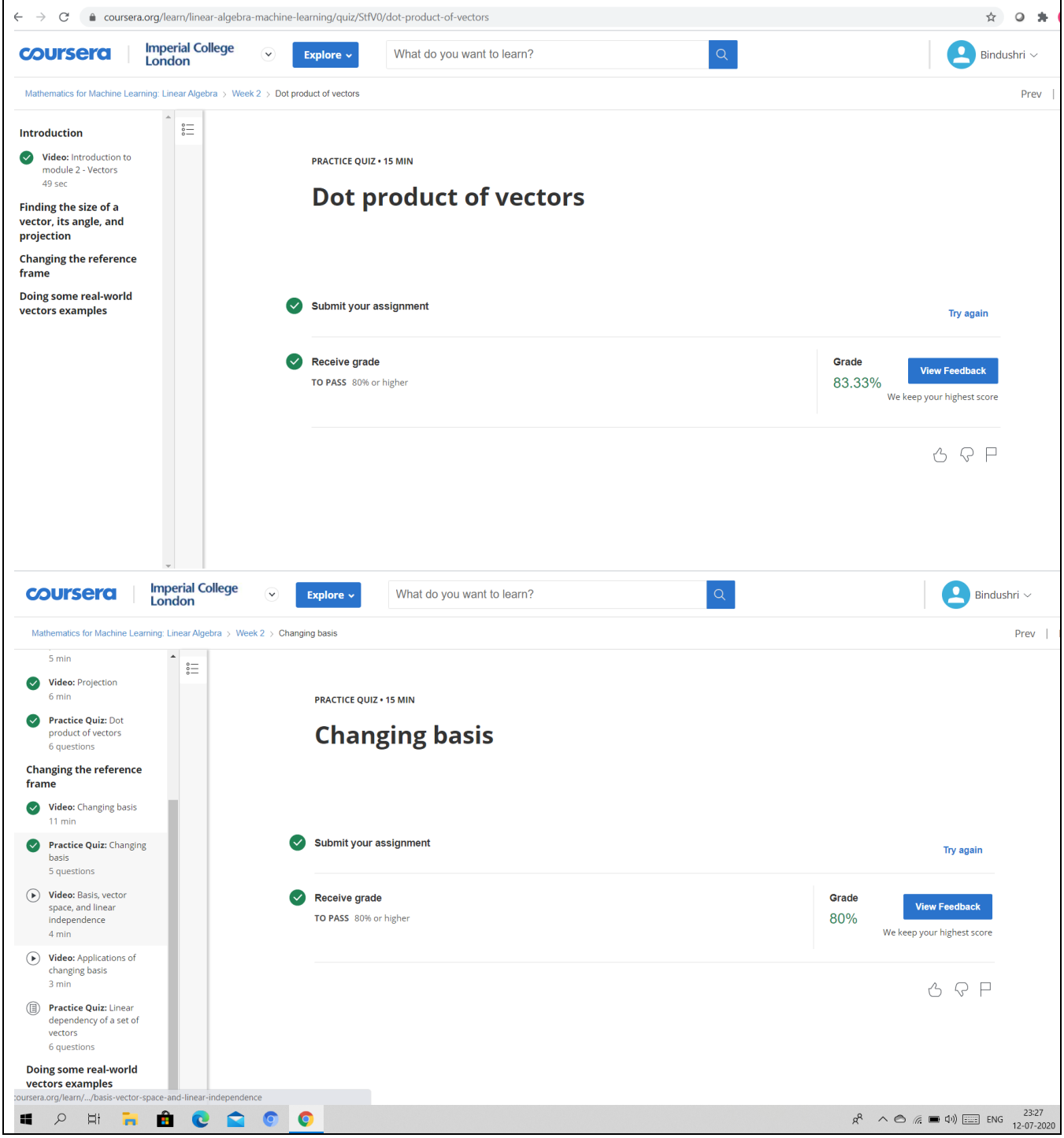
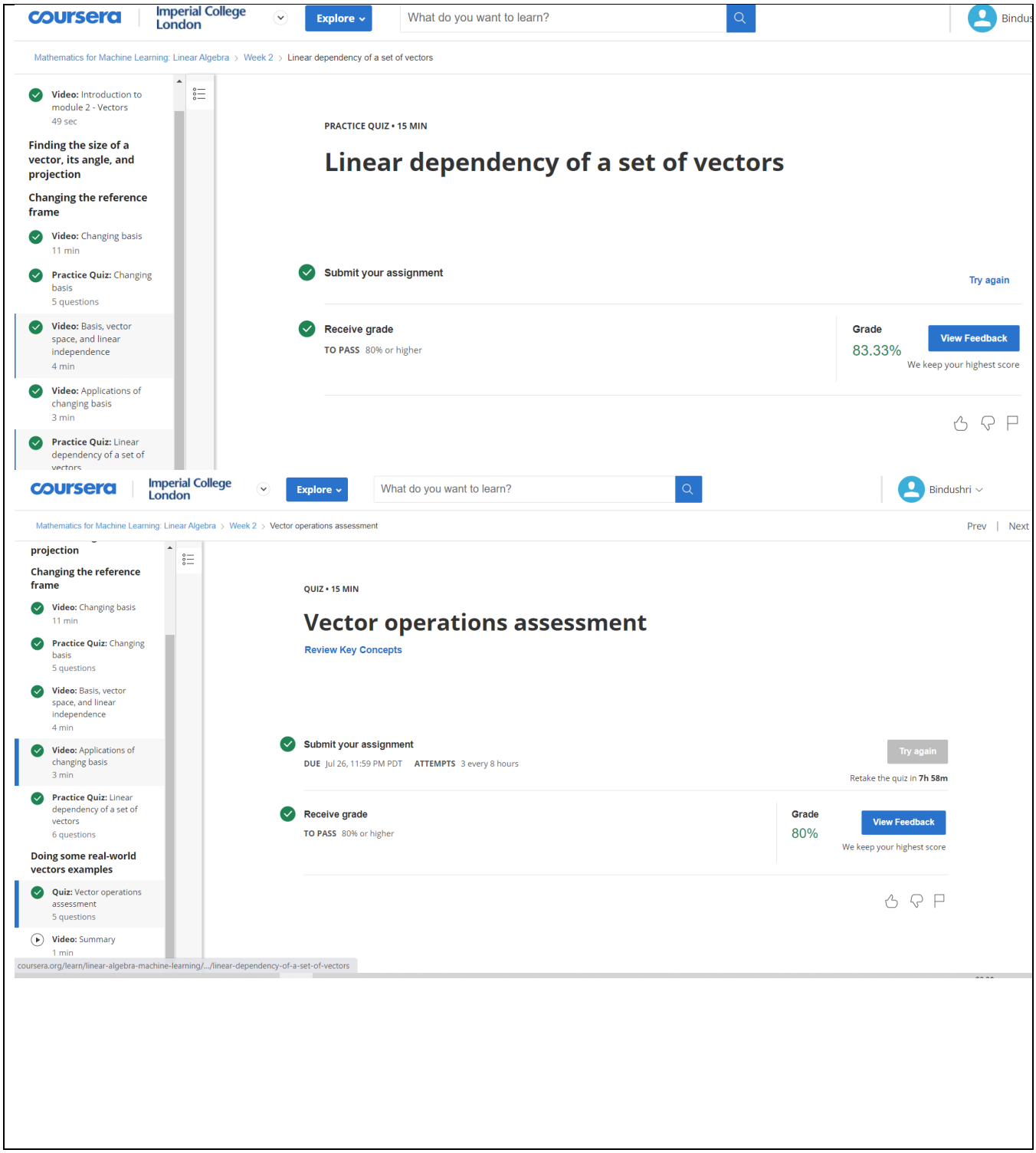
DAILY ASSESSMENT FORMAT

Date:	**13-07-2020**	**Name:**	**BINDUSHRI**
Course:	**Mathematics for machine learning:linear algebra (coursera)**	**USN:**	**4AL17EC011**
Topic:	**Week-2**	**Semester & Section:**	**6th sem&Asec**
Github repository	**Bindushri**		

FORENOON SESSION DETAILS (9.00am to 1.00pm)




coursera
Imperial College London
Explore
What do you want to learn?
Bindus
Mathematics for Machine Learning: Linear Algebra > Week 2 > Linear dependency of a set of vectors
Video: Introduction to module 2 - Vectors
49 sec
Finding the size of a vector, its angle, and projection
Changing the reference frame
Video: Changing basis
11 min
Practice Quiz: Changing basis
5 questions
Video: Basis, vector space, and linear independence
4 min
Video: Applications of changing basis
3 min
Practice Quiz: Linear dependency of a set of vectors
PRACTICE QUIZ • 15 MIN
Linear dependency of a set of vectors
Submit your assignment
Try again
Receive grade
TO PASS 80% or higher
Grade
83.33%
View Feedback
We keep your highest score
coursera
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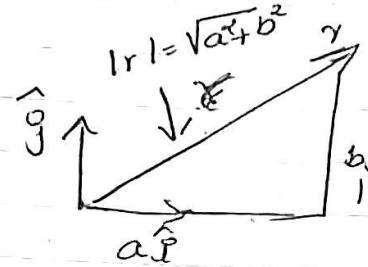
Explore
What do you want to learn?
Bindushri
Mathematics for Machine Learning: Linear Algebra > Week 2 > Vector operations assessment
Prev | Next
projection
Changing the reference frame
Video: Changing basis
11 min
Practice Quiz: Changing basis
5 questions
Video: Basis, vector space, and linear independence
4 min
Video: Applications of changing basis
3 min
Practice Quiz: Linear dependency of a set of vectors
6 questions
Doing some real-world vectors examples
Quiz: Vector operations assessment
5 questions
Video: Summary
1 min
QUIZ • 15 MIN
Vector operations assessment
Review Key Concepts
Submit your assignment
DUE Jul 26, 11:59 PM PDT ATTEMPTS 3 every 8 hours
Try again
Retake the quiz in 7h 58m
Receive grade
TO PASS 80% or higher
Grade
80%
View Feedback
We keep your highest score
coursera.org/learn/linear-algebra-machine-learning/.../linear-dependency-of-a-set-of-vectors

Week-2

* Mathematics for Machine learning : Linear Algebra

Introduction to vector

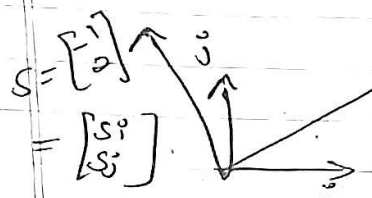
modulus & inner part



$r = ai + bj = \begin{bmatrix} a \\ b \end{bmatrix}$

$r = \left| \begin{matrix} a \\ b \end{matrix} \right|$

$|r| = \sqrt{a^2+b^2}$



$s \cdot r = r_i s_i + r_j s_j$ Communicative

$3 \times -1 + 2 \times 2$

$= 1$ s.r

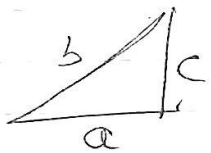
distributive over addition

$r \cdot (s+t) = r * s + r * t$

$r = \begin{bmatrix} r_1 \\ r_2 \\ r_n \end{bmatrix} \quad s = \begin{bmatrix} s_1 \\ s_2 \\ s_n \end{bmatrix} \quad t = \begin{bmatrix} t_1 \\ t_2 \\ t_n \end{bmatrix}$

$r \cdot (s+t) = r_1(s_1+t_1) + r_2(s_2+t_2) + \dots + r_n(s_n+t_n)$

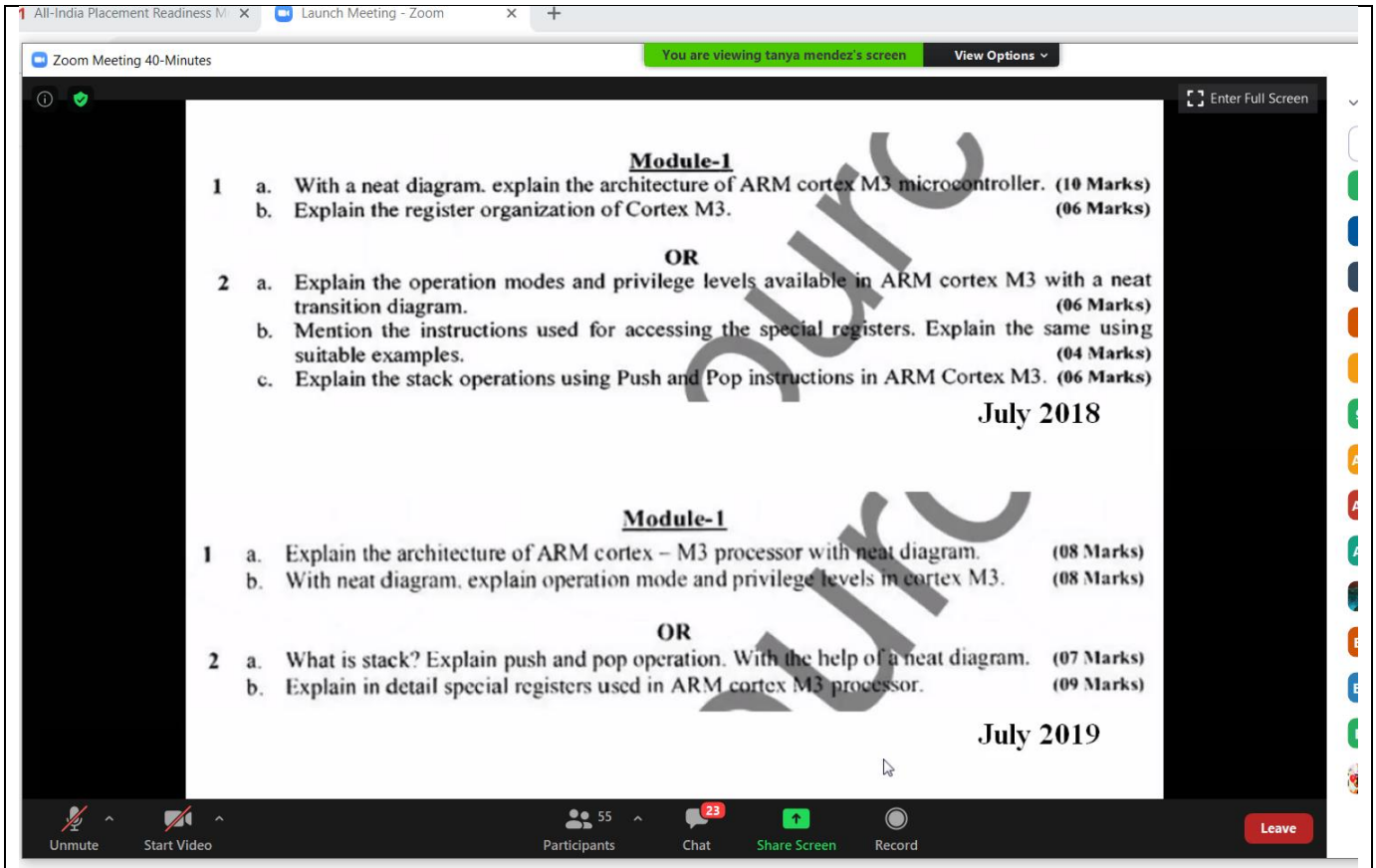
$= r_1 s_1 + r_1 t_1 + r_2 s_2 + r_2 t_2 + \dots + r_n s_n + r_n t_n$

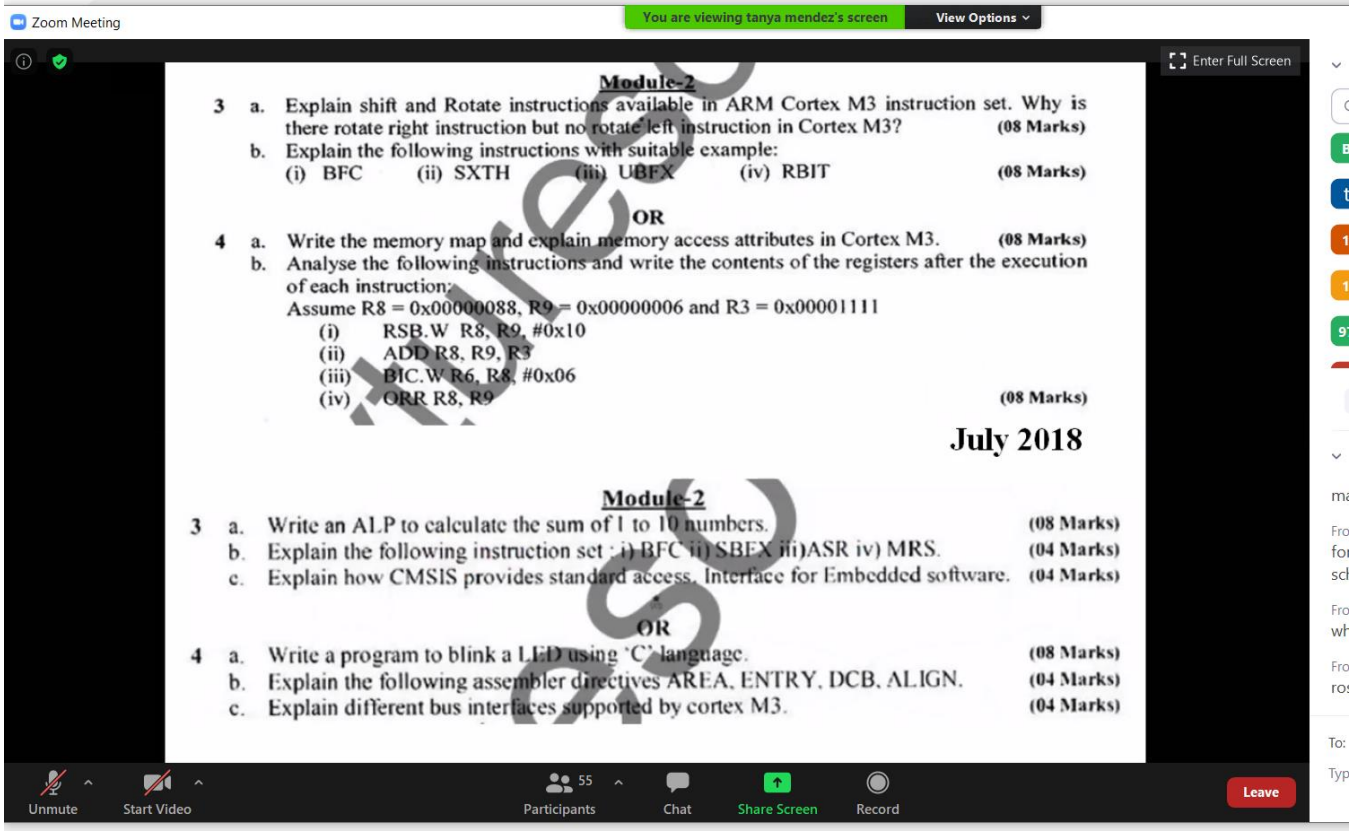


DAILY ASSESSMENT FORMAT

Date:	**13-07-2020**	**Name:**	**BINDUSHRI**
Course:	**AMES**	**USN:**	**4AL17EC011**
Topic:	**revision**	**Semester & Section:**	**6th Asec**

AFTERNOON SESSION DETAILS(2.00pm to 5.00pm)


Zoom Meeting 40-Minutes
You are viewing tanya mendez's screen
View Options
Enter Full Screen
Module-1
1 a. With a neat diagram. explain the architecture of ARM cortex M3 microcontroller. (10 Marks)
b. Explain the register organization of Cortex M3. (06 Marks)
OR
2 a. Explain the operation modes and privilege levels available in ARM cortex M3 with a neat transition diagram. (06 Marks)
b. Mention the instructions used for accessing the special registers. Explain the same using suitable examples. (04 Marks)
c. Explain the stack operations using Push and Pop instructions in ARM Cortex M3. (06 Marks)
July 2018
Module-1
1 a. Explain the architecture of ARM cortex – M3 processor with neat diagram. (08 Marks)
b. With neat diagram. explain operation mode and privilege levels in cortex M3. (08 Marks)
OR
2 a. What is stack? Explain push and pop operation. With the help of a neat diagram. (07 Marks)
b. Explain in detail special registers used in ARM cortex M3 processor. (09 Marks)
July 2019
Unmute
Start Video
55
Participants
23
Chat
Share Screen
Record
Leave


Zoom Meeting
You are viewing tanya mendez's screen
View Options
Enter Full Screen
Module-2
3 a. Explain shift and Rotate instructions available in ARM Cortex M3 instruction set. Why is there rotate right instruction but no rotate left instruction in Cortex M3? (08 Marks)
b. Explain the following instructions with suitable example:
(i) BFC (ii) SXTH (iii) UBFX (iv) RBIT (08 Marks)
OR
4 a. Write the memory map and explain memory access attributes in Cortex M3. (08 Marks)
b. Analyse the following instructions and write the contents of the registers after the execution of each instruction:
Assume R8 = 0x00000088, R9 = 0x00000006 and R3 = 0x00001111
(i) RSB.W R8, R9, #0x10
(ii) ADD R8, R9, R3
(iii) BIC.W R6, R8, #0x06
(iv) ORR R8, R9 (08 Marks)
July 2018
Module-2
3 a. Write an ALP to calculate the sum of 1 to 10 numbers. (08 Marks)
b. Explain the following instruction set : i) BFC ii) SBFX iii)ASR iv) MRS. (04 Marks)
c. Explain how CMSIS provides standard access, Interface for Embedded software. (04 Marks)
OR
4 a. Write a program to blink a LED using 'C' language. (08 Marks)
b. Explain the following assembler directives AREA, ENTRY, DCB, ALIGN. (04 Marks)
c. Explain different bus interfaces supported by cortex M3. (04 Marks)
Unmute
Start Video
55
Participants
Chat
Share Screen
Record
Leave

Revision module-1

→ ARM cortex M3 - architechture

memory protection unit → is optional.

NOVIC → it has

R0 to R12:- General purpose register.

R13 : Stack pointers.

MSP → main stack pointer. (default).

② Register organisation

R0

R1

R2

R3

R4

R5

R6

R7

R8

R9

R10

R11

R12

R13 (MSP) R13 (PSP)

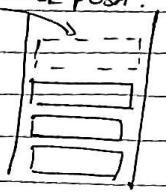
R14

R15

1. Nested interupt support.
2. Vector interupt support
3. Dynamic priority change support
4. Reduction of interupt latency
5. Interupt masking

4) Stack PUSH and POP

Stack push.



R0 0x... → PUSH : stack is decremented by 4 then it is stored.

0x...

PSR.

5) Application of ARM cortexM3 (5 Application).
→ Used in Real time Application
→ Data communication system
→ Industrial control. Application

6) Thumb2 (short note).

module-2

Problem

(9) RSB.W R8, R9, #0x10
RSB.W Rd, Rn, #immediate.
Rd = #immediate − Rn
Reverse Subtract

:- ARM cortex m3 has also having special Register.

1. PSRs
2. PRIMASK, FAULTMASK, BASEPRI
3. CONTROL.

Name	Functions
XPSR	Progma status Registers. (APSR (Arithmatic flag), IPSR (Interrupt), EPSR (Enabled IF THEN))
PRIMASK	Interupt Mask Register.
FAULTMASK	
BASEPRI	
CONTROL	control Register.

Special Register.

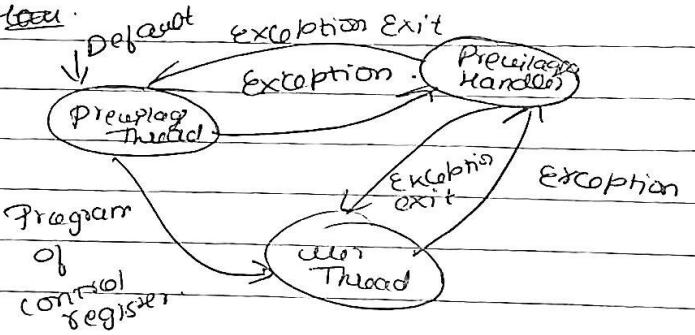
control status Register :- It has 2 bits,
If bit is set to 0 privilage mode and
If bit set 1 _____.

3. explain operation mode & previlaged level of cortex m3.

-> has two modes & two privilage levels.

- Thread mode.
- Handler Mode.

Reset.



NVIC -> features.

- closely coupled to the processor core