**DAILY ASSESSMENT FORMAT**

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| **Date:** | **4 june 2020** | **Name:** | **Divyashri Bahubali Samajage** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC031** |
| **Topic:** | **1. Hardware modelling using verilog**  **2. FPGA and ASIC Interview questions** | **Semester & Section:** | **6TH SEM & ‘A’ SEC** |
| **Github Repository:** | **Divyashri-cource** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
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| **Date:4 june 2020** |  | **Name:Sanketh S Acharay** |  |
| **Course:** |  | **USN:4AL17EC084** |  |
| **Topic:** |  | **Semester & Section:6TH SEM&’B’ SEC** |  |
| **AFTERNOON SESSION DETAILS** | | | |
| **Bonus lecture on Electrical Engineering by Prof. Aniruddhan IIT Madras** | | | |
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