**DAILY ASSESSMENT FORMAT**

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| --- | --- | --- | --- | --- | --- | --- |
| **Date:** | **04/06/2020** | | **Name:** | **Abhishek Vasudev Mahendrakar** | | |
| **Course:** | **Digital Design using HDL** | | **USN:** | **4AL17EC003** | | |
| **Topic:** | 1. Hardware modelling using Verilog 2. FPGA and ASIC Interview questions | | **Semester & Section:** | **6th-‘A’** | | |
| **Github Repository:** | **ECEAbhishekVMahendrakar** | | **E-mail:** | **abhi2244mahendrakar@gmail.com** | | |
| **FORENOON SESSION DETAILS** | | | | | |
| **Image of session** | | | | | |
| **Report – Report can be typed or hand written for up to two pages.** | | | | | |
| **Date:** | **/5/2020** | **Name:** | | | **Abhishek Vasudev Mahendrakar** |
| **Course:** | **UDEMY-The Python Mega Course: Build 10 real world applications** | **USN:** | | | **4AL17EC003** |
| **Topic:** |  | **Semester & Section:** | | | **6th-‘A’** |
| **AFTERNOON SESSION DETAILS** | | | | | |
| **Image of session** | | | | | |
| **Report – Report can be typed or hand written for up to two pages.** | | | | | |