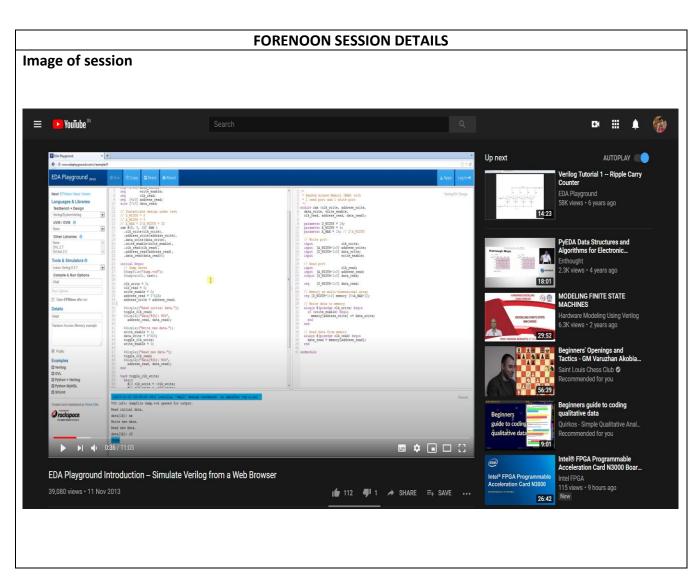
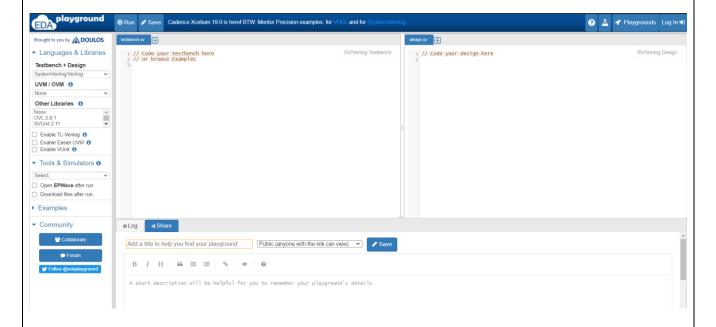
DAILY ASSESSMENT REPORT

Date:	03 June 2020	Name:	Gagan M K
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC032
Topic:	 EDA Playground Online complier EDA Playground Tutorial Demo Video How to Download And Install Xilinx Vivado Design Suite Vivado Design Suite for implementation of HDL code 	Semester & Section:	6 th sem & 'A' sec
Github Repository:	Alvas-education- foundation/Gagan-Git		



Report – Report can be typed or hand written for up to two pages.

EDA Playground Online complier:

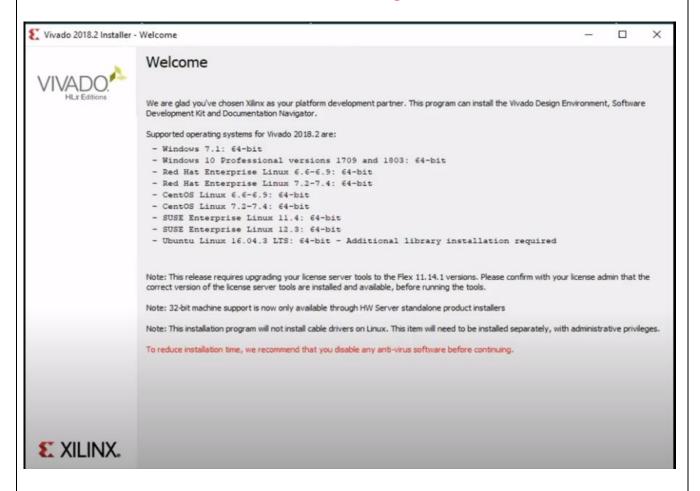


EDA Playground Tutorial Demo Video:

```
testbench.sv.
                                                                                       design.sv
                                                                SV/Verilog Testbench
                                                                                          1 // Code your design here
2 module inverter(a, y);
                                                                                                                                      SV/Verilog Design
  1 // Code your testbench here
  2 // or browse Examples
  3 'timescale lns/lps
                                                                                              input a;
                                                                                              output y;
 5 module testbench();
                                                                                              assign y = \sim a;
                                                                                          6 endmodule
      reg al;
      wire y1;
      inverter inv1(a1, y1);
 10
      initial begin
        a1 = 1'b1;
$display("a=%b",a1);
$display("y=%b",y1);
      end
 16
 18 endmodule
⊚Log

Share
testbench.sv:3: warning: Some modules have no timescale. This may cause
                    : confusing timing results. Affected modules are:
testbench.sv:3:
                       : -- module inverter declared here: design.sv:2
testbench.sv:3:
a=1
y=Z
```

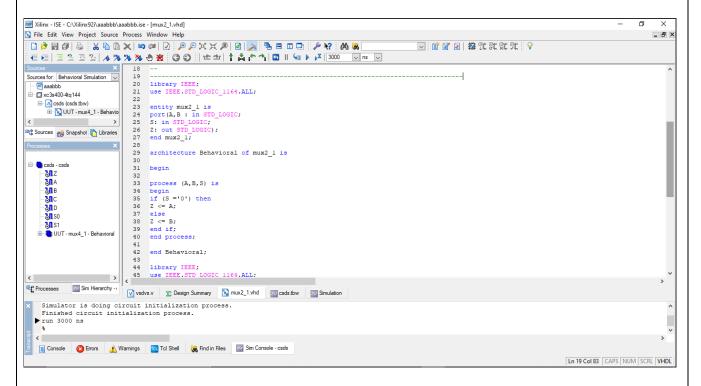
How to Download And Install Xilinx Vivado Design Suite:



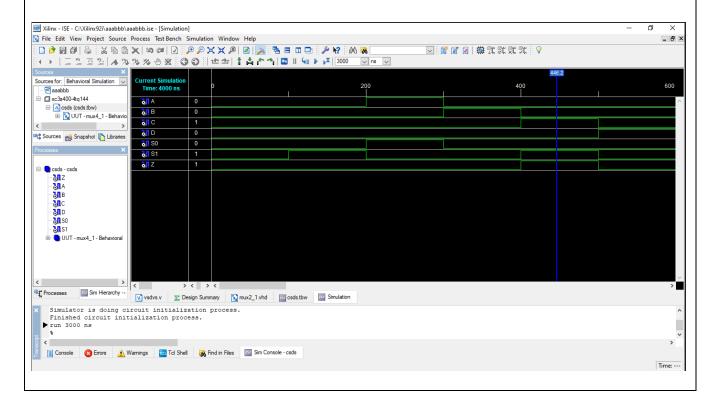
Vivado Design Suite for implementation of HDL code:

TASK:

Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.



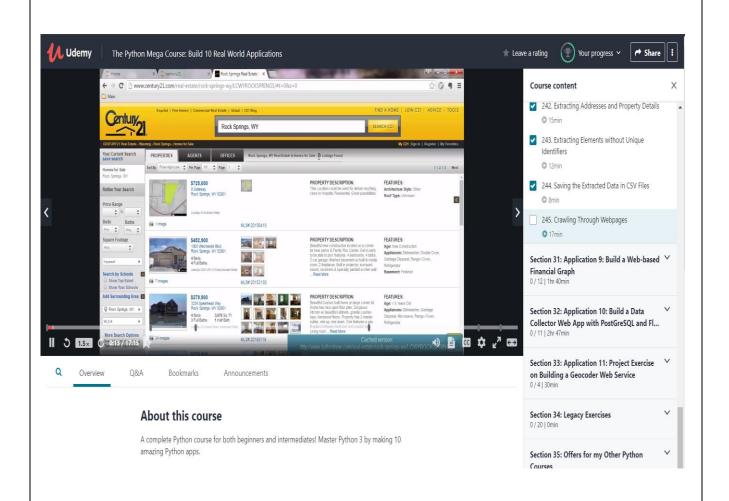
OUTPUT:



Date:	03 June 2020	Name:	Gagan M K
Course:	The Python Mega Course	USN:	4AL17EC032
Topic:	Application 8: Scrape Real Estate	Semester	6 th sem & 'A' sec
	Property Data from the Web	& Section:	

AFTERNOON SESSION DETAILS

Image of session:



Report – Report can be typed or hand written for up to two pages.

Scrape Real Estate Property Data from the Web:

- In this application we learnt how to collect data from various websites using python.
- We learnt about loading the webpages in python.
- We learnt to extract the "div" tags.
- We learnt about extracting addresses and property details.
- We learnt about extracting elements without unique identifiers.
- We learnt how to save the obtained data in .csv format.
- And also we learnt to extract data from various websites at a time using crawling through websites using python.
- The output obtained from website is saved in excel sheet as shown below.

