

## DAILY ASSESSMENT REPORT

Date:	04 June 2020	Name:	Gagan M K
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC032
Topic:	<ul style="list-style-type: none"> <li>Hardware modelling using Verilog</li> <li>FPGA and ASIC Interview questions</li> </ul>	Semester & Section:	6 <sup>th</sup> sem & 'A' sec
GitHub Repository:	Alvas-education-foundation/Gagan-Git		

### FORENOON SESSION DETAILS

Image of session

The screenshot shows a YouTube video player interface. The main video is titled "Introduction" and is part of a series on "Hardware Modeling using Verilog". The video has 41,568 views and was uploaded on 18 Aug 2017. The speaker is a man with glasses, wearing a blue shirt. The video player includes a search bar at the top, a list of related videos on the right, and a "Helping you connect" banner at the bottom. The video player also shows the current time as 3:23 / 28:00.

**Report – Report can be typed or hand written for up to two pages.**

### **Hardware modelling using Verilog:**

- **Learnt about the Verilog hardware description language.**
- **Understood the difference between behavioral and structural design styles.**
- **Learnt to write test benches and analyze simulation results.**
- **Learnt to model combinational and sequential circuits.**
- **Distinguish between good and bad coding practices.**
- **Case studies with some complex designs.**

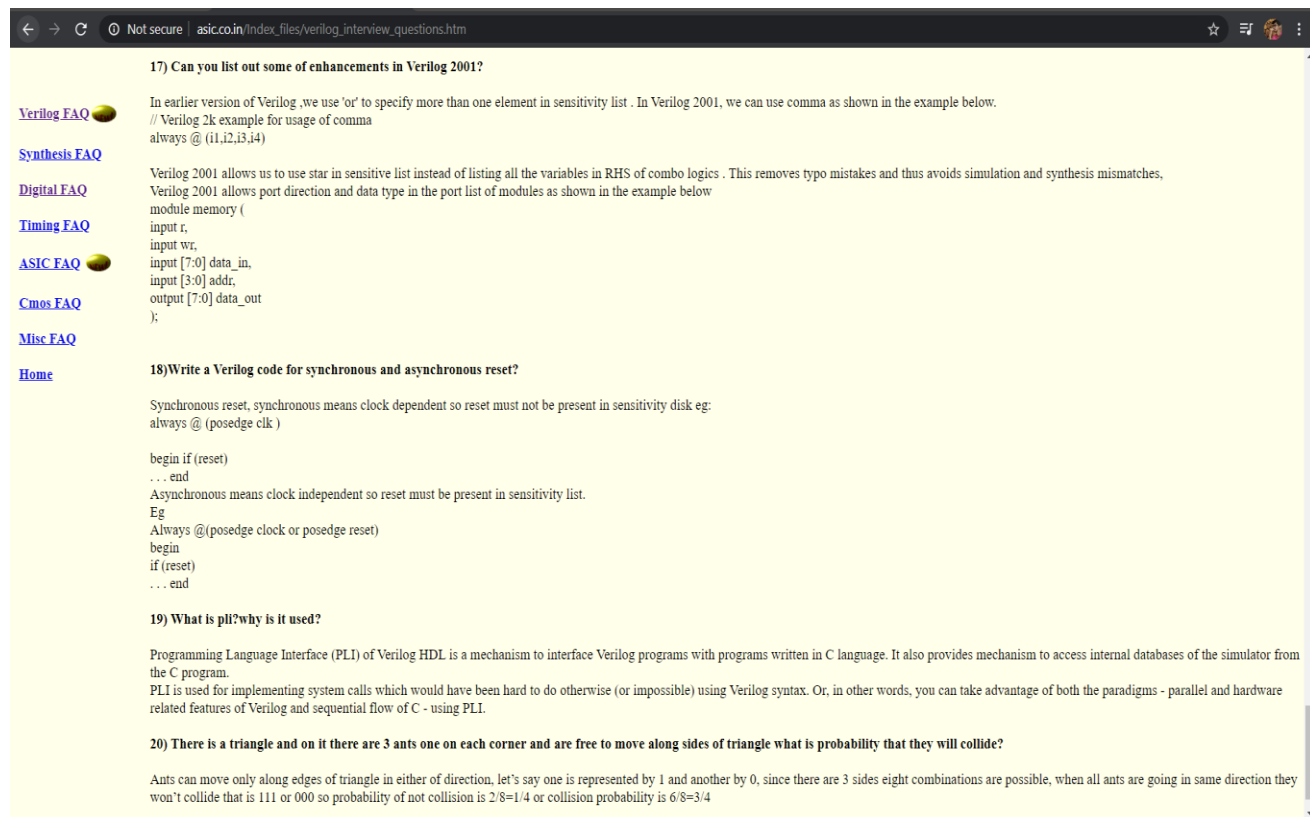
- **Logic design**
  - Generate a netlist of gates/flip-flops or standard cells.
  - A standard cell is a pre-designed circuit module (like gates, flip-flops, multiplexer, etc.) at the layout level.
  - Various logic optimization techniques are used to obtain a cost effective design.
  - There may be conflicting requirements during optimization:
    - Minimize number of gates.
    - Minimize number of gate levels (i.e. delay).
    - Minimize signal transition activities (i.e. dynamic power).
- **Physical design and Manufacturing**
  - Generate the final layout that can be sent for fabrication.
  - The layout contains a large number of regular geometric shapes corresponding to the different fabrication layers.
  - Alternatively, the final target may be Field Programmable Gate Array (FPGA), where technology mapping from the gate level netlist is used.
    - Can be programmed in-field.
    - Much greater flexibility, but less speed.

## **Other Steps in the Design Flow**

- **Simulation for verification**
  - At various levels: logic level, switch level, circuit level
- **Formal verification**
  - Used to verify the designs through formal techniques
- **Testability analysis and Test pattern generation**
  - Required for testing the manufactured devices

## FPGA and ASIC Interview questions:

- Gone through the most frequently asked questions from Verilog in Interviews.



17) Can you list out some of enhancements in Verilog 2001?

In earlier version of Verilog ,we use 'or' to specify more than one element in sensitivity list . In Verilog 2001, we can use comma as shown in the example below:  
// Verilog 2k example for usage of comma  
always @(i1,i2,i3,i4)

Verilog 2001 allows us to use star in sensitive list instead of listing all the variables in RHS of combo logics . This removes typo mistakes and thus avoids simulation and synthesis mismatches.  
Verilog 2001 allows port direction and data type in the port list of modules as shown in the example below  
module memory (  
input r,  
input wr,  
input [7:0] data\_in,  
input [3:0] addr,  
output [7:0] data\_out  
);

18) Write a Verilog code for synchronous and asynchronous reset?

Synchronous reset, synchronous means clock dependent so reset must not be present in sensitivity disk eg:  
always @(posedge clk )  
  
begin if (reset)  
... end  
Asynchronous means clock independent so reset must be present in sensitivity list.  
Eg  
Always @(posedge clock or posedge reset)  
begin  
if (reset)  
... end

19) What is pli? why is it used?

Programming Language Interface (PLI) of Verilog HDL is a mechanism to interface Verilog programs with programs written in C language. It also provides mechanism to access internal databases of the simulator from the C program.  
PLI is used for implementing system calls which would have been hard to do otherwise (or impossible) using Verilog syntax. Or, in other words, you can take advantage of both the paradigms - parallel and hardware related features of Verilog and sequential flow of C - using PLI.

20) There is a triangle and on it there are 3 ants one on each corner and are free to move along sides of triangle what is probability that they will collide?

Ants can move only along edges of triangle in either of direction, let's say one is represented by 1 and another by 0, since there are 3 sides eight combinations are possible, when all ants are going in same direction they won't collide that is 111 or 000 so probability of not collision is  $2/8=1/4$  or collision probability is  $6/8=3/4$

## TASK: Implement a simple T Flipflop and test the module using a compiler.

### Design:

```
module tff (    input clk,
               input rstn,
               input t,
               output reg q);

    always @ (posedge clk) begin
        if (!rstn)
            q <= 0;
        else
            if (t)
                q <= ~q;
            else
                q <= q;
    end
endmodule
```

## Testbench:

```
module tb;
  reg clk;
  reg rstn;
  reg t;

  tff u0 ( .clk(clk),
           .rstn(rstn),
           .t(t),
           .q(q) );

  always #5 clk = ~clk;

  initial begin
    {rstn, clk, t} <= 0;

    $monitor ("T=%0t rstn=%0b t=%0d q=%0d", $time, rstn, t, q);
    repeat(2) @(posedge clk);
    rstn <= 1;

    for (integer i = 0; i < 20; i = i+1) begin
      reg [4:0] dly = $random;
      #(dly) t <= $random;
    end
    #20 $finish;
  end
endmodule
```

The screenshot shows a Verilog IDE with two files open: `testbench.sv` and `design.sv`.

**testbench.sv** (SV/Verilog Testbench):

```
1
2
3 module test;
4   reg clk, reset;
5   wire q;
6
7   tff(reset,clk,q);
8
9   initial
10    begin
11      $dumpfile("dump.vcd");
12      $dumpvars(1);
13      reset=1'b1;
14      clk=1'b0;
15      #5 reset=1'b0;
16      #30 $finish;
17    end
18
19    always #1 clk=~clk;
20
21
22 endmodule
```

**design.sv**:

```
1 module tff(input reset, input clk, output reg q);
2   always @(posedge clk) if (reset) q<=1'b0; else q<=~q;
3 endmodule
```

Date:	04 June 2020	Name:	Gagan M K
Course:	The Python Mega Course	USN:	4AL17EC032
Topic:	Application 9: Build a Web-based Financial Graph	Semester & Section:	6 <sup>th</sup> sem & 'A' sec

## AFTERNOON SESSION DETAILS

Image of session:

**Course content**

- 253. Styling the Chart (4min)
- 254. The Concept Behind Embedding Bokeh Charts in a Flask Webpage (11min)
- 255. Note (1min)
- 256. Embedding the Bokeh Chart in a Webpage (16min)
- 257. Deploying the Chart Website to a Live Server (9min)

**Section 32: Application 10: Build a Data Collector Web App with PostgreSQL and FL...**  
0 / 11 | 2hr 47min

**Section 33: Application 11: Project Exercise on Building a Geocoder Web Service**  
0 / 4 | 30min

**Section 34: Legacy Exercises**  
0 / 20 | 0min

**Section 35: Offers for my Other Python Courses**  
0 / 11 | 5min

**About this course**  
A complete Python course for both beginners and intermediates! Master Python 3 by making 10 amazing Python apps.

**Attended Bonus live session on “What is Electrical Engineering?” by Prof. S.Aniruddhan**

**GATE exam**

- A must for Masters degrees in most Indian universities
- In some places, GATE is not mandatory for PhD applicants or for some types of part-time and distance degrees
- Increasingly used by PSUs for ranking applicants
- Different depts/streams may require applicant to write a particular GATE paper e.g. if you want to apply for Masters in Wireless Communications, you will probably be asked to write ECE GATE paper
- Some universities are okay with a non-EE bachelors degree as long as you write the correct GATE paper
- Use NPTEL, IITM video resources for GATE preparation

See <http://www.gate.iitm.ac.in/> for more information

**Top chat replay**

- Shashikant Basniwal good evening all
- Bhargab Nath set set set set set set
- karthika mullapudi Hello sir good evening
- vikas naik ee kar ke bhi to it job hi milta hai
- Azhages San good evening all 🙏
- rajan krishnan hi
- Bhargab Nath kelaaaaaaaaaaaaa...
- shakti shankar pati good evening to all
- vikas naik sir gud evening
- gomathi samyu Good evening all
- Sheshma Bhavani hello sir good evening
- Suparna Maity Good Evening Sir
- Archana Parmar Hello
- Dr. Debabrata Roy good evening sir
- Sushil Chhugani Good Evening Sir
- Karthik Karthik hai
- Dr. Rayudu Peyyala Good evening all

**LIVE \_ What is Electrical Engineering?**  
7,231 views • Streamed live 20 hours ago

557 14 SHARE SAVE ... Up next AUTOPLAY

**Report – Report can be typed or hand written for up to two pages.**

### **Web-based Financial Graph:**

- **How to Download Datasets with Python.**
  - **Learnt analyzing Stock Market Data.**
  - **Plotting Stock Market Data Candlestick Charts.**
  - **Updating Candlestick Charts with Bokeh Quadrants**
  - **Learnt to plot Candlestick Charts with Bokeh Rectangles**
  - **Creating Candlestick Segments**
  - **Stylizing the obtained Chart**
  - **Learnt the Concept Behind Embedding Bokeh**
  - **Sharing the Charts in a Flask Webpage**
  - **Learnt how to Embed the Bokeh Chart in a Webpage.**
  - **Learnt to Deploy the Chart Website to a Live Server.**
- 
- **Below shown are the some pictures of graph produced, which are the stocks of Google from 01 Jan 2020 to 30 May 2020 and plotted using Candlestick format.**

