**DAILY ASSESSMENT FORMAT**

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| **Date:** | **02-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **Digital Design using HDL** | **USN:** | **4AL17EC035** |
| **Topic:** | **1.FPGA Basics: Architecture, Applications and Uses**  **2.Verilog HDL Basics by Intel**  **3.Verilog Testbench code to verify the design under test (DUT).** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.** |

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| **Date:** | **02-06-2020** | **Name:** | **HEMALATHA SANIL** |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC035** |
| **Topic:** | **Section 28 and Section 29** | **Semester & Section:** | **6 SEM & ‘A’ SEC** |
| **Github Repository:** | **Hemalatha-Sanil** |  |  |

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| **AFTERNOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**      **INTERACTIVE DATA VISUALIZATION WITH BOKEH**  **1.Basic Graph**      **2.Basic\_Pandas\_Graph**    **3.Triangle Graph**      **4.Circle Graph**      **5.Bachelor’s Graph**      **6.Weather Graph**          **WEBSCRAPING EXAMPLE** |

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