

# DAILY ASSESSMENT FORMAT

Date:	02-06-2020	Name:	Jagadeesha Hegde
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC036
Topic:	FPGA Basics: Architecture, Applications and Uses  Verilog HDL Basics by Intel Verilog Test bench code to verify the design under test (DUT)	Semester & Section:	6th A-sec
Github Repository:	Jagadeesha-036		

## FORENOON SESSION DETAILS

### Image of session

### Connecting Module Instantiation Ports

- **Two methods to define port connections**
  - By ordered list
  - By name
- **By ordered list (1<sup>st</sup> half adder\*)**
  - Port connections defined by the order of the port list in the lower-level module declaration
    - `module half_adder (co, sum, a, b);`
  - Order of the port connections *does* matter
    - `co -> c1, sum -> s1, a -> a, b -> b`
- **By name (2<sup>nd</sup> half\_adder\*)**
  - Port connections defined by name
  - Recommended method
  - Order of the port connections *does not* matter
    - `a -> s1, b -> cin, sum -> fsum, co -> c2`

```

module full_adder (
  output fco, fsum,
  input cin, a, b
);
  wire c1, s1, c2;

  half_adder u1 (c1, s1, a, b);
  half_adder u2 (.a(s1), .b(cin),
    .sum(fsum), .co(c2));
  or u3(fco, c1, c2);

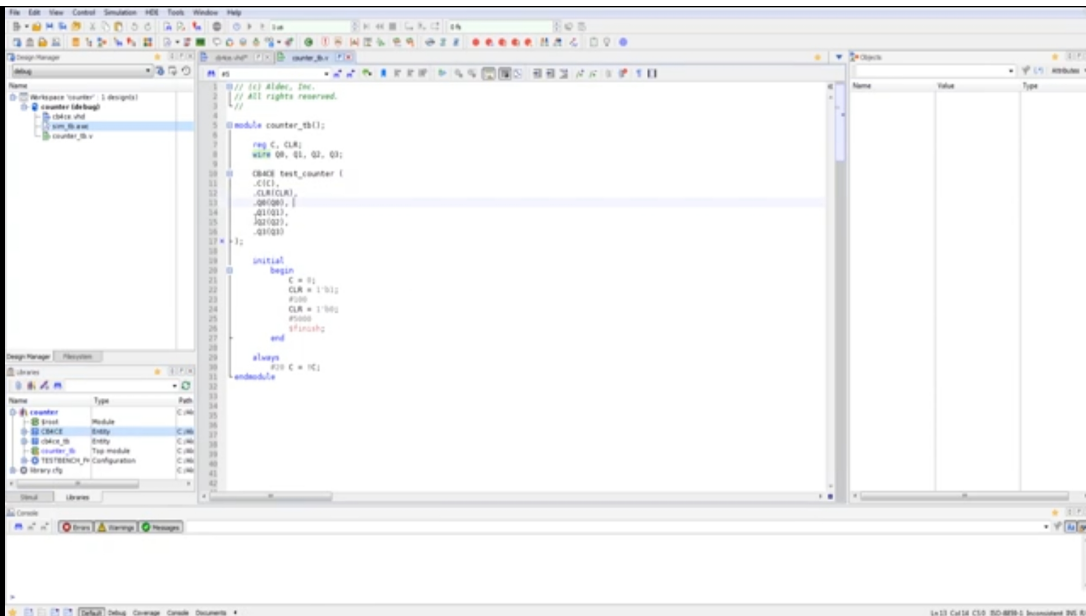
endmodule
                
```

**half\_adder** u1 (c1, s1, a, b);  
**half\_adder** u2 (.a(s1), .b(cin),  
 .sum(fsum), .co(c2));  
**or** u3(fco, c1, c2);

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MEASURABLE ADVANTAGE™



Report – Report can be typed or hand written for up to two pages.

**FPGA Basics: Architecture, Applications and Uses Verilog HDL Basics by intel Verilog Test bench code to verify the design under test (DUT).**

Specific application of an FPGA includes digital signal processing, bioinformatics, device controllers, software-defined radio, random logic, ASIC prototyping, medical imaging, computer hardware emulation, integrating multiple SPLDs, voice recognition, cryptography, filtering and communication encoding and many

more.

FPGAs are particularly useful for prototyping application-specific integrated circuits (ASICs) or processors. An FPGA can be reprogrammed until the ASIC or processor design is final and bug-free and the actual manufacturing of the final ASIC begins. Intel itself uses FPGAs to prototype new chips.

The FPGA is Field Programmable Gate Array. It is a type of device that is widely used in electronic circuits. FPGAs are semiconductor devices which contain programmable logic blocks and interconnection circuits. It can be programmed or reprogrammed to the required functionality after manufacturing.

The Device Under Test (D.U.T.) In this example, the DUT is behavioral Verilog code for a 4-bit counter found in Appendix A. This is also known as a Register Transfer Level or RTL description of the design. In the HDL source, all the input and output signals are declared in the port list.

Code for multiplexing

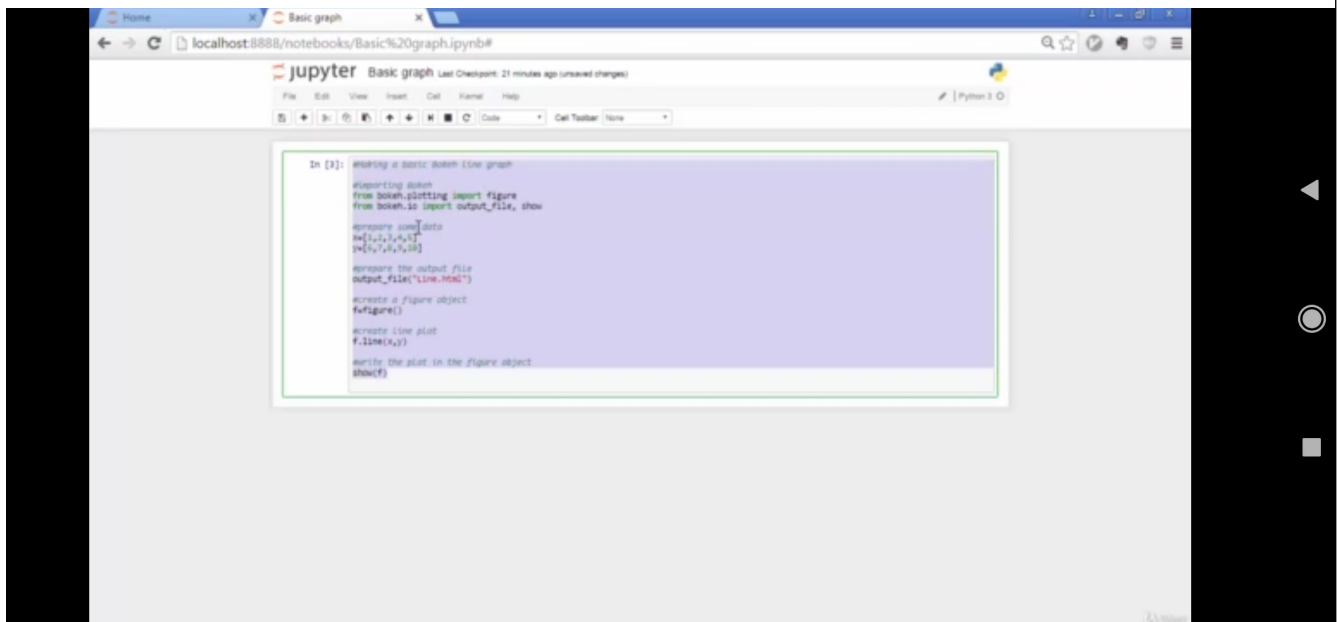
```
module mux_4to1_case ( input [3:0] a,           // 4-bit input
                      called a input [3:0] b,
                      input [3:0] c,
                      input [3:0] d,
                      input [1:0] sel,
                      between a, b, c, d output reg [3:0] out);
    always @ (a or b or c or d or sel) begin
        case (sel)
            2'b00 : out <= a;
            2'b01 : out <= b;
            2'b10 : out <= c;
            2'b11 : out <= d;
```

end case  
end  
endmodule

Date:	02-06-2020	Name:	Jagadeesha Hegde
Course:	The Python Mega Course	USN:	4AL17EC036
Topic:	Interactive Data Visualization with Bokeh	Semester & Section:	6th A-sec
	Webscraping with Python		
	Beautiful Soup		

## AFTERNOON SESSION DETAILS

### Image of session



```
D:\Dropbox\ppp\Section1_get_started\Demo\data.csv - Notepad++
File Edit Search View Encoding Language Settings Macro Run Plugins Window ?

5 cur=conn.cursor()
6 cur.execute("CREATE TABLE IF NOT EXISTS book (id INTEGER
PRIMARY KEY, title text, author text, year integer, isbn
integer)")
7 conn.commit()
8 conn.close()
9
10 def insert(title,author,year,isbn):
11     conn=sqlite3.connect("books.db")
12     cur=conn.cursor()
13     cur.execute("INSERT INTO book VALUES (NULL,?, ?, ?, ?)",(title,
author,year,isbn))
14     conn.commit()
15     conn.close()
16
17 def view():
18     conn=sqlite3.connect("books.db")
19     cur=conn.cursor()
20     cur.execute("SELECT * FROM book")
21     rows=cur.fetchall()
22     conn.close()
23     return rows
24
25 def search(title="",author="",year="",isbn=""):
26     conn=sqlite3.connect("books.db")
27     cur=conn.cursor()
28     cur.execute("SELECT * FROM book WHERE title=? OR author=? OR
year=? OR isbn=?", (title,author,year,isbn))
29     rows=cur.fetchall()
30     conn.close()
31     return rows
32
33 def delete(id):
34     conn=sqlite3.connect("books.db")
35     cur=conn.cursor()

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```

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## **SCRAPING WITH PYTHON BEAUTIFUL SOUP**

**The incredible amount of data on the internet is a rich resource of any field id research or personal internet.**

**To effectively harvest the data , you ll need to become skilled at web scraping .**

**The python libraries requests and beautiful soul are powerful tools for job.if you like to learn with hands on examples and you have a basic understanding of python and HTML.**

## **INTERACRIVE DATA VISUALIZATION WITH BOKEH**

**Bokeh prides itself on being a library for interactive data visualization.**

**Unlike popular counterparts in the python visualization space, like matplotlib and seaborn, bokeh renders its graphics using HTML and java scripts.**

