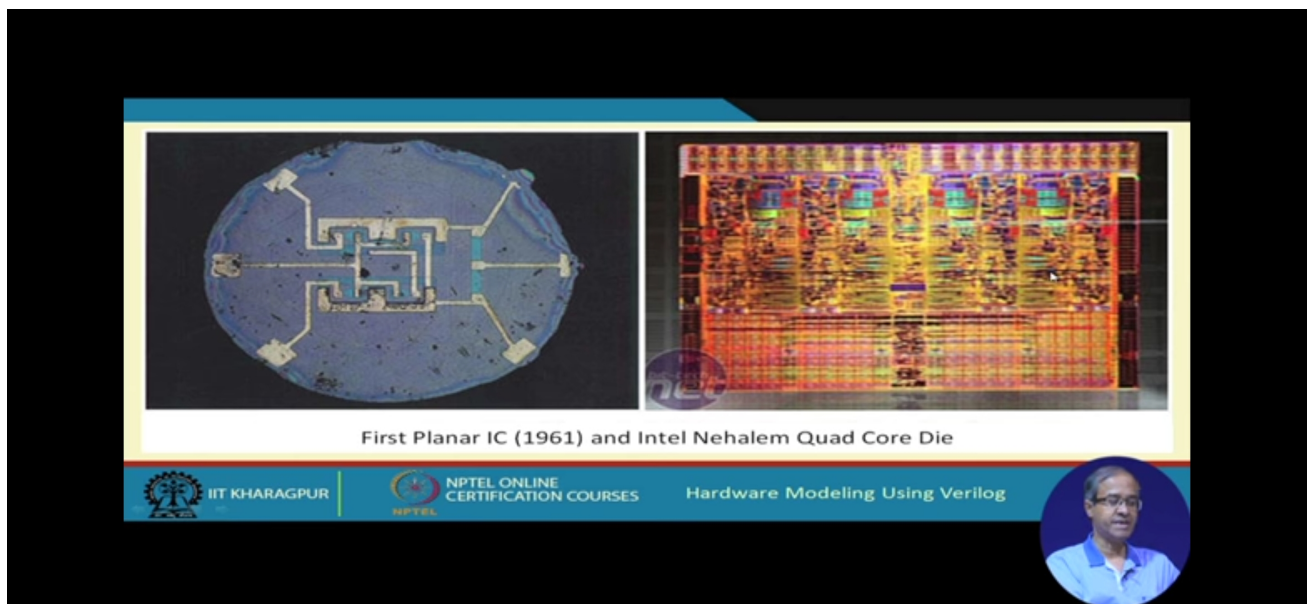


## DAILY ASSESSMENT FORMAT

Date:	04-06-2020	Name:	Jagadeesha Hegde
Course:	Logic Design	USN:	4AL17EC036
Topic:	Hardware modelling using Verilog  FPGA and ASIC Interview questions	Semester & Section:	6th A-sec
Github Repository:	Jagadeesha-036		

### FORENOON SESSION DETAILS

Image of session



## Steps in the Design Flow

- Behavioral design
  - Specify the functionality of the design in terms of its *behavior*.
  - Various ways of specifying:
    - Boolean expression or truth table.
    - Finite-state machine behavior (e.g. state transition diagram or table).
    - In the form of a high-level algorithm.
  - Needs to be synthesized into more detailed specifications for hardware realization.



IIT KHARAGPUR



NPTEL ONLINE  
CERTIFICATION COURSES

Hardware Modeling Using Verilog



Report – Report can be typed or hand written for up to two pages.

## VLSI DESIGN PROCESS

1. Design complexity increasing rapidly
2. CAD tools are essential
3. The present trends
  - Standardize the design flow
  - Emphasis on low power design and increased performance

## MOORES LAW

- Exponential growth
- DESIGN complexity increase rapidly

- Automated tools are essential
- Must follow well defined design flow

## **VLSI DESIGN FLOW**

- Standardize design procedure
  - Emphasis many steps
1. Specifications
  2. Synthesis
  3. Simulation
  4. Layout
  5. Testability analysis
- Need to use computer aided design (CAD) Tool

## **TWO COMPLEXITY HDLS**

- VERILOG
- Vhdl

## **Steps in design flow**

- Design idea
- Behavioural design
- Data path design
- Logic design
- Physical design
- Manufacturing
- Chip /board

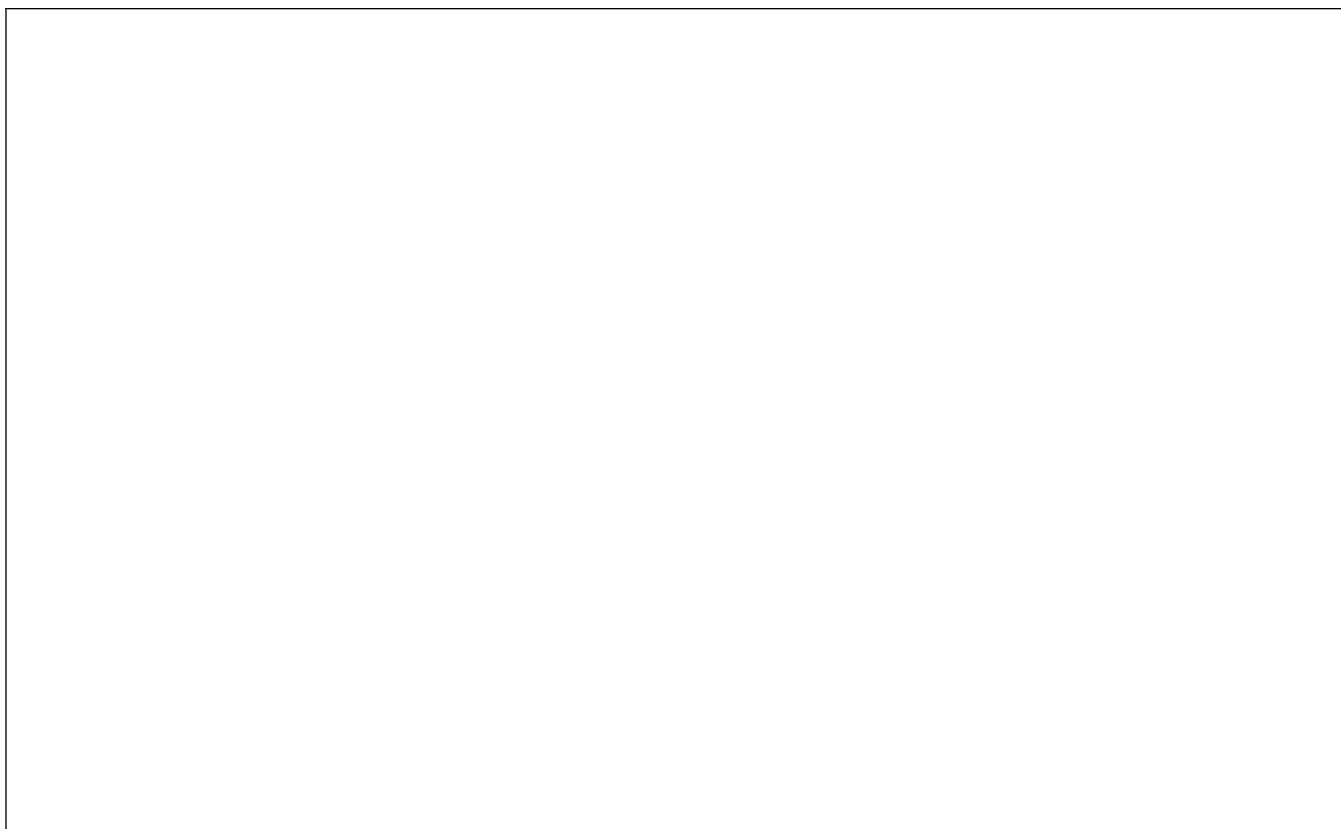
## OTHER STPES IN DESIGN FLOW

- Simulation for verification
- Formal verification
- Testability analysis and test pattern generation

## IMPLEMENT A SIMPLE T FLIPFLOP AND TEST THE MODULE USING A COMPILER

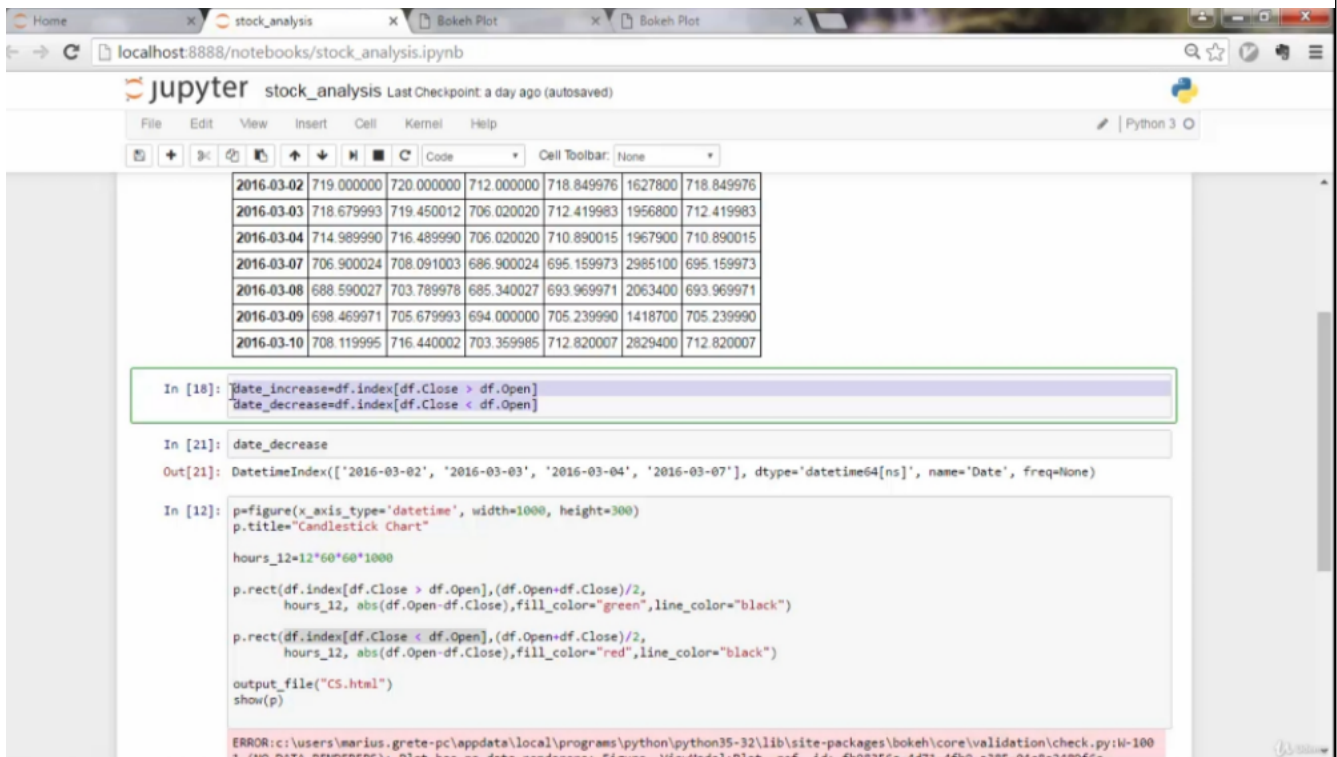
Code:

```
module tff ( input clk, input rstn, input t,
            output reg q);
always @ (posedge clk) begin
if (!rstn)
    q <= 0;
else
    if (t)
        q <= ~q;
    else
        q <= q;
end
endmodule
```



<b>Date:</b>	<b>04-06-2020</b>	<b>Name:</b>	<b>Jagadeesha Hegde</b>
<b>Course:</b>	<b>The Python Mega Course</b>	<b>USN:</b>	<b>4AL17EC036</b>
<b>Topic:</b>	<b>Application 9: Build a Web-based financial Graph</b>	<b>Semester &amp; Section:</b>	<b>6th A-sec</b>

AFTERNOON SESSION DETAILS
Image of session



Report – Report can be typed or hand written for up to two pages.

## CREATION OF BASIC ENCRYPTION APP

- Practice over loop together
- Create where there are a communication on watusp or let's say telegram or whatever app what's happening in that those communication are encrypted
- Decided to create a encryptic engine to be able to criple let's say conversation

```
def crypted(sentence):  
translation = ""  
for element in sentence:  
    if element in "Aa":  
        translation=translation+"1"  
    elif element in "Bb":  
        translation = translation + "2"  
    elif element in "Cc":  
        translation = translation + "3"  
    elif element in "Dd":  
        translation = translation + "4"  
    elif element in "Ee":  
        translation = translation + "5"  
    elif element in "Ff":  
        translation =translation + "6"
```

**elif element in "Gg":**

**translation = translation + "7"**

**elif element in "Hh":**

**translation = translation + "8"**

**elif element in "Ii":**

**translation = translation + "9"**

**elif element in "Jj":**

**translation = translation + "!"**

**else :**

**translation = translation + element**

**restore translation '**