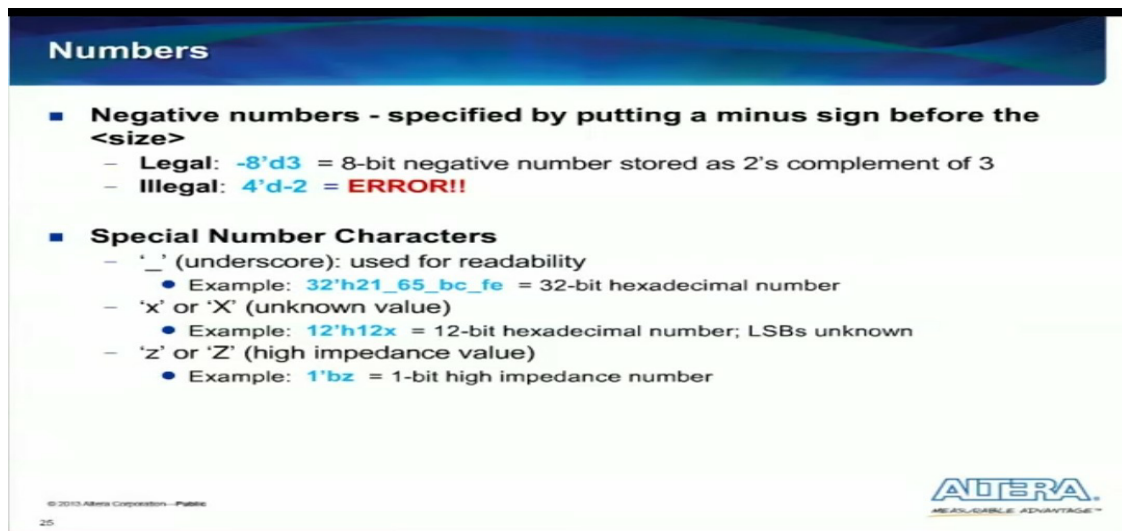


# DAILY ASSESSMENT FORMAT

Date:	02-06-2020	Name:	K Muthu
Course:	DIGITAL DESIGN USING HDL	USN:	4a17ec038
Topic:	<ul style="list-style-type: none"> <li>FPGA Basics: Architecture, Applications and UsesFPGA Business Fundamentals</li> <li>Verilog HDL Basics by Intel</li> <li>Task</li> </ul>	Semester & Section:	6 & 'A'
Github Repository:	K.Muthu-courses		

## FORENOON SESSION DETAILS

### Image of session



### Verilog HDL Basics

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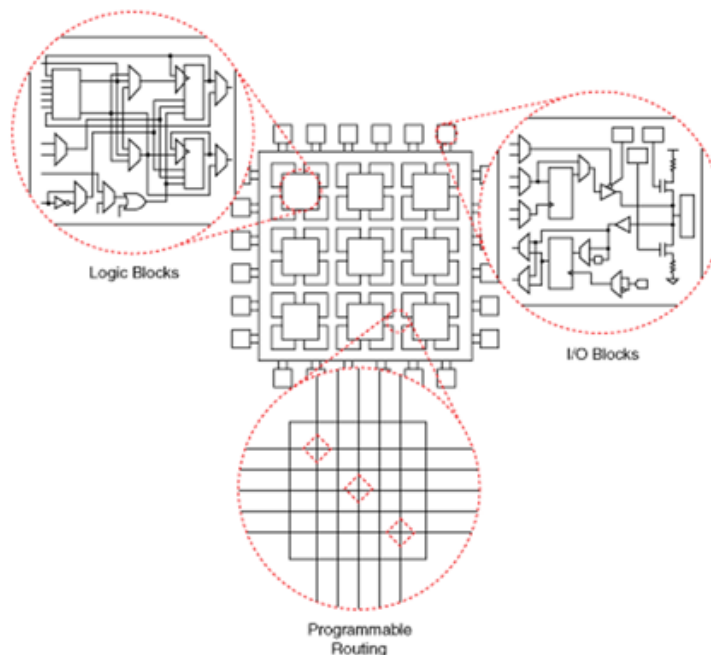
**Report – Report can be typed or hand written for up to two pag**

### **FPGA Basics: Architecture, Applications and Uses :**

The FPGA is an integrated circuit that consists of internal hardware blocks with user-programmable interconnects to customize operation for a specific application.

- **Architecture :**

A basic FPGA architecture consists of thousands of fundamental elements called configurable logic blocks (CLBs) surrounded by a system of programmable interconnects, called a fabric, that routes signals between CLBs.



- **Application :**

- ✓ Broadcast
- ✓ Consumer
- ✓ Embedded Vision
- ✓ Medical
- ✓ Military / Aerospace / Government
- ✓ Wireless & Wireline

- **Uses :**

- ✓ Microsoft is using FPGAs in its data centers to run Bing search algorithms.
- ✓ The FPGA can change to support new algorithms as they are created.
- ✓ If needs change, the design can be repurposed to run simulation or modeling routines in an HPC application.
- ✓ This flexibility is difficult or impossible to achieve with an ASIC.

### Verilog HDL Basics by Intel :

- Verilog is a HARDWARE DESCRIPTION LANGUAGE (HDL).
- It is a language used for describing a digital system like a network switch or a microprocessor or a memory or a flip-flop.
- It means, by using a HDL we can describe any digital hardware at any level.
- Verilog supports a design at many levels of abstraction. The major three are –
  - ✓ Behavioral level
  - ✓ Register-transfer level
  - ✓ Gate level
- **Behavioral level** - This level describes a system by concurrent algorithms (Behavioural). Every algorithm is sequential, which means it consists of a set of instructions that are executed one by one. Functions, tasks and blocks are the main elements. There is no regard to the structural realization of the design.
- **Register-Transfer Level** - Designs using the Register-Transfer Level specify the characteristics of a circuit using operations and the transfer of data between the registers. Modern definition of an RTL code is "Any code that is synthesizable is called RTL code".
- **Gate Level** - Within the logical level, the characteristics of a system are described by logical links and their timing properties. All signals are discrete signals. They can only have definite logical values (`0', `1', `X', `Z'). The usable operations are predefined logic primitives (basic gates).

**Task : Implement a 4:1 MUX and write the test bench code to verify the module**

**Verilog code :**

```
module mux4_1(a, s, o);  
    input [3:0] a;  
    input [1:0] s;  
    output reg o;  
    always @(a or s)  
    begin  
        case (s)  
            2'b00:o=a[0];  
            2'b01:o=a[1];  
            2'b10:o=a[2];  
            2'b11:o=a[3];  
            default:o=0;  
        endcase  
    end  
endmodule
```

**Testbench code :**

```
module muxt_b;  
    reg [3:0] a;  
    reg [1:0] s;  
    wire o;  
    mux4bit uut (.a(a), .s(s),.o(o));  
    initial begin  
        #10 a=4'b1010;
```

```
#10 s=2'b00;
```

```
#10 s=2'b01;
```

```
#10 s=2'b10;
```

```
#10 s=2'b11;
```

```
#10 $stop;
```

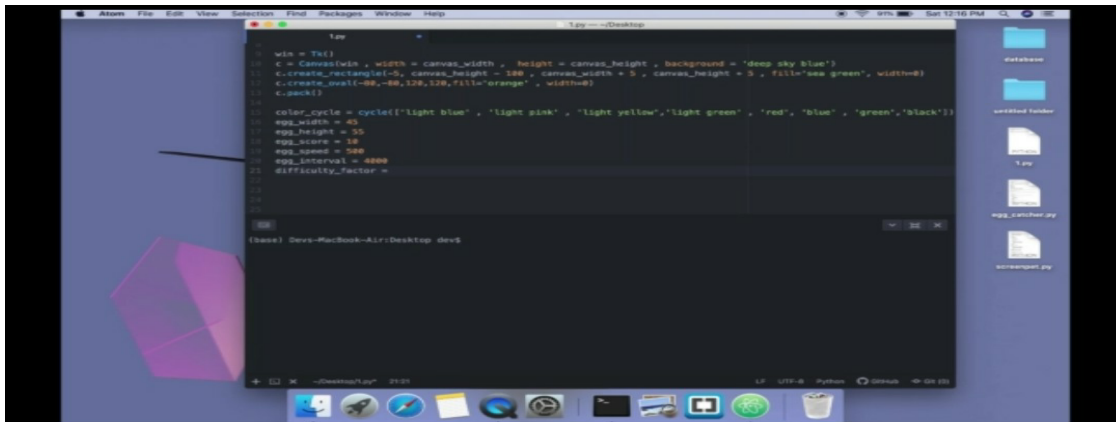
```
end
```

```
endmodule
```


Date:	02-06-2020	Name:	K Muthu
Course:	Python Bootcamp 2020 build 15 working applications and Games	USN:	4a17ec038
Topic:	Egg catcher game	Semester & Section:	6 & 'A'

### AFTERNOON SESSION DETAILS

#### Image of session



Lectures

More



#### Section 39 - Project-13 Egg catcher game



- 366 Introduction to this module  
 Video - 00:44 mins
- 367 Overview of the project  
 Video - 01:45 mins
- 368 Creating window  
 Video - 07:53 mins
- 369 Egg and catcher



**Report – Report can be typed or hand written for up to two pages.**

### **Egg catcher game :**

- A Egg catcher game is programmed using Tkinter module package of python library.
- Tkinter is the standard GUI library for Python.
- Python when combined with Tkinter provides a fast and easy way to create GUI applications.
- Tkinter provides a powerful object-oriented interface to the Tk GUI toolkit.
- Creating a GUI application using Tkinter is an easy task.
- Steps involved in creating the egg catcher game are,
  - ✓ Import the Tkinter module.
  - ✓ Create the GUI application main window.
  - ✓ Add the required widgets to the GUI application.
  - ✓ Enter the main event loop to take action against each event triggered by the user.

