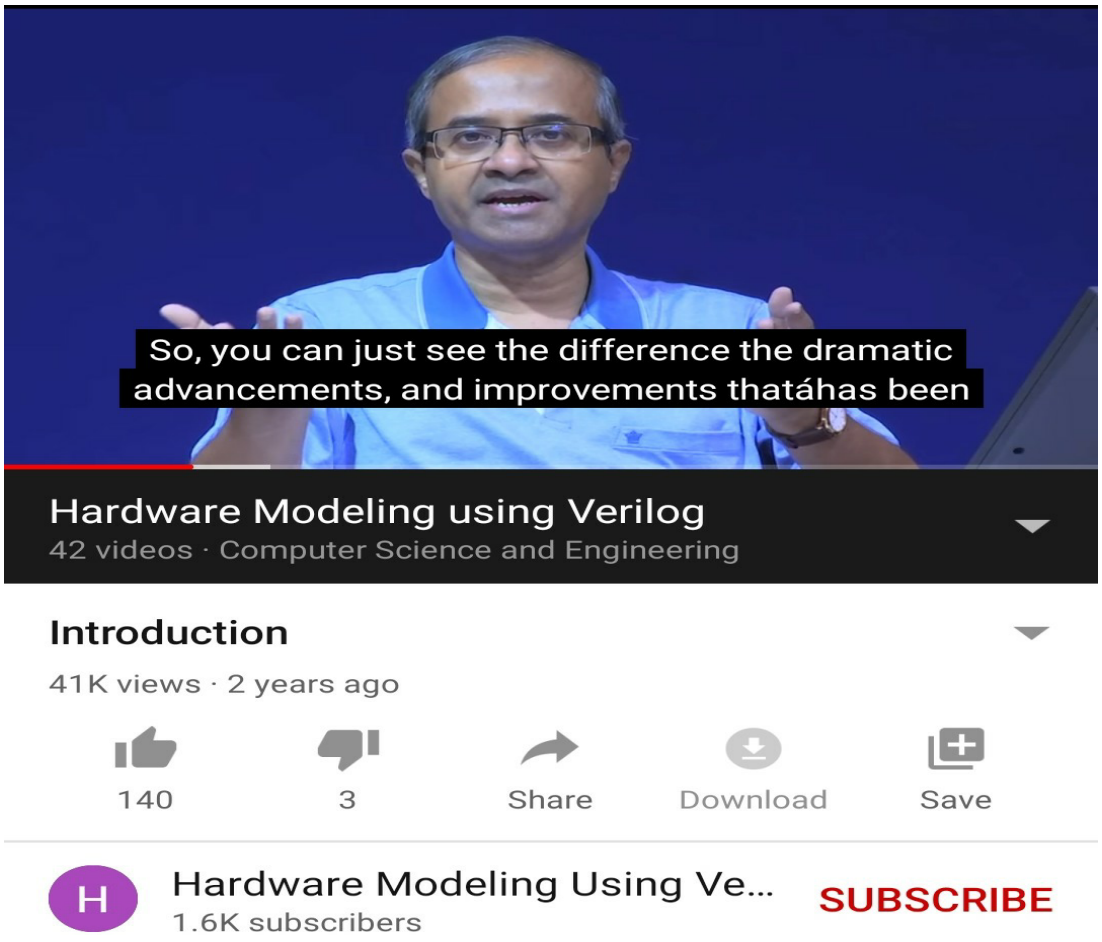
DAILY ASSESSMENT FORMAT

Date:	**04-06-2020**	**Name:**	**K Muthu**
Course:	**DIGITAL DESIGN USING HDL**	**USN:**	**4al17ec038**
Topic:	• Hardware modelling using verilog • FPGA and ASIC Interview questions • Task	**Semester & Section:**	**6 & 'A'**
Github Repository:	**K.Muthu-courses**		

FORENOON SESSION DETAILS

Image of session



Report –

Hardware modelling using verilog :

The outcome of the session are,

- ✓ Learnt about the verilog hardware description language.
- ✓ Understand the difference between behavioural and structural modelling styles.
- ✓ Learnt to write test benches and analyse simulation results.
- ✓ Learnt to model combinational logic circuits.
- ✓ Distinguish between good and bad coding practices.
- ✓ Case studies with some complex designs.

FPGA and ASIC Interview questions :

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1) Write a verilog code to swap contents of two registers with and without a temporary register?

With temp reg ;

```
always @ (posedge clock)
begin
temp=b;
b=a;
a=temp;
end
```

Without temp reg;

```
always @ (posedge clock)
begin
a <= b;
b <= a;
end
```

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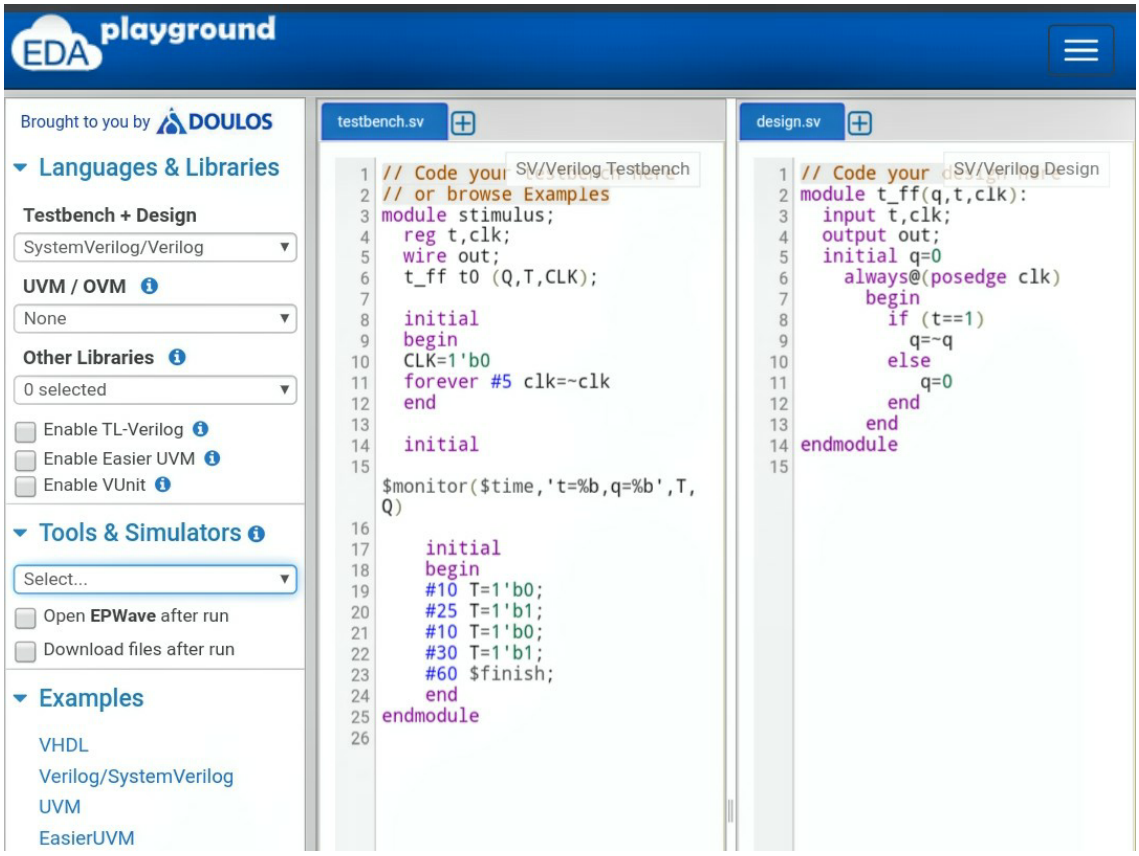
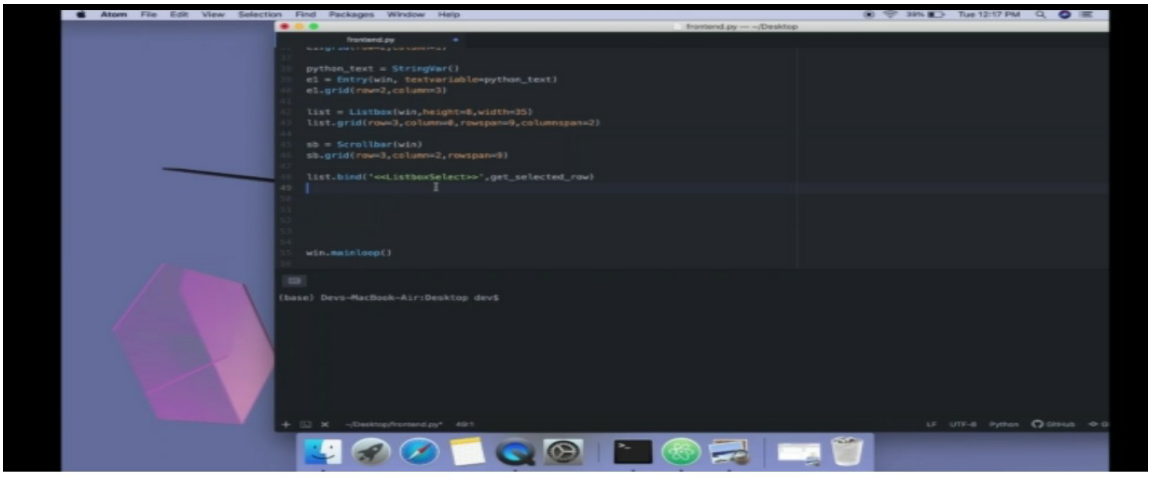
Task : Implement a simple T Flipflop and test the module using a compiler.

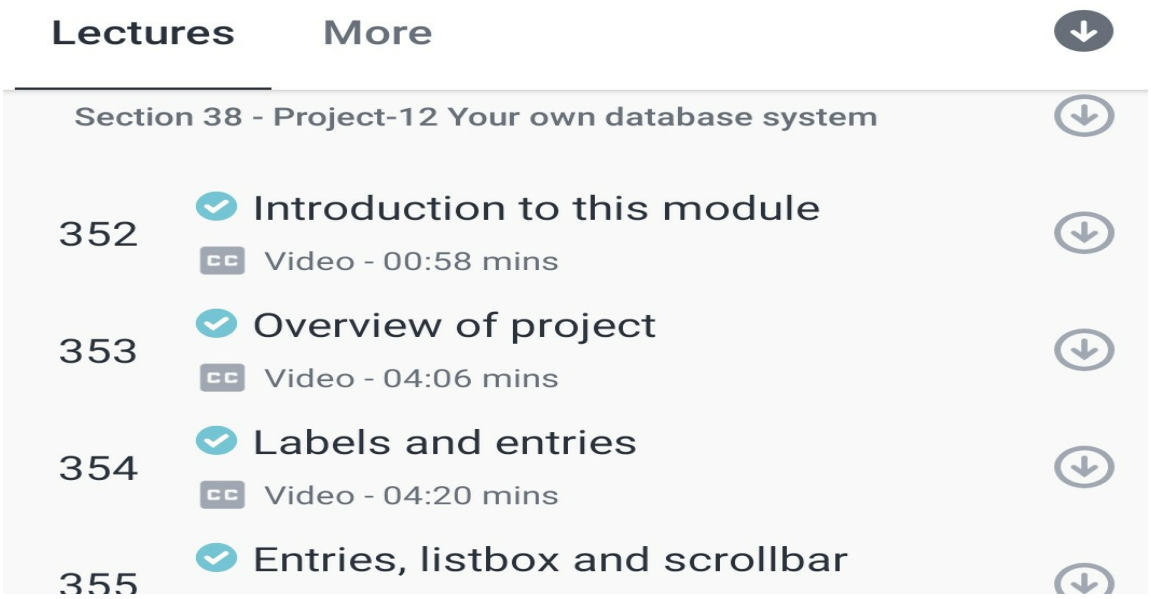


Date:	**04-06-2020**	**Name:**	**K Muthu**
Course:	**Python Bootcamp 2020 build 15 working applications and Games**	**USN:**	**4al17ec038**
Topic:	Own database	**Semester & Section:**	**6 & 'A'**

AFTERNOON SESSION DETAILS

Image of session





Report –

Own database :

- A database is an abstraction over an operating system's file system that makes it easier for developers to build applications that create, read, update and delete persistent data.
- are a concept with many implementations, including PostgreSQL, MySQL and SQLite.
- and MySQL are two of the most common open source databases for storing Python web applications' data.