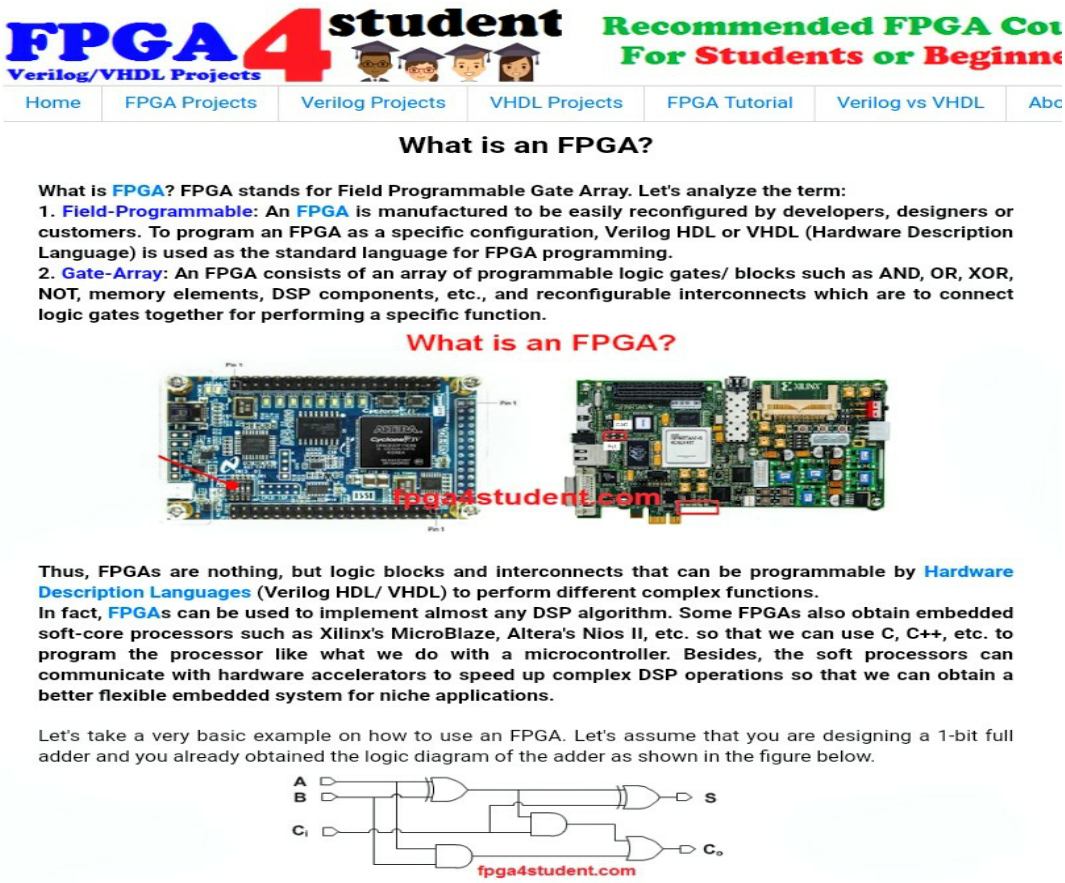
DAILY ASSESSMENT FORMAT

Date:	05-06-2020	**Name:**	K Muthu
Course:	DIGITAL DESIGN USING HDL	**USN:**	4al17ec038
Topic:	• Verilog Tutorials and practice programs • Building/ Demo projects using FPGA • Task	**Semester & Section:**	6 & 'A'
Github Repository:	K.Muthu-courses		

FORENOON SESSION DETAILS

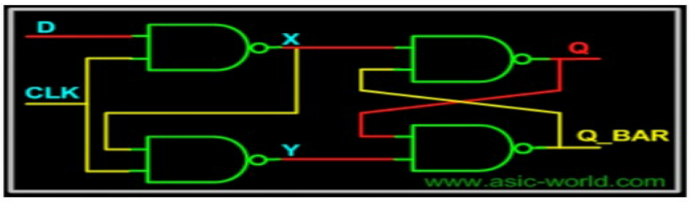
Image of session



Report –

Verilog Tutorials and practice programs :

D–Flip flop from NAND Gate



Verilog Code

```
module dff_from_nand();
wire Q,Q_BAR;
reg D,CLK;

nand U1 (X,D,CLK) ;
nand U2 (Y,X,CLK) ;
nand U3 (Q,Q_BAR,X);
nand U4 (Q_BAR,Q,Y);

// Testbench of above code
initial begin
   $monitor( "CLK = %b D = %b Q = %b Q_BAR = %b" ,CLK, D, Q, Q_BAR);
   CLK = 0;
   D = 0;
   #3 D = 1;
   #3 D = 0;
   #3 $finish;
end

always #2 CLK = ~CLK;

endmodule
```

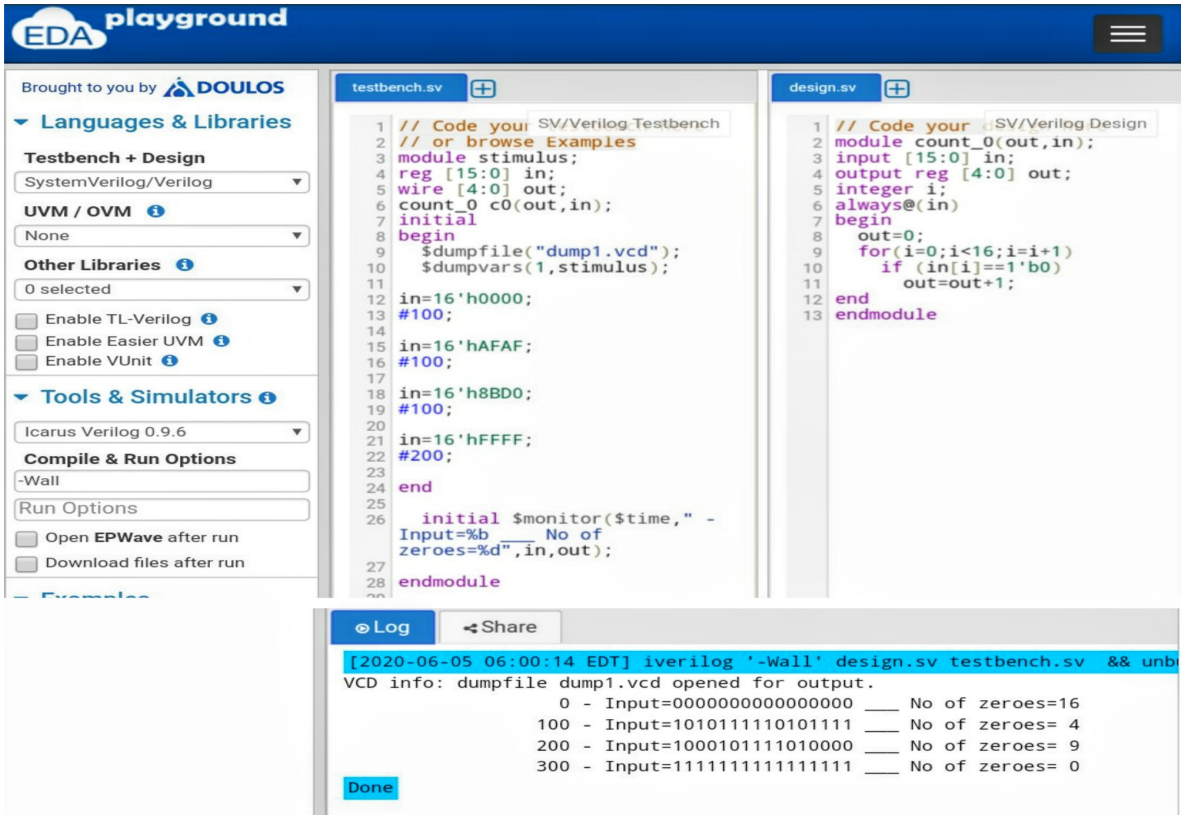
Building/ Demo projects using FPGA :

Some of the FPGA projects can be FPGA tutorials such as What is FPGA Programming, image proc on FPGA, matrix multiplication on FPGA Xilinx using Core Generator, Verilog vs VHDL: Expl Examples and how to load text files or images into FPGA. Many others FPGA projects provide st with full Verilog/ VHDL source code to practice and run on FPGA boards. Some of them can be us another bigger FPGA projects.
Following are the FPGA projects on fpga4student.com:

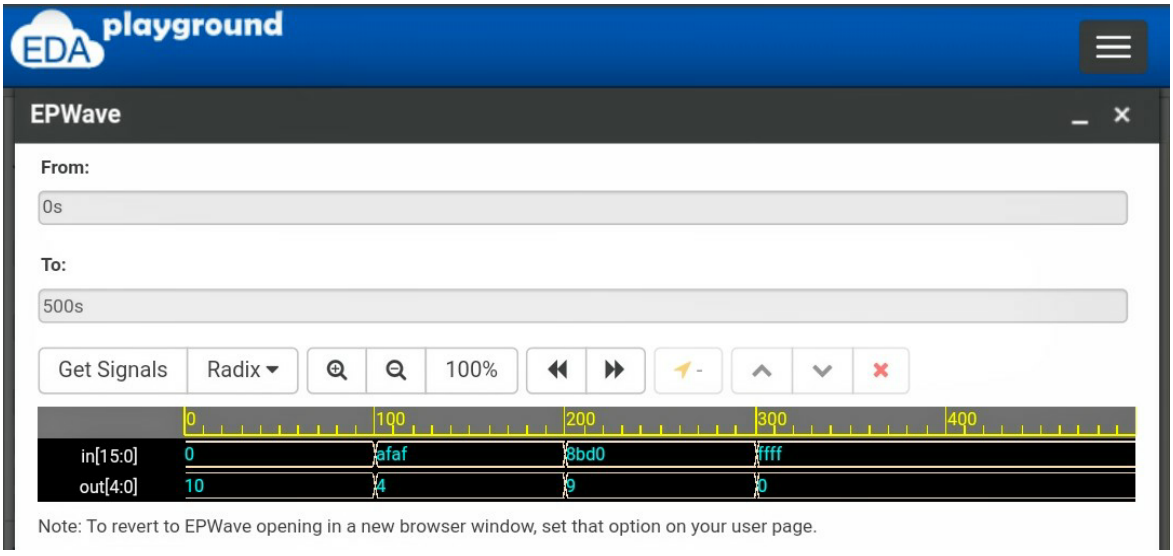
1. What is an FPGA? How does FPGA work?
2. Basys 3 FPGA OV7670 Camera
3. How to load text file or image into FPGA
4. Image processing on FPGA using Verilog
5. License Plate Recognition on FPGA
6. Alarm Clock on FPGA using Verilog
7. Digital Clock on FPGA using VHDL
8. Simple Verilog code for debouncing buttons on FPGA
9. Traffic Light Controller on FPGA
10. Car Parking System on FPGA in Verilog
11. VHDL code for comparator on FPGA
12. Verilog code for Multiplier on FPGA
13. N-bit Ring Counter in VHDL on FPGA
14. Verilog implementation of Microcontroller on FPGA
15. Verilog Carry Look Ahead Multiplier on FPGA
16. VHDL Matrix Multiplication on FPGA Xilinx
17. Fixed Point Matrix Multiplication on FPGA using Verilog
18. Verilog Divider on FPGA
19. VHDL code for Microcontroller on FPGA
20. VHDL code for FIR Filter on FPGA
21. Verilog code for Digital logic components on FPGA
22. Delay Timer Implementation on FPGA using Verilog
23. Single-Cycle MIPS processor on FPGA using Verilog
24. FIFO Verilog Implementation on FPGA
25. FIFO VHDL Implementation on FPGA
26. Verilog D Flip Flop on FPGA
27. Comparator Design on FPGA using Verilog
28. D Flip Flop on FPGA using VHDL
29. Full Adder Design on FPGA using Verilog
30. Full Adder Design on FPGA using VHDL

Task : Implement a verilog module to count number of 0's in a 16 bit number in compiler.

- **Verilog code :**



- **Output :**

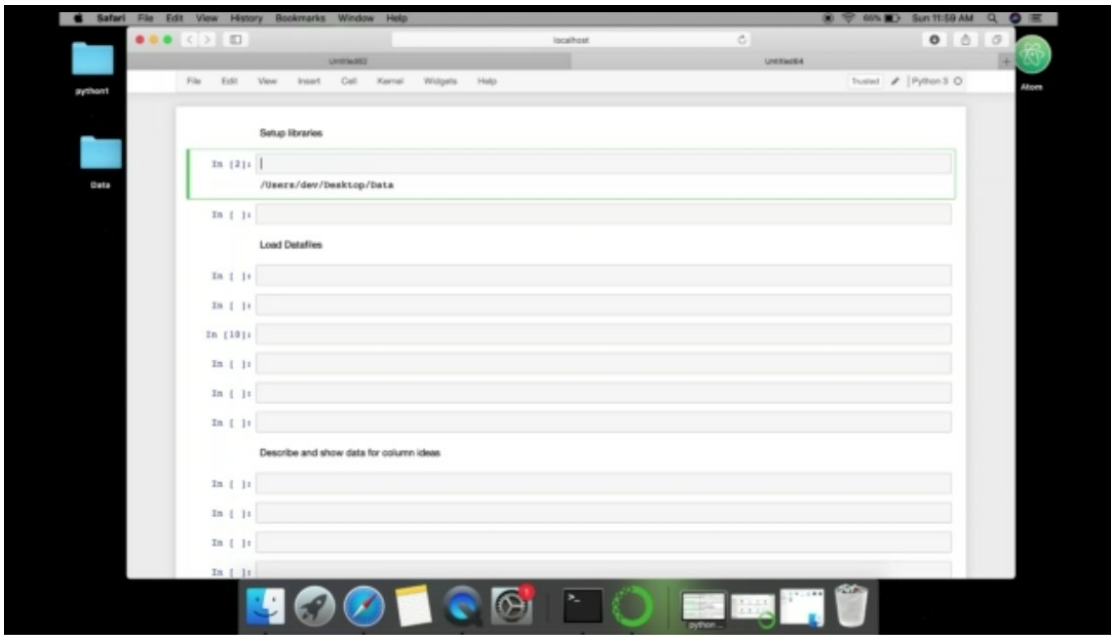


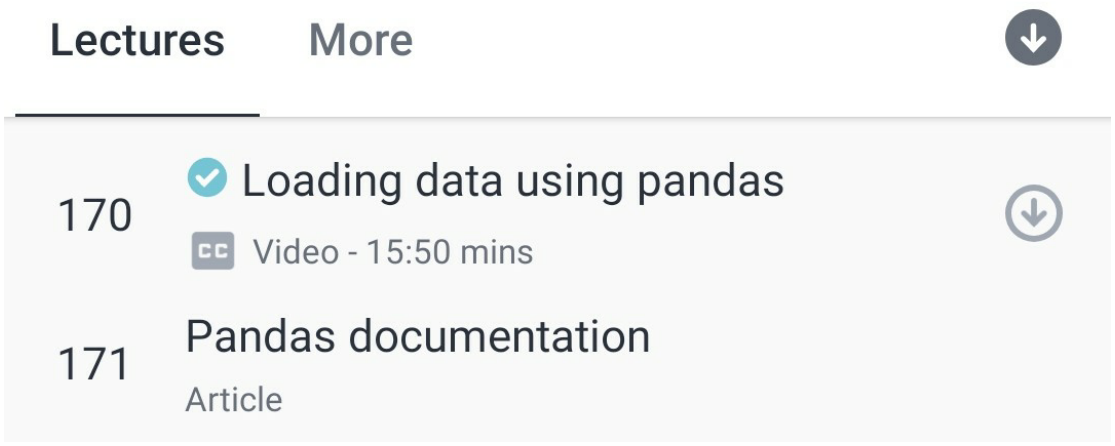
Note : The values displayed in EPWave output are in hexadecimal base.

Date:	**05-06-2020**	**Name:**	**K Muthu**
Course:	**Python Bootcamp 2020 build 15 working applications and Games**	**USN:**	**4al17ec038**
Topic:	Data Cleaning	**Semester & Section:**	**6 & 'A'**

AFTERNOON SESSION DETAILS

Image of session





Report –

Data Cleaning :

- Data cleaning is the process of preparing data for analysis by removing or modifying data that is incorrect, incomplete, irrelevant, duplicated, or improperly formatted.
- This data is usually not necessary or helpful when it comes to analyzing data because it may hinder the process or provide inaccurate results.
- There are several methods for cleaning data depending on how it is stored along with the answers being sought.
- Data cleaning is a vital step to ensure that the answers you generate are accurate.
- Steps that are performed in data cleaning are,
  - ✓ Load the dataset
  - ✓ Identify the number of NULL values in the dataset
  - ✓ Modify the dataset by converting the NULL values into maximum occured element of that perticular column.
  - ✓ Repeat the process until all the NULL values are modified