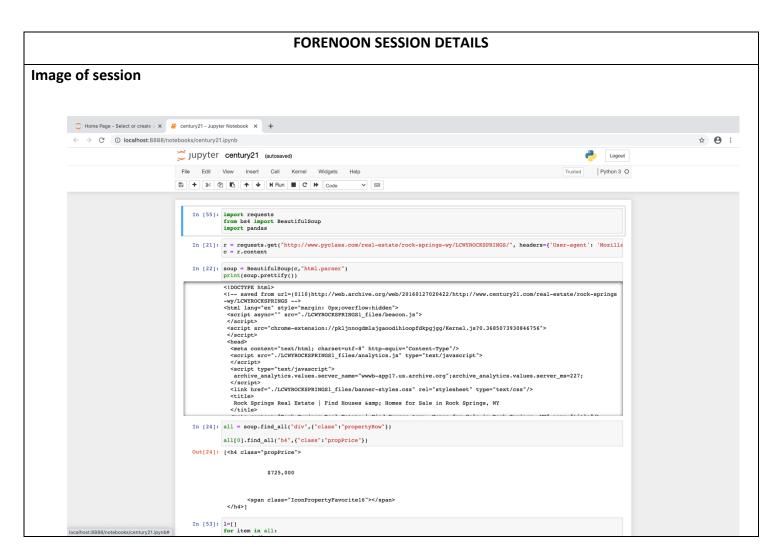
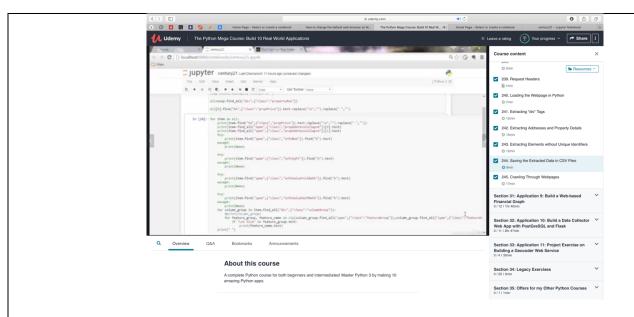
## **DAILY ASSESSMENT FORMAT**

Date:	03/06/2020	Name:	K B KUSHI
Course:	Python	USN:	4AL17EC107
Topic:	Application 7: Scrape Real     Estate Property Data from     the Web	Semester & Section:	6 B
Github Repository:	https://github.com/alvas- education-foundation/KUSHI- COURSES.git		





#### Report:

In this section we were taught how to scrap data from a real estate website.

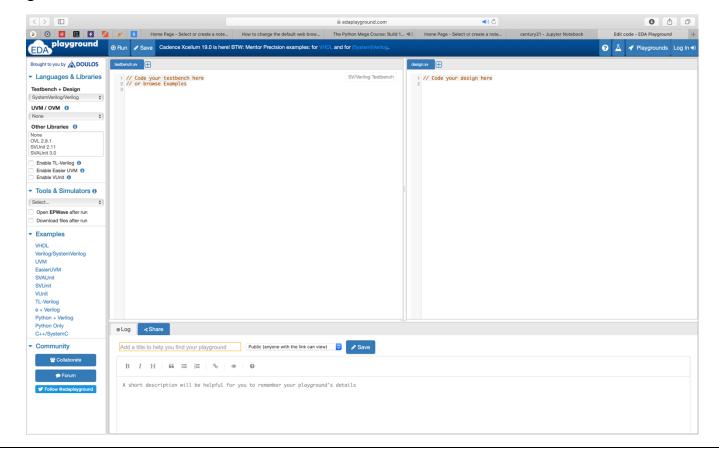
#### Python for Web Scraping?

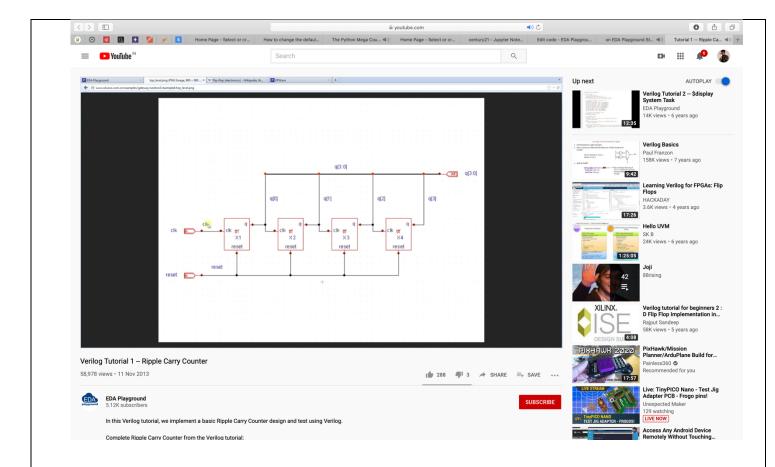
- Ease of Use: Python is simple to code. You do not have to add semi-colons ";" or curly-braces "{}" anywhere. This makes it less messy and easy to use.
- Large Collection of Libraries: Python has a huge collection of libraries such
  as <u>Numpy</u>, <u>Matlplotlib</u>, <u>Pandas</u> etc., which provides methods and services for various purposes.
  Hence, it is suitable for web scraping and for further manipulation of extracted data.
- Dynamically typed: In Python, you don't have to define datatypes for variables, you can directly use the variables wherever required. This saves time and makes your job faster.
- Easily Understandable Syntax: Python syntax is easily understandable mainly because reading a
  Python code is very similar to reading a statement in English. It is expressive and easily readable, and
  the indentation used in Python also helps the user to differentiate between different scope/blocks in
  the code.
- Small code, large task: Web scraping is used to save time. But what's the use if you spend more time writing the code? Well, you don't have to. In Python, you can write small codes to do large tasks. Hence, you save time even while writing the code.
- Community: What if you get stuck while writing the code? You don't have to worry. Python community has one of the biggest and most active communities, where you can seek help from.

Date:	03/06/2020	Name:	K B KUSHI
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC107
Topic:	<ol> <li>EDA Playground Online complier</li> <li>EDA Playground Tutorial Demo Video</li> <li>How to Download And Install Xilinx Vivado Design Suite</li> <li>Vivado Design Suite for</li> </ol>	Semester & Section:	6 B
Github Repository:	implementation of HDL code https://github.com/alvas- education-foundation/KUSHI- COURSES.git		

## **AFTERNOON SESSION DETAILS**

# Image of session





Report – Report can be typed or hand written for up to two pages.

- In today's session we noted how to use a EDA Playground Online complier
- EDA Playground Tutorial Demo Video helped us in getting familiarized with the tool.
- How to Download And Install Xilinx Vivado Design Suite and Vivado Design Suite for implementation
  of HDL code video taught us how to download and use the Xilinx to implement Verilog code.

Implement 4 to 1 MUX using two 2 to 1 MUX using structural modelling style and test the module in online/offline compiler.

## Code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux2_1 is
```

port(A,B: in STD\_LOGIC;

S: in STD\_LOGIC;

Z: out STD\_LOGIC);

```
end mux2_1;
architecture Behavioral of mux2_1 is
begin
process (A,B,S) is
begin
if (S ='0') then
Z <= A;
else
Z <= B;
end if;
end process;
end Behavioral;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux4_1 is
port(
A,B,C,D: in STD_LOGIC;
S0,S1: in STD_LOGIC;
Z: out STD_LOGIC
);
end mux4_1;
architecture Behavioral of mux4_1 is
```

```
component mux2_1
port( A,B : in STD_LOGIC;
S: in STD_LOGIC;
Z: out STD_LOGIC);
end component;
signal temp1, temp2: std_logic;
begin
m1: mux2_1 port map(A,B,S0,temp1);
m2: mux2_1 port map(C,D,S0,temp2);
m3: mux2_1 port map(temp1,temp2,S1,Z);
end Behavioral;
Output:
                                                                       Refile Edit View Project Source Process Window Help

Refile Edit View Project Sourc
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           _ 6 X
                                                                                                                                                                                                                                                                                                                                                                                                            18 --
19 --
20 library IEEE;
21 use IEEE. STD_LOGIC_1164.ALL;
22 entity mux2 l is
24 port(A,B : in STD_LOGIC;
25 S: in STD_LOGIC;
26 Z: out STD_LOGIC;
27 end mux2_1;
28
29 architecture Behavioral of mux2_l is
30
31 beris
                                                                         Sources X
Sources for: Behavioral Simulation 
aaabbb
caaabbb
caaabbb
                                                                                 xc3s400-4tq144

- A csds (csds tbw)

B - U UUT - mux4_1 - Behavio
                                                                          Sources Snapshot hibraries
                                                                                                                                                              architecture Senavi

begin

32

33 process (A,B,S) is

44 begin

35 if (5 = '0') then

36 2 <= A;

37 else

38 2 <= B;

39 end if;

40 end process;

41

42 end Behavioral;

43

44 library IEEE;
                                                                                                                         13 | 44 | library IEEE; 45 | use IEEE.STD LOGIC 1164.ALL;
```

Ln 19 Col 83 CAPS NUM SCRL VHDL

0.00 MB/s へ 知 ((4)) ENG 11:46 0.00 MB/s へ 知 ((4)) (1)

Simulator is doing circuit initialization process.
Finished circuit initialization process.

> run 3000 ns

Console SErrors 🔔 Warnings 🧰 Tcl Shell 🛣 Find in Files 🔤 Sim Console - cada

O 🛱 🔤

