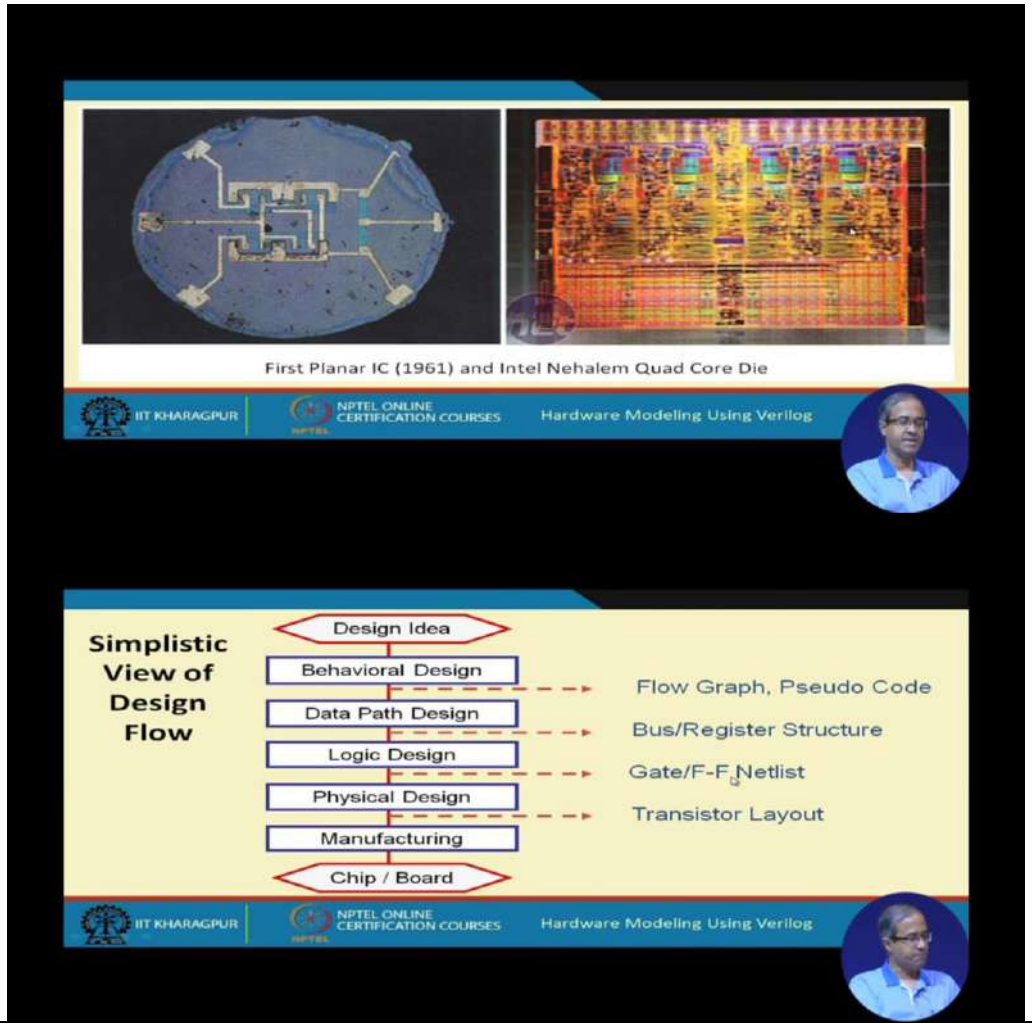
DAILY ASSESSMENT FORMAT

Date:	**04/06/2020**	**Name:**	**Lavanya B**
Course:	**Verilog HDL**	**USN:**	**4al17ec043**
Topic:	**Hardware modeling using verilog FPGA & ASIC interview questions**	**Semester & Section:**	**6th A**
Github Repository:	**Lavanya-B**		

FORENOON SESSION DETAILS
Image of session
Report



4/08/2020

Hardware modelling using verilog

VLSI - basic hardware chip

VLSI Design process

- Design complexity increasing rapidly
  - Increased size and complexity
  - Fabrication technology improving
  - CAD tools are essential
  - Conflicting requirements like area, speed & energy consumption
- The present trend
  - Standardise the design flow.
  - Emphasis on low-power design, increased performance

Moore's law

Exponential growth
Design complexity increase rapidly
Automated tools are essential
Must follow well-defined design flow

CMOS → FinFET → Quantum

VLSI Design Flow

- Specification
- Synthesis
- Simulation
- Layout
- Testability analysis

2 computing HDLs

1. Verilog
2. VHDL

FPGA and ASIC interview questions

1) Swap contents by 2 reg

- with temp reg:

```
always @(posedge clock)
begin
temp = b;
b = a;
a = temp;
end
```

- without temp reg:

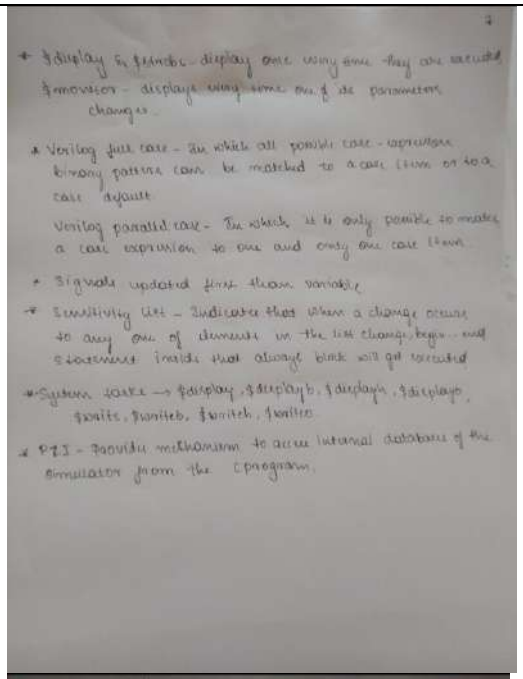
```
always @(posedge clock)
begin
a <= b;
b <= a;
end
```

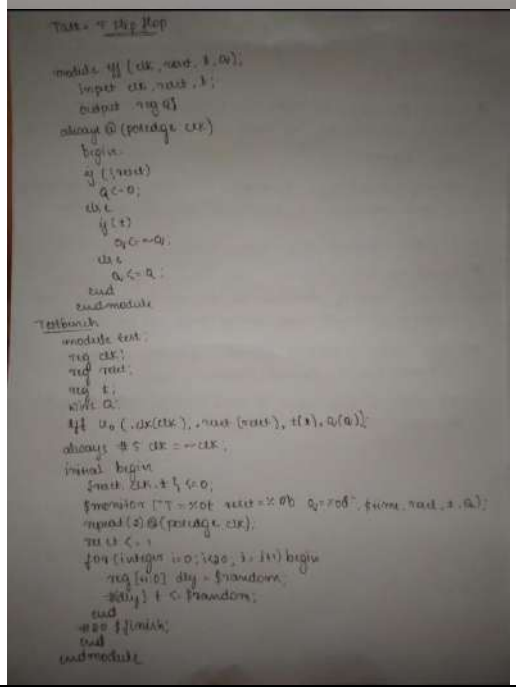
a) Blocking(=): the whole statement is done before control passes on the next statement

Non-blocking(<=): Evaluates all the right-hand sides for the current time unit and assigns the left hand sides at the end of the time unit

3) Tasks: Tasks are capable of invoking a function as well as enabling other tasks of task

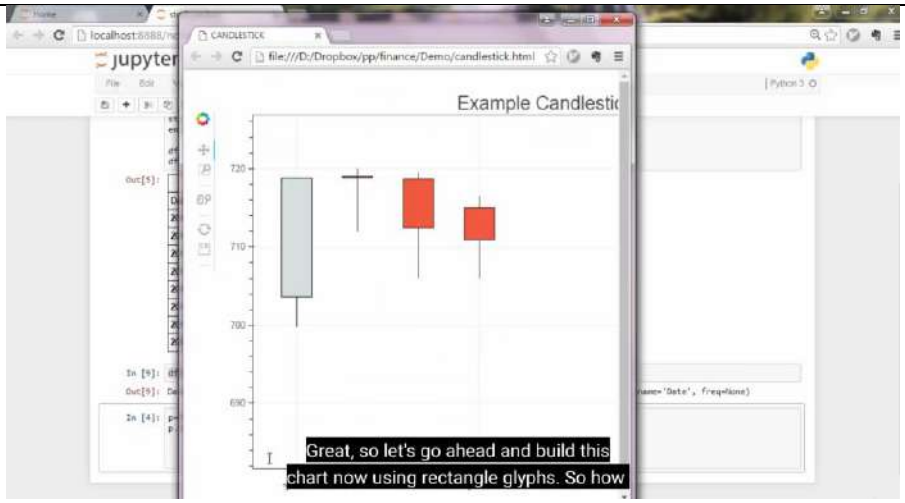
function: these are unable to enable a task however functions can enable other functions



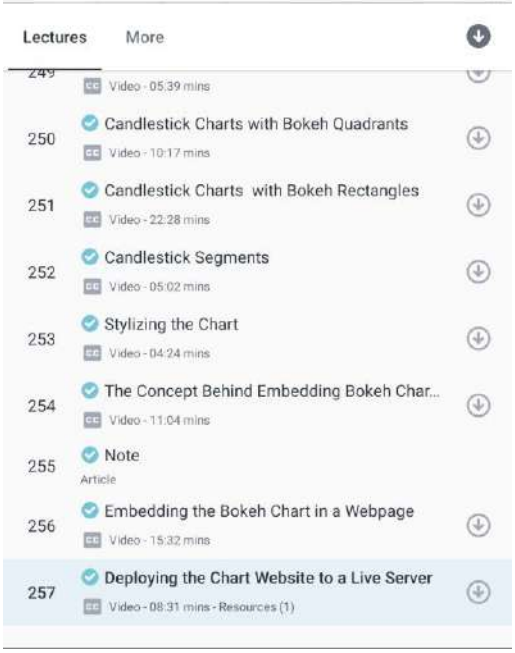


Date:	**04/06/2020**	**Name:**	**Lavanya B**
Course:	**Python**	**USN:**	**4al17ec043**
Topic:	**Application 09**	**Semester & Section:**	**6th A**

AFTERNOON SESSION DETAILS
Image of session


jupyter
CANDLESTICK
file:///D:/Dropbox/pp/finance/Demo/candlestick.html
Example Candlesti
720
710
700
690
Great, so let's go ahead and build this
chart now using rectangle glyphs. So how


ANDIT'S WEB APP
My about page
Candlestick Chart


Lectures
More
249
Video - 05:39 mins
250
Candlestick Charts with Bokeh Quadrants
Video - 10:17 mins
251
Candlestick Charts with Bokeh Rectangles
Video - 22:28 mins
252
Candlestick Segments
Video - 05:02 mins
253
Stylizing the Chart
Video - 04:24 mins
254
The Concept Behind Embedding Bokeh Char...
Video - 11:04 mins
255
Note
Article
256
Embedding the Bokeh Chart in a Webpage
Video - 15:32 mins
257
Deploying the Chart Website to a Live Server
Video - 08:31 mins - Resources (1)

Report

Application 09: Build a web-based functional graphs