

## DAILY ASSESSMENT FORMAT

Date:	04/06/2020	Name:	Lavanya B
Course:	Verilog HDL	USN:	4a117ec043
Topic:	Hardware modeling using verilog FPGA & ASIC interview questions	Semester & Section:	6th A
Github Repository:	Lavanya-B		

### FORENOON SESSION DETAILS

Image of session

First Planar IC (1961) and Intel Nehalem Quad Core Die

IIT KHARAGPUR NPTEL ONLINE CERTIFICATION COURSES Hardware Modeling Using Verilog

**Simplistic View of Design Flow**

```

graph TD
    A[Design Idea] --> B[Behavioral Design]
    B --> C[Data Path Design]
    C --> D[Logic Design]
    D --> E[Physical Design]
    E --> F[Manufacturing]
    F --> G[Chip / Board]
    B -.-> H[Flow Graph, Pseudo Code]
    C -.-> I[Bus/Register Structure]
    D -.-> J[Gate/F-F Netlist]
    E -.-> K[Transistor Layout]
  
```

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Report

Hardware modeling using Verilog  
VLSI - basic hardware chip

VLSI Design process

- Design complexity increasing rapidly
  - Increased size and complexity
  - Fabrication technology improving
  - CAD tools are essential
  - conflicting requirements size area, speed & energy consumption
- The primary trend
  - Standardize the design flow
  - Emphasis on low-power design, increased performance

Moore's Law

Exponential growth

- Design complexity increases rapidly
- Automated tools are essential
- Must follow well-defined design flow

CMOS → FinFET → Quantum

VLSI Design Flow

- Specification
- Synthesis
- Simulation
- Layout
- Testability analysis

2. Comparing HDLs  
1. Verilog  
2. VHDL

FPGA and ASIC Interview Questions

- 1) Swap contents by 2 ms  
+ with temp reg:

```
always @(posedge clk)
begin
  temp = b;
  b = a;
  a = temp;
end
```

- 2 without temp reg:

```
always @(posedge clk)
begin
  a <- b;
  b <- a;
end
```

- 3) Blocking(): the whole statement is done before control passes on the next statement

non-blocking(): Evaluate all the right-hand side for the current time unit and assigns the left-hand side at the end of the time unit

- 4) Tasks: These are capable of modeling a function as well as modeling other versions of task

Functions: These are unable to invoke a task however functions can make other functions

- \* \$display is printf - display one using one they are executed
- \$monitor - displays msg some no. of its parameter changes.
- \* Verilog full case - In which all possible case-expressions binary pattern can be matched to a case item or to a case default.
- Verilog parallel case - In which it is only possible to make a case expression to one and only one case item.
- \* Signals updated first than variable.
- \* Sensitive list - Indicates that when a change occurs to any one of elements in the list change begins and statement inside that always block will get executed.
- \* System tasks → \$display, \$displayb, \$displayh, \$displayp, \$write, \$writb, \$writeh, \$writp.
- \* PZI - Provides mechanism to access internal database of the simulator from the C program.

```

Title = "Flip Flop"

module ff (clk, reset, i, a);
    input clk, reset, i;
    output reg a;
    always @ (posedge clk)
    begin
        a <= i;
        if (i)
            a <= ~a;
        else
            a <= a;
    end
endmodule

// Testbench
module test;
    reg clk;
    reg reset;
    reg i;
    wire a;
    ff u0 (.clk(clk), .reset(reset), .i(i), .a(a));
    always #5 clk = ~clk;
    initial begin
        $monit 20, $monit 20, $monit 20, $monit 20, $monit 20, $monit 20, $monit 20, $monit 20;
        $input(0) @ (posedge clk);
        #10 i <= 1;
        for (integer i = 0; i < 10; i = i + 1) begin
            reg [10] dly = $random;
            #dly i <= $random;
        end
        #20 $finish;
    end
endmodule

```

Date: 04/06/2020  
Course: Python  
Topic: Application 09

Name: Lavanya B  
USN: 4a17ec043  
Semester 6th A  
& Section:

#### AFTERNOON SESSION DETAILS

Image of session



Lectures	More	
249	Video - 05:39 mins	
250	✓ Candlestick Charts with Bokeh Quadrants	
	Video - 10:17 mins	
251	✓ Candlestick Charts with Bokeh Rectangles	
	Video - 22:28 mins	
252	✓ Candlestick Segments	
	Video - 05:02 mins	
253	✓ Stylizing the Chart	
	Video - 04:24 mins	
254	✓ The Concept Behind Embedding Bokeh Char...	
	Video - 11:04 mins	
255	✓ Note	
	Article	
256	✓ Embedding the Bokeh Chart in a Webpage	
	Video - 15:32 mins	
257	✓ Deploying the Chart Website to a Live Server	
	Video - 08:31 mins - Resources (1)	

## Report

# Application 09: Build a web-based functional graphs

Application 09: Build a web-based financial graph.

- candlestick chart which is used for analysis in stock market.
- downloading data sets with python -  

```
from pandas_datareader import dataq
import datetime
```
- stock market data (candlestick chart)  

```
start = datetime.datetime(2015, 5, 1)
end = datetime.datetime(2016, 5, 10)
df = dataq.datareader(name = "GOOG", data_source = "yahoo",
start = start, end = end)
```
- Embedding the both chart in a webpage  
→ from flask import flask, render\_template  

```
app = flask(__name__)
@app.route("/")
def home():
    return render_template("home.html")
@app.route("/about")
def about():
    return render_template("about.html")
if __name__ == "__main__":
    app.run(debug = True)
```
- Code for script  

```
from flask import flask, render_template
app = flask(__name__)
@app.route("/plot")
def plot():
    from pandas_datareader import dataq
    import datetime
    from bokeh.plotting import figure, show, output_file
    from bokeh.embed import component
    from bokeh.palettes import cm
```

```
start = datetime.datetime(2015, 5, 1)
end = datetime.datetime(2016, 5, 10)
df = dataq.datareader(name = "GOOG", data_source = "yahoo",
start = start, end = end)
```

- plotting  

```
{% include "layout.html" %}
<? block content %>
<div class = "about">
<h1> my about page </h1>
<p> this is a test website again </p>
</div>
<? end block %>
```