**DAILY ASSESSMENT FORMAT**

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| **Date:** | **03/06/2020** | **Name:** | **Lepakshi T V** |
| **Course:** | **Digital design using HDL** | **USN:** | **4AL17EC044** |
| **Topic:** | **EDA Tool** | **Semester & Section:** | **6th sem, A sec** |
| **Github Repository:** | **Lepakshi-044** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **EDA playground online complier:**  **EDA Playground** gives engineers immediate hands-on exposure to simulating Verilog/SystemVerilog/VHDL. All you need is a web browser. The goal is to accelerate learning of design/testbench development with easier code sharing, and with simpler access to simulators and libraries. EDA Playground is specifically designed for small prototypes and examples.   * With a simple click, run your code and see console output in real time. Pick another simulator version and run it again. * Save your code snippets. Share your code and simulation results with a web link. Perfect for web forum discussions or emails. Great for asking questions or sharing your knowledge. * Quickly try something out   + Try out a System Verilog feature before using it on your project.   + Try out a library that you're thinking of using.   + Modify another engineer's shared code and re-run it. * Eliminate environment differences. Since the code always executes in the same environment, everyone will see the same result on a subsequent re-run. * Browse and use a large repository of working code examples and templates.   **How to download and install xilinx Vivada design suite:**  1.Go to [www.xilinx.com](http://www.xilinx.com)  2.Select which we need to download  3.Sign in and download  **4:1 Mux:**  module and\_gate(output a, input b, c, d);  assign a = b & c & d;  endmodule  module not\_gate(output f, input e);  assign e = ~ f;  endmodule  module or\_gate(output l, input m, n, o, p);  assign l = m | n | o | p;  endmodule  module m41(out, a, b, c, d, s0, s1);  output out;  input a, b, c, d, s0, s1;  wire s0bar, s1bar, T1, T2, T3;  not\_gate u1(s1bar, s1);  not\_gate u2(s0bar, s0);  and\_gate u3(T1, a, s0bar, s1bar);  and\_gate u4(T2, b, s0, s1bar);  and\_gate u5(T3, c, s0bar, s1);  and\_gate u6(T4, d, s0, s1);  or\_gate u7(out, T1, T2, T3, T4);  endmodule  **Test Bench Code:**  module top;  wire  out;  reg  a;  reg  b;  reg  c;  reg  d;  reg s0, s1;  m41 name(.out(out), .a(a), .b(b), .c(c), .d(d), .s0(s0), .s1(s1));  initial  begin   a=1'b0; b=1'b0; c=1'b0; d=1'b0;  s0=1'b0; s1=1'b0;  #500 $finish;  end  always #40 a=~a;  always #20 b=~b;  always #10 c=~c;  always #5 d=~d;  always #80 s0=~s0;  always #160 s1=~s1;  always@(a or b or c or d or s0 or s1)  $monitor("At time = %t, Output = %d", $time, out);  endmodule; |

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| **Date:** | **03/06/2020** | **Name:** | **Lepakshi T V** |
| **Course:** | **Python** | **USN:** | **4AL17EC044** |
| **Topic:** | **Srapel Real estate properly data from the web** | **Semester & Section:** | **6th sem, A sec** |
| **Github Repository:** | **Lepakshi-044** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**   * **Loading the web page in Python** * **Extracting div tags** * **How to request headers** * **Extracting address and property details** * **Extracting elements without unique identifiers** * **Saving the data CSV files** * **Crawling through web pages** |