**DAILY ASSESSMENT FORMAT**

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| **Date:** | **04/06/2020** | **Name:** | **Lepakshi T V** |
| **Course:** | **Digital design using HDL** | **USN:** | **4AL17EC044** |
| **Topic:** | 1. **Hardware modelling using Verilog** 2. **FPGA and ASIC Interview questions** 3. **Implement T-FF** | **Semester & Section:** | **6th sem , A sec** |
| **Github Repository:** | **Lepakshi-044** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  **Hardware modelling using Verilog:**   * Learn about the Verilog HDL. * Difference between structural and behavioral design. * To write test benches and analyze simulation. * Model combinational and sequential circuits. * Differentiate between good and bad coding practices.   **VLSI design process:**   * Design complexity increasing rapidly. * The present trend   **Moore’s Law:**   * Exponential growth * Design complexity increasing rapidly * Automated tools are essential * Must follow well defined design flow   **VLSI design flow:**   * Standardized design procedure * Encompasses many steps * Need to use CAD tools   **Verilog code to implement T-FF :**  module tff ( input clk,  input rstn,  input t,  output reg q);    always @ (posedge clk) begin  if (!rstn)  q <= 0;  else  if (t)  q <= ~q;  else  q <= q;  end  endmodule  **Test bench code:**  module tb;  reg clk;  reg rstn;  reg t;    tff u0 ( .clk(clk),  .rstn(rstn),  .t(t),  .q(q));    always #5 clk = ~clk;    initial begin  {rstn, clk, t} <= 0;    $monitor ("T=%0t rstn=%0b t=%0d q=%0d", $time, rstn, t, q);  repeat (2) @ (posedge clk);  rstn <= 1;    for (integer i = 0; i < 20; i = i+1) begin  reg [4:0] dly = $random;  #(dly) t <= $random;  end  #20 $finish;  end  endmodule |

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| **Date:** | **04/06/2020** | **Name:** | **Lepakshi T V** |
| **Course:** | **Python** | **USN:** | **4AL17EC044** |
| **Topic:** | **Build a web based financial graph** | **Semester & Section:** | **6th sem , A sec** |
| **Github Repository:** | **Lepakshi-044** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**   * Downloading datasets with python * Stock market data * Stock market data candlestick charts * Candlestick charts and Bokeh rectangles * Candlestick segments * Styling the charts * The concept behind embedded Bokeh charts in webpage * Deploying the chart website to a live server. |