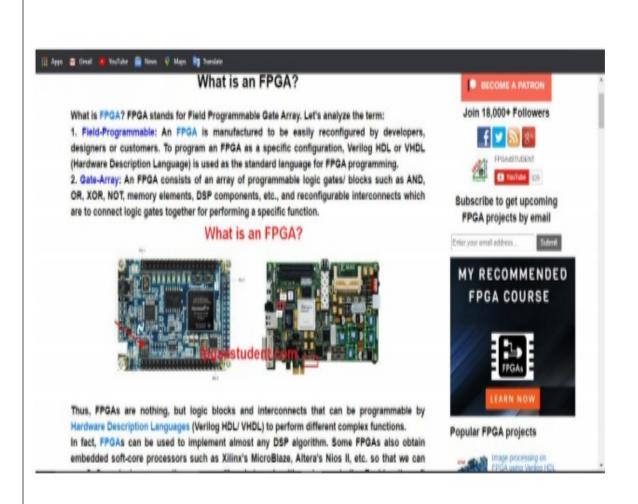
DAILY ASSESSMENT FORMAT

Date:	05-06-2020	Name:	M V Ramya
Course:	logic design	USN:	4AL17EC045
Topic:	FPGA	Semester & Section:	6th sem, A sec
Github Repository:	M V Ramya-045		

FORENOON SESSION DETAILS	



```
- FPGA -> Field Programmable Grate Array . It is an
                                                             bigin
    integrated circuit which can be "filld" programme.
                                                          10=0:
     to work as per the intended design
                                                            2 = 0:
 - Virilag like any other hardward description language
    permit the designed to design a design in either
                                                          for liso; i < 16 di+1)
     Bottom up or Top-down methodology
 - Various stage of ASIC IFFGA : Specification
                                                          it (In[i] == 1'b1)
                                 High level Duign
                                micro Design I law level Dun
                               RTL coding
                                                          0 = 0+1;
                                Syntheis
                                                          Z = 16-0;
                              Place and route
  - An FPGA designer likes working on this due to them
                                                           ones = 0;
    reason: - Very fast on-thip (FPGA) demostration
                                                          21103 = Z3
             simple and fast duign process on FPGA
            FPGA's programmability.
                                                         und
           FPHA's high performance
                                                         undmodule.
            FPGA's fleaibility
 Task: luplement a verilog module to count number
           of 0's in a 16 bit number in complete
module num-zero-onu
linput [15:0] in, output reg[4:0] once, output reg[4:0] 2008);
integer 1,0,2;
always @ (in)
```

Date: 05june 2020 Name: MV Ramya

Course: python USN:4AL17EC045

Topic:web app with Semester & 6th sem Asec

PostGreSQL and Flask Section:

AFTERNOON SESSION DETAILS

Image of session



```
Python
   Application: 4 Build a Date collector web app
      with Post GresQL and Flaste.
  * Post Gresal Oatabase with App with Flash: step
  - Develop a HTML code for generating a webpage
  - Backend & Frontend is developed
 - Frontend sends the data to Backend
 * Frontend -> HIML
  < ! DOCTYPE html>
  <html larg = "in">
  < title > Data collector APP </title>
 < link href = ". Istotic Imain . css " rel = "styluheet">
  < lhead>
  < body>
  < div class = "container">
 < hix collecting hight < /hix

    \( h_3 > Please fill the entires to get population station of

                            hilght <143>
 ( form action = "succes , when method = upost" >
 <input title = "gour email will be sate with us" ,
              holder = "Enter your email address" hype
                name = "email - name" required > 460
Emport title = "your date will be safe with us "place hidd
```

```
Enter hight em "type = "number" min = "50", max = "300
               nume = "hight num" (br >)
Chutton type = "submit" > submit < 1 button >
< I form>
 < 1div>
< 160d4>
21 html>
Buckend: Getting user iput
from flush import Flush, render template, request app.
                                           Flask (-nume
(a) upp. route ("/")
 def index ():
return rendle-template ("index , html")
@ app. route ("/ succes", method = ['post'])
det weener:
 it request . method = " POST' :
 email = request . form [ "email - name"]
     print (request. (om)
     return render-template (" weenful - html")
 it-nume = '- main -' :
  app. debug = Trul
  upp . runch .
```