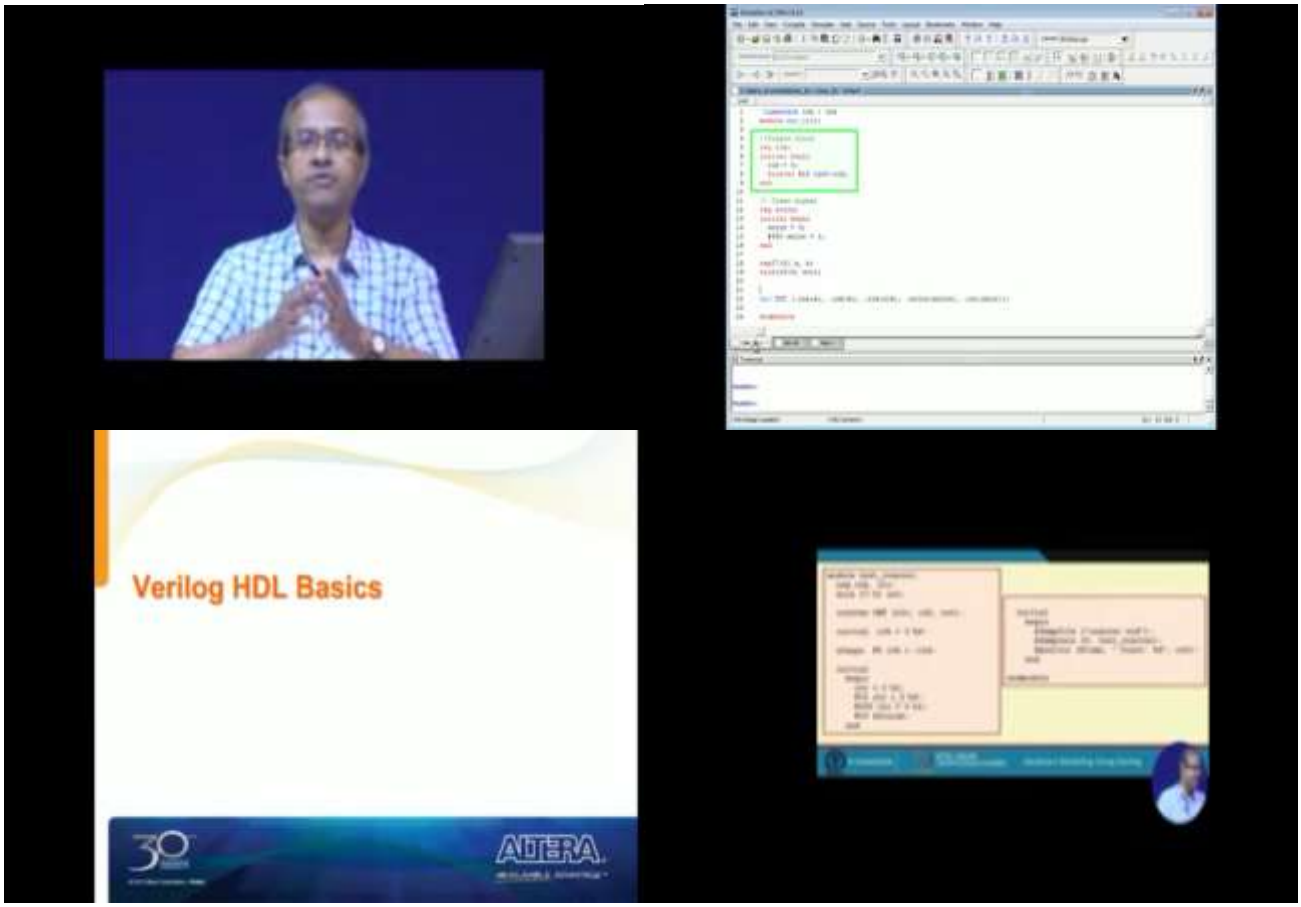
DAILY ASSESSMENT FORMAT

Date:	**02_06_2020**	**Name:**	**PRINCIA MELITA DSOUZA**
Course:	**DIGITAL DESIGN USING HDL**	**USN:**	**4AL17EC075**
Topic:	**FPGA**	**Semester & Section:**	**6TH B**
Github Repository:	**MELITA-1999**		

FORENOON SESSION DETAILS

Image of session



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THE TERM FPGA STANDS FOR FIELDPROGRAMMING GATE ARRAY

And it is a one type of semiconductor logic chip which can be programmed to become almost any kind of system or digital circuit , similarly to PLDs . PLDs are limited to hundred of gates , but FPGAs supports 1000 of gates .The configuration of the FPGA architecture is generally specified using a language i.e , HDL hardware description language which is similar to the one used for an ASIC.

Field Programmable Gate Arrays

FPGAs can provide a number of advantages over a fixed function ASIC technology such as standard cells. Normally, ASICs takes months to manufacture and the cost of them will be thousands of dollars to obtain the device. But, FPGAs are fabricated in less than a second,the cost will be from a few dollars to a thousand dollars.The flexible nature of the FPGA comes at a significant costin area, power consumption and delay.When compared to a standard cell ASIC, an FPGA requires 20 to 35 times more area, and the speed's performance will be 3 to 4 times slower than the ASIC. This article describes about theFPGA basics and FPGA architecture module that includes I/O pad, logic blocks and switch matrix. FPGAs are some of the new trending areas of VLSI. Therefore, these are used in VLSI based projects for electronic engineering students.

FPGA Architecture

The general FPGA architecture consists of three types of modules. They are I/O blocks or Pads, Switch Matrix/ Interconnection Wires and Configurable logic blocks (CLB). The basic FPGA architecture has two dimensional arrays of logic blocks with a means for a user to arrange the interconnection between the logic blocks. The functions of an FPGA architecture module are discussed below:CLB (Configurable Logic Block) includes digital logic, inputs, outputs. It implements the user logic.Interconnects provide direction between the logic blocks to implement the user logic.Depending on the logic, switch matrix provides switching between interconnects. I/O Pads used for the outside world to communicate with different applications.FPGA Architecture Logic Block contains MUX (Multiplexer), D flip flop and LUT. LUT implements the combinational logical functions; the MUX is used for selection logic, and D flip flop stores the output of the LUT The basic building block of the FPGA is the Look Up Table based function generator. The number of inputs to the LUT vary from 3,4,6, and even 8 after experiments. Now, we have adaptive LUTs that provides two outputs per single LUT with the implementation of two function generators.

FPGA Logic Block

Xilinx Virtex-5 is the most popular FPGA, that contains a Look up Table (LUT) which is connected with MUX, and a flip flop as discussed above. Present FPGA consists of about hundreds or thousands of configurable logic blocks. For configuring the FPGA, Modelsim and Xilinx ISE softwares are used to generate a bitstream file and for development.Types of FPGAs Based on ApplicationsField Programmable Gate Arrays are classified into three types based on applications such as Low-end FPGAs, Mid-range FPGAs and high-end FPGAs

Code for multiplexing

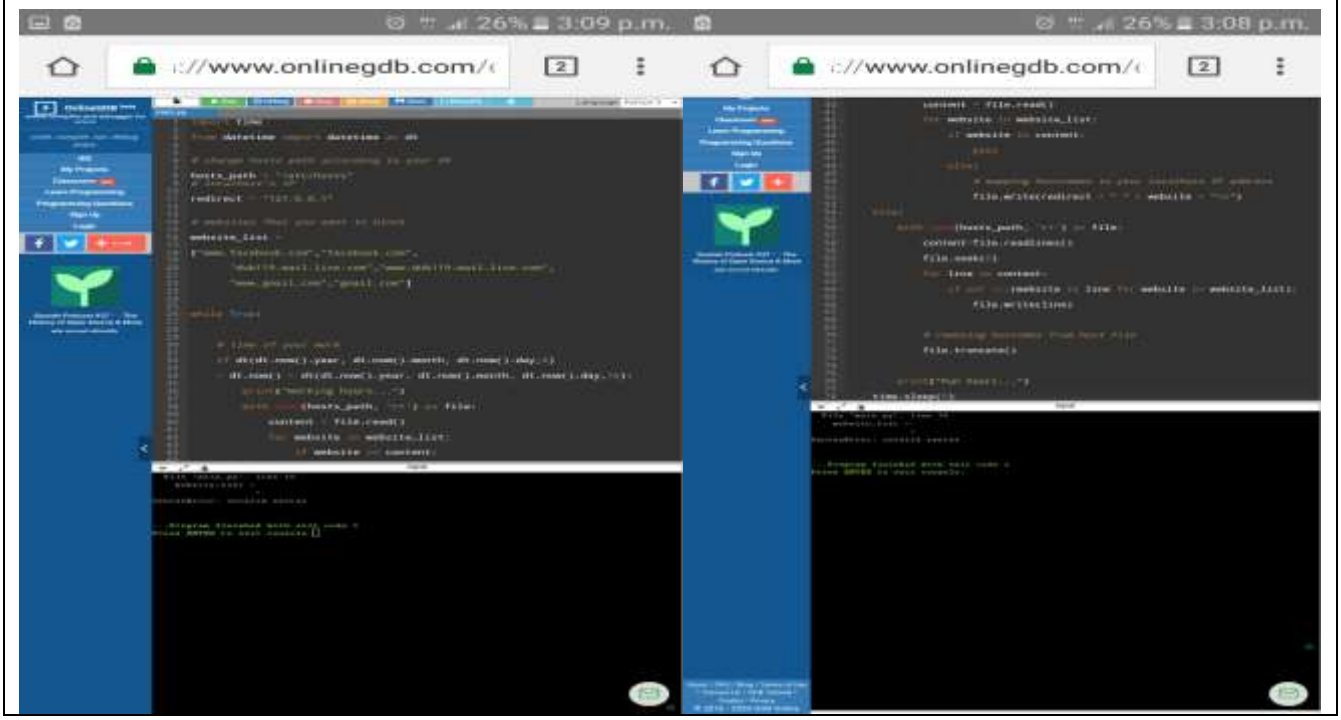
```
module mux_4to1_case ( input [3:0] a,              // 4-bit input called a
                       input [3:0] b,              // 4-bit input called b
                       input [3:0] c,              // 4-bit input called c
                       input [3:0] d,              // 4-bit input called d
                       input [1:0] sel,            // input sel used to select between a,b,c,d
                       output reg [3:0] out);      // 4-bit output based on input sel
```

```
  // This always block gets executed whenever a/b/c/d/sel changes value
  // When that happens, based on value in sel, output is assigned to either a/b/c/d
  always @ (a or b or c or d or sel) begin
    case (sel)
      2'b00 : out <= a;
      2'b01 : out <= b;
      2'b10 : out <= c;
      2'b11 : out <= d;
    endcase
  end
endmodule
```

Date:	**02_06_2020**	**Name:**	**PRINCIA MELITA DSOUZA**
Course:	**PYTHON**	**USN:**	**4AL17EC075**
Topic:	**WEB SCRAPING WITH PYTHON BEAUTIFUL SOUP & INTERACRIVE DATA VISUALIZATION WITH BOKEH**	**Semester & Section:**	**6TH B**

AFTERNOON SESSION DETAILS

Image of session



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WEB SCRAPING WITH PYTHON BEAUTIFUL SOUP

The incredible amount of data on the internet is a rich resource of any field id research or personal internet.
To effectively harvest the data , you ll need to become skilled at web scraping . the python libraries requests and beautiful soul are powerful tools for job.if you like to learn with hands on examples and you have a basic understanding of python and HTML.

INTERACRIVE DATA VISUALIZATION WITH BOKEH

Bokeh prides itself on being a library for interactive data visualization.
Unlike popular counterparts in the python visualization space, like matplotlib and seaborn, bokeh renders its graphics using HTML and java scripts.