**DAILY ASSESSMENT FORMAT**

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| **Date:** | **02/06/2020** | **Name:** | **PADMINI M** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC066** |
| **Topic:** | **FPGA Basics: Architecture, Applications and Uses**  **Verilog HDL Basics by Intel**  **Verilog Testbench code to verify the design under test (DUT)** | **Semester & Section:** | **6th Bsec** |
| **Github Repository:** | **Padmini** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  FPGA Architecture   * A basic FPGA architecture (Figure 1) consists of thousands of fundamental elements called configurable logic blocks (CLBs) surrounded by a system of programmable interconnects, called a fabric, that routes signals between CLBs. * Input/output (I/O) blocks interface between the FPGA and external devices. * Depending on the manufacturer, the CLB may also be referred to as a logic block (LB), a logic element (LE) or a logic cell (LC). * An individual CLB (Figure 2) is made up of several logic blocks. A lookup table (LUT) is a characteristic feature of an FPGA. An LUT stores a predefined list of logic outputs for any combination of inputs   SoC FPGAs  The FPGA product family includes complex system-on-chip (SoC) parts that integrate the FPGA architecture, hard IP and a microprocessor CPU core into a single component. Compared to separate devices, a SoC FPGA provides higher integration, lower power, smaller board size and higher-bandwidth communication between the core and other blocks.  FPGA Design  Designers have traditionally used a hardware description language (HDL) such as VHDL or Verilog to design the FPGA configuration.  Once the FPGA design has been created and verified using HDL, the compiler takes the text-based file and generates a configuration file that contains information on how the components should be wired together. Even if the HDL code has no errors, choosing the wrong FPGA may still cause the compilation to fail.  FPGA Applications:    A good example of FPGA use is high-speed search: Microsoft is using FPGAs in its data centers to run Bing search algorithms. The FPGA can change to support new algorithms as they are created. If needs change, the design can be repurposed to run simulation or modeling routines in an HPC application. This flexibility is difficult or impossible to achieve with an ASIC.  Other FPGA uses include aerospace and defense, medical electronics, digital television, consumer electronics, industrial motor control, scientific instruments, cybersecurity systems and wireless communications. |

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| **Date:** | **02/06/2020** | **Name:** | **PADMINI M** | |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC066** | |
| **Topic:** | **Interactive Data Visualization with Bokeh**  **Webscraping with Python Beautiful Soup** | **Semester & Section:** | **6th Bsec** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| |  | | --- | | **Report – Report can be typed or hand written for up to two pages.**   * Bokeh is a data visualization library for Python. Unlike Matplotlib and Seaborn, they are also Python packages for data visualization, Bokeh renders its plots using HTML and JavaScript. Hence, it proves to be extremely useful for developing web based dashboards. * The Bokeh project is sponsored by NumFocus also supports PyData, an educational program, involved in development of other important tools such as NumPy, Pandas and more. * Bokeh can easily connect with these tools and produce interactive plots, dashboards and data applications. * Bokeh primarily converts the data source into a JSON file which is used as input for BokehJS, a JavaScript library, which in turn is written in TypeScript and renders the visualizations in modern browsers. * When a Bokeh plot is rendered, normally a tool bar appears on the right side of the figure. It contains a default set of tools. First of all, the position of toolbar can be configured by toolbar\_location property in figure() function. This property can take one of the following values above,below,left,right,None.   Steps involved in web scraping:   * Send an HTTP request to the URL of the webpage you want to access. The server responds to the request by returning the HTML content of the webpage. For this task, we will use a third-party HTTP library for python-requests. * Once we have accessed the HTML content, we are left with the task of parsing the data. Since most of the HTML data is nested, we cannot extract data simply through string processing. One needs a parser which can create a nested/tree structure of the HTML data. There are many HTML parser libraries available but the most advanced one is html5lib. * Now, all we need to do is navigating and searching the parse tree that we created, i.e. tree traversal. For this task, we will be using another third-party python library, Beautiful Soup. It is a Python library for pulling data out of HTML and XML files. | | | | |