**DAILY ASSESSMENT FORMAT**

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| **Date:** | **04/06/2020** | **Name:** | **PADMINI M** |
| **Course:** | **DIGITAL DESIGN USING HDL** | **USN:** | **4AL17EC066** |
| **Topic:** | **Hardware Modeling usingVerilog,Implement T Flip-Flop** | **Semester & Section:** | **6th Bsec** |
| **Github Repository:** | **Padmini** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report – Report can be typed or hand written for up to two pages.**  Hardware Modeling UsingVerilog Objective of Hardware Modeling Using Verilog   * Learn about the Verilog hardware description language. * Understand the difference between behavioral and structural design styles. * Learn to write test benches and analyze simulation results. * Learn to model combinational and sequential circuits, * Distinguish between good and bad coding practices. * Case studies with some complex designs.   VLSI Design Process   * Design complexity increasing rapidly * Increased size and complexity * Fabrication technology improving * CAD tools are essential * Conflicting requirements like area, speed, and energy consumption   The present trend   * Standardize the design flow * Emphasis on low-power design, and increased performance Moore’s Law * Exponential growth * Design complexity increases rapidly * Automated tools are essential * Must follow well defined design flowStandardized design procedure * Starting from the design idea down to the actual implementation. * Encompasses many steps: * Specification Synthesis   Simulation   * Layout Testability analysis * and many moreNeed to use Computer Aided Design (CAD) tools. * Hardware Description Language (HDL) * Based on HDL provide formats for representing the outputs of various design steps * A CAD tool transforms its HDL input into a HDL output that contains more detailed information about the hardware. * Behavioral level to register transfer level * Register transfer level to gate level * Gate level to transistor level * Transistor to the layout level Two Competing HDL’s * Verilog * VHDLBehavioral design * Specify the functionality of the design in terms of its behavior. * Various ways of specifying: * Boolean expression or truth table. * Finite-state machine behavior (e.g. state transition diagram or table). * In the form of a high-level algorithm. * Needs to be synthesized into more detailed specifications for hardware realization, Data path design * Generate a netlist of register transfer level components, like registers, adders,multipliers,multiplexers, decoders, etc. |

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| **Date:** | **04/06/2020** | **Name:** | **PADMINI M** | |
| **Course:** | **PYTHON** | **USN:** | **4AL17EC066** | |
| **Topic:** | **Build a Web-basedFinancial Graph** | **Semester & Section:** | **6th Bsec** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| **Report – Report can be typed or hand written for up to two pages.**  Web-based Financial Graph:   * How to DownloadDatasets with Python * Learnt analyzing Stock Market Data. * Plotting Stock Market Data Candlestick Charts. * Updating Candlestick Charts with Bokeh Quadrants * Learnt to plot Candlestick Charts with Bokeh Rectangles * Creating Candlestick Segments * Stylizing the obtained Chart * Learnt the Concept Behind Embedding Bokeh * Sharing the Charts in a Flask Webpage * Learnt how to Embedthe Bokeh Chart in a Webpage. * Learnt to Deploythe Chart Website to a Live Server. * Below shown are the some pictures of graph produced, which are the stocks of Google from 01 Jan 2020 to 30 May 2020 andplotted using Candlestick format. | | | |