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HDL

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Verilog Tutorial

Verilog is a Hardware description language (HDL) which is used to describe a digital system.

Design Methodologies → Top-down and Bottom-up,

Abstraction levels of verilog:
Behavioral level, Register-Transfer level, gate level.

Various stages of ASIC / FPGA.
Specification, High level design, Micro Design / Low level design, RTL coding, Simulation, Synthesis, place & Route, Post SI validation.

code-

```
Module hello-world;
Initial begin.
    $display ("Hello world");
    #10 $finish;
end.
```

```
end fpga_adder;
architecture structural of fpga_adder is
signal tmp1, tmp2, tmp3: std_logic;
begin
    tmp1 <= A xor B;
    tmp2 <= A and B;
    tmp3 <= tmp1 and Ci;
    Co <= tmp2 or tmp3;
    S <= tmp1 xor Ci;
end structural;
```

* Implement a verilog Module to count the number of 0s in a 16 bit number in computer.

```
Module num_zeroes(input [15:0] A, output
reg [4:0] zero);
integer i;
always @(A)
begin
  zeroes = 0;
for (i=0; i<16; i=i+1)
  if (A[i] == 1'b0)
    zeroes = zeroes+1;
end
endmodule
```

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* Application -10: Build a data collector web App with postgresSQL and Flask

- Postgresql Database web App with Flask step.
- Develop a HTML code for generating a webpage.
- Backend & frontend is developed.
- frontend sends the data to backend.

- FRONTEND → HTML

```
<!DOCTYPE html>
<html lang = "en">
<title> Date collector App </title>
<head>
<link heat = "../static/main.css" rel =
"stylsheet">
</head>
<body>
<div class = "container">
<h1> collecting height </h1>
<h3> Please fill the entries to get
Population statistics of height </h3>
<form action = "success.html" Method="post">
<input title = "your email address" type=
```

name = "email" name "required" >
<input title = "your data will be safe with us" placeholder
= enter height in cM" type = "number" min
max = "300", name = "height_name"
<button type = "submit" > submit </button>
</form>

</body>
</Html>

Backend: getting user input.
from flask import Flask, render_template, request,
app = Flask (__name__)

- Verilog HDL abstraction levels-
  Behavioral Models
  RTL Models.
  Structural Models

* Building / Demo projects, using FPGA.

- FPGAs are nothing but logic blocks and interconnects that can be programmable by Hardware description languages (verilog HDL / VHDL) to perform different complex functions

- Verilog code for Adder on FPGA-
  Module fpga adder (input A, B, C,
  output S, CO);
  wire temp1, tmp2, tmp3;
  xor u1 (temp1, A, B);
  and u2 (tmp2, A, B);
  and u3 (tmp3 temp1, Ci);
  or (co, tmp 2, tmp3);
  xor u5 (S, tmp1, Ci);
  endmodule.

  library ieee;
  use ieee. std, logic, 1164, all;
  entity fpga, adder is.
  port (A, B, Ci : in std, logic;
  S, CO : out std, logic);