Poojary Sushmita Shrinivas
1AL16EC046
6B - 1/6/2020
Digital design HDL

* Diff hardware are like signs...

1) ASIC (Application specific Integratted ckt.)
2) ASSP (Application specific standard product)
3) FPGA (Field programmable gate array)

* FPGA?

→ An FPGA is a digital, configurable ASIC. I say mostly because there are analog & mixed-signal aspects to modern FPGAs. For ex:- some have A/D converters & PLLs. I put re-in parethesis because there are actually one-time-programmable FPGAs where once you configure them, that's it, never

* FPGA Basics - A look under Hood :
- The main underlying technology options are SRAM- based flash & anti fuse.

→ strengths :- • parallel prove.
• High data -to - clk - rate - ration.

→ Weaknesses :- • Complex calculations intevfveo
• Sorting Isearching.
• flooting point avithemetic.
• Very low power, low cost.

→ FPGA is a synchronous - device.
→ Core components - look up table, flipflop, Block memory, multipliers or DSP blocks, I/o, docking & routing

* Task for Day-1
- Write a veriloy code to implement NAND gate in all diff styles.

① Gate-level modeling

```
module NAND-2 (output Y, input A,B);
wire Yd,
and (Yd, A,B);
not (Y,Yd);
endmodule:
```

② Data flow modeling

```
modul NAND_2 (output Y, input A,B);
assign Y = ~(A &B);
```

3) Behavioral modeling

```
module NAND_2 (output reg Y, input A, B);
always @ (A or B) begin
    if (A == 1'b1 & B == 1'b1) begin
      Y = 1'b0;
    end
    else
      Y = 1'b1;
end
endmodule
```

Application 6:-
Build a webcam motion detector.
- Detect in web-cam objects:

```
import cv2, time
first_frame = None
video = cv2.videoCapture(0)

while true:
    check, frame = video.read()
    gray = cv2.cvtcolor(frame, cv2.COLOR_
                        BGR2GRAY)
    Gray = cv2.GaussionBlur(gray, (21,21), 0)

    if first_frame is none:
    first_frame = gray
    continue
delta_frame = cv2.obsdiff(first_frame, gray)
thresh_frame = cv2.threshold(delta_frame, 30, 225
                    cv2, THRESH_BINARY)[1]
thresh_frame = cv2.delate(thresh_frame, none,
                    interaction = 2)
cnts,) cv2.findContours(thresh_frame.copy(),
                    cv2, RETR_EXTERNAL, cv2.(HAIN_
                    APPROX_SIMPLE)
for contour in cnts:
    if cv2.contourArea(contour) < 1000;
    continue
```

```
(x, y, w, h) = cv2.boundingRect(contour)
cv2.rectangle(frame, (x, y), (x+w, y+h), (0, 255, 0), 3)

cv2.imshow("Gray Frame", gray)
cv2.imshow("Delta Frame", thresh_frame)
cv2.imshow("Color Frame", frame)

key = cv2.waitKey(1)
```

GUVI

tech deserves you

Sushmita Poojary

is here by awarded the certificate of achievement for

the successful completion of

Step into Robotic Process Automation

during GUVI's RPA SKILL-A-THON 2020

S.P.Balamurugan

Co-founder, CEO

Verify certificate at

In association with

UiPath Academic Alliance