	Poojary Suchmita Shrinivas
	HALIBEC OH 6
	6B1. 6 2020
	Digital design HDL
Jr.	Diff hardware are like signs.
44/25/21	
	1) ASIC (Application specific integrated cht.)
	2) ASSP (poolication specific standard product)
	3) FPGA (Field programmable gate array)
•	The state of the s
*	FPGA?
	An FPGA is a digital, configurable ASIC, I say
	mostly because there are analog & mixed-signal
	aspects to modern FOGAS. For existing have AD
	convertors & PLLs. I put re-in parethesis because
-	there are actually one-time-programmablex FPGAs
₹,	where on a you configure them, that's It, never

	O Mark law Wood?
*	FPGA Basic - A look under Hood:
	· The main underlying technology: aptions are
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	SAAM- based flash & antifuse. Strengths:-Pavallel proce.
	Strengths paraced processing strengths paraced processing the strength paraced processing the strengths paraced processing the
	-) Weaknesses; - « Complex calculations interfreo
	Sortino I searchine
	· flooting point arithemetic.
	· Very low power, low cost.
3 E	PGA is a synchronous-device.
7 0	ove components - look up table, flipflop, Block memory
· · · · · · · · · · · · · · · · · · ·	nultipliers or DSP blocks, To docking & routing
X T	ask for Day-1
	write a veriloy code to implement NAND gate in
00	l diff styles.
n G	10te-level modeling
m D	dule NAND-2 (output Y, input A,B);
1.134	2 Yd,
11	b (Yd, A,B);
- 11	
11	(v; vd);
endi	nodua:
100	
(g) 10	ita flow modeling
mode	of NAND-2 (output Vinput A.B);
Ossign	1 Y = ~ (A & B);

44

	3 Behavioral modeling
	module NAND 2 Courput veg Y, input A, B;
· .	Olways Q (A or B) begin 14 (A = = 1'b1 & B ==1 b) begin
	12 (A == 1'61 & B==1'61) begin
	1=1,80) - 1000 -
	end
	2=1'b1;
	[마리] 그렇게 다른데 마스 마스 마스 (1) [마스 마스트 (1) [마스 마스트 (1) [마스트 (
	end end module
\parallel	and module
#	
\parallel	Traine a market and the second of the second
	Well Diversity of Colonies Diversity Colonies
#	
\parallel	
#-	
	200,77,7,303.3
	LARCE SERVICE STREET, I LET SEVEN STREET STREET
	The state of the s
	ATTO ROBERT LANGE HE TO LEVO.
· Vila	Warren J. W. J. S. J. Company D. L. C. W. C. L. C.
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	Company of the contract of the
	Little Land Committee Comm

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Python 1/6/2020
The second of th
Application 6:
Build a webcom motion detector.
· Detectin web-com objects:
import CV2, time
first frame = None
Video = CV2. Video Capture (0)
while true:
check, frame = video. read()
gray = CV2, CV + color (frame, CV2, COLOR_
BCRBGRAY)
gray = (V2. & Gayssion Blue (gray, (21,21), 0)
if first frame is none:
first frame = gray
continul
elta_frame = CV2. obsdiff (first_frame gray)
thresh-frame= CV2. Othreshold (delta-frame, 30,225
CV2, THRESH-BINARY)[]
hresh-frame = CV2. delate (thresh-frame, none.
in teraction= 2)
cnts-) (va. find contours (thresh-frame, copy)
CV8, RETR_ EXTERNAL, CV2. (HAIN_
APPROX SIMPLE)
or contout in ents:
;4 (V2. contour Area Contour) < 1000;
continue
Scanned with CamScanner

	(x,yw,b) = (V2 - boundin Roct (con tour)
	(X, Y, W, h) = (V2 - boundin Rect (contout) (V8, 10ctorge (frame, (X, Y), (X+W, Y+h), (0,255,0),3
	CV2, imshow ("Gray Frame, gray)
	CV2. imshow ("Gray Frame", gray) CV2. imshow ("Delta France", thresh-frame)
	CV2 imshow (" colox frame", frame
	Kly = CV2, waitkey (1)
4	



Sushmita Poojary

is here by awarded the certificate of achievement for the successful completion of

Step into Robotic Process Automation

during GUVI's RPA SKILL-A-THON 2020

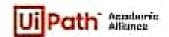
S.P.Balamurugan

Venter cembrate as e on June 12020.

With mith min ID glad video CTC LIBORH

Ca-founder, CEO

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