**DAILY ASSESSMENT FORMAT**

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| **Date:** | **02-06-2020** | **Name:** | **Pragati M Kundalkar** |
| **Course:** | **Digital design using HDL** | **USN:** | **4AL17EC072** |
| **Topic:** | **FPGA basics: Architecture, Applications and uses.**  **Verilog HDL Basics by intel.**  **Verilog testbench code to verify the design under test (DUT)** | **Semester & Section:** | **6TH SEM**  **B - SEC** |
| **Github Repository:** | **Pragati-m-k** |  |  |

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| **FORENOON SESSION DETAILS** |
| C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\HDL_2_1.jpg  C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\HDL_2_2.jpg |

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| **Date:** | **02-06-2020** | **Name:** | **Pragati M Kundalkar** | |
| **Course:** | **Python programming** | **USN:** | **4AL17EC072** | |
| **Topic:** | **Interactive Data Visualization with Bokeh.**  **Webscrabing with python beautiful soup.** | **Semester & Section:** | **6TH SEM**  **B - SEC** | |
| **AFTERNOON SESSION DETAILS** | | | |
| C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\python_14_1.jpg  C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\python_14_2.jpg | | | |