**DAILY ASSESSMENT FORMAT**

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| --- | --- | --- | --- |
| **Date:** | **04-06-2020** | **Name:** | **Pragati M Kundalkar** |
| **Course:** | **Digital design using HDL** | **USN:** | **4AL17EC072** |
| **Topic:** | **Hardware modeling using verilog,**  **FPGA and ASIC interview questions.** | **Semester & Section:** | **6TH SEM**  **B - SEC** |
| **Github Repository:** | **Pragati-m-k** |  |  |

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| **FORENOON SESSION DETAILS** |
| C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\HDL_4_1.jpg  C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\HDL_4_2.jpg |

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| **Date:** | **04-06-2020** | **Name:** | **Pragati M Kundalkar** | |
| **Course:** | **Python programming** | **USN:** | **4AL17EC072** | |
| **Topic:** | **Application 8: Build a web-based financial graph.** | **Semester & Section:** | **6TH SEM**  **B - SEC** | |
| **AFTERNOON SESSION DETAILS** | | | |
| C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\python_16_1.jpg  C:\Users\User\AppData\Local\Microsoft\Windows\INetCache\Content.Word\python_16_2.jpg | | | |