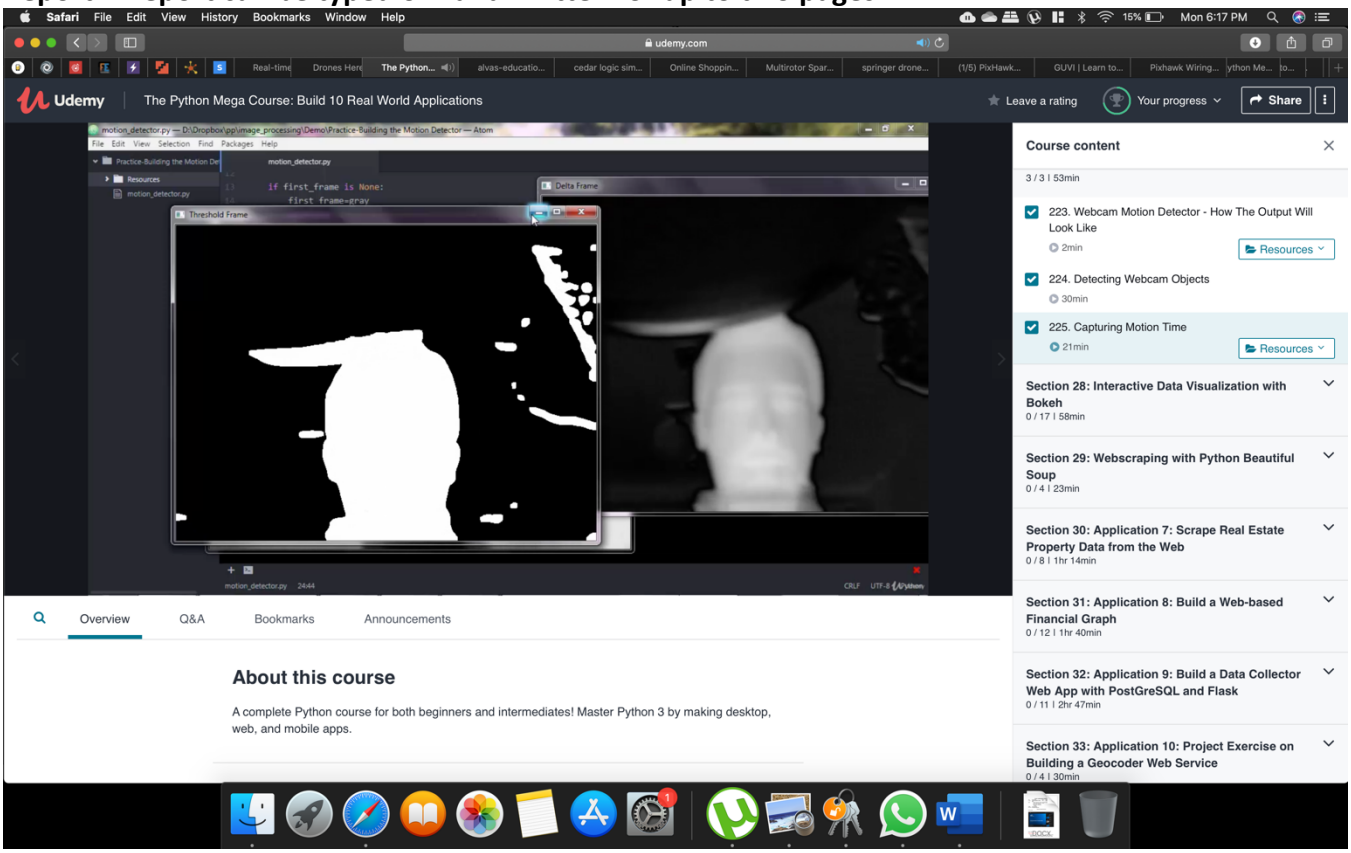
DAILY ASSESSMENT FORMAT

Date:	**1/06/2020**	**Name:**	**Prajwal Kamagethi Chakravarti P L**
Course:	**Python**	**USN:**	**4AL17EC073**
Topic:	**Application 6: Build a Webcam Motion Detector**	**Semester & Section:**	**6 & B**
Github Repository:	**https://github.com/alvas-education-foundation/Prajwal-Kamagethi.git**		

FORENOON SESSION DETAILS

Report – Report can be typed or hand written for up to two pages.

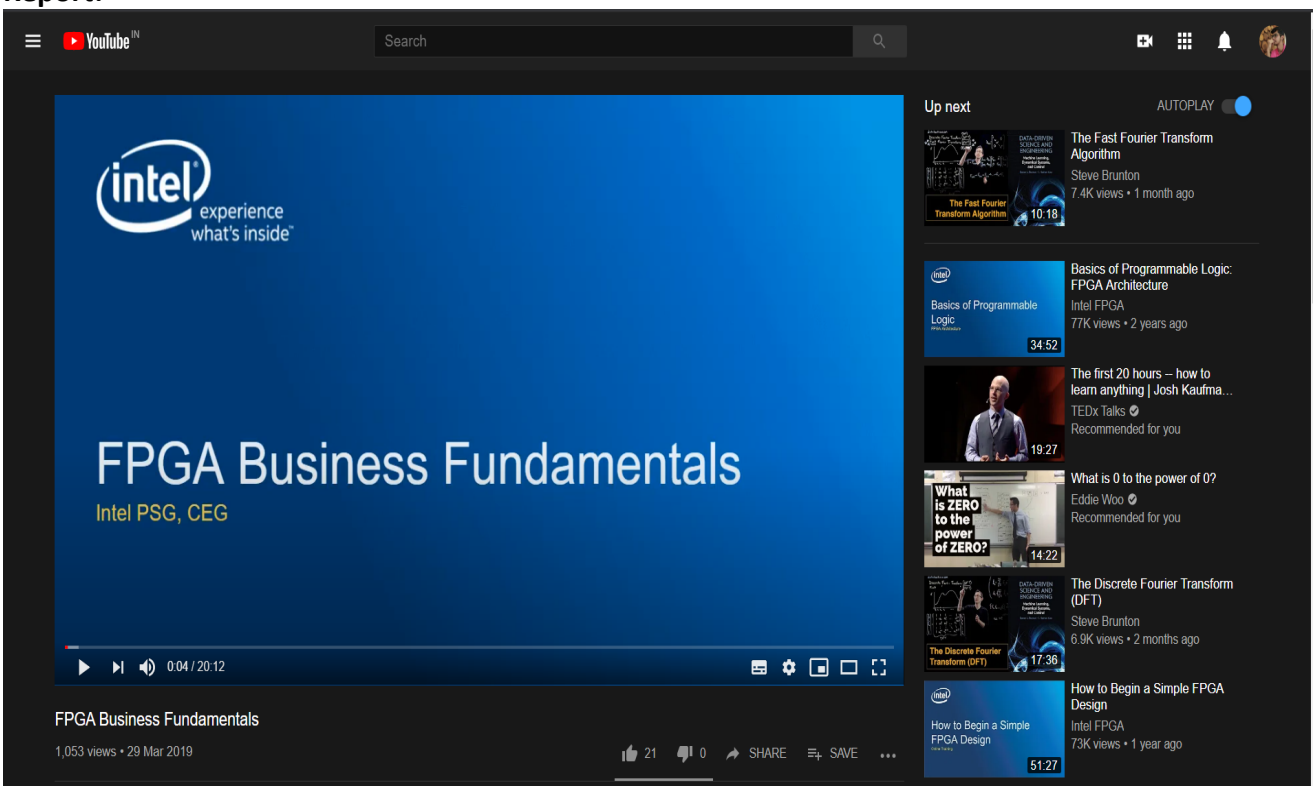


- **In this section,we learnt about building a Webcam Motion Detector.Creating Gray scale images and converting it into white and black.Also having raw colored images to detect motion.When motion is detected it starts noting the time at which the motion is detected.And that time and date is stored in excel file. Time at which motion was detected and saved in excel sheet is shown below.**

A	B	C
	Start	End
0	37:53.7	37:59.4
1	37:59.9	37:59.9
2	38:03.1	38:04.2
3	38:06.0	38:07.1
4	38:08.9	38:10.0
5	38:10.7	38:14.8

Date:	**01-06-2020**	**Name:**	**Prajwal Kamagethi Chakravarti P L**
Course:	**DIGITAL DESIGN USING HDL**	**USN:**	**4AL17EC073**
Topic:	• **1. Industry Applications of FPGA** • **FPGA Business Fundamentals** • **FPGA vs ASIC Design Flow** **FPGA Basics – A Look Under the Hood**	**Semester & Section:**	**6TH & B**
Github Repository:	**https://github.com/alvas-education-foundation/Prajwal-Kamagethi.git**		

Report:



Industry Applications of FPGA:

- **The impact of new FPGA features in industrial applications is analyzed in detail in three main areas, namely digital real-time simulation, advanced control techniques, and electronic instrumentation, with focus on mechatronics, robotics, and power systems design.**

FPGA vs ASIC Design Flow:

- **The below table shows the differences between FPGA and ASIC**

	FPGA	ASIC
NRE	✔	
Performance		✔
Time to market	✔	
Design Flow	✔	
Cost per Unit (High volume)		✔
Barrier to Entry	✔	
Energy Efficiency		✔
Analog Blocks		✔

Write a verilog code to implement NAND gate in all different styles:

1. **Gate Level Code:**

```
module NAND_2_gate_level(output Y, input A, B);
    wire Yd;
    and(Yd, A, B);
    not(Y, Yd);
endmodule
```

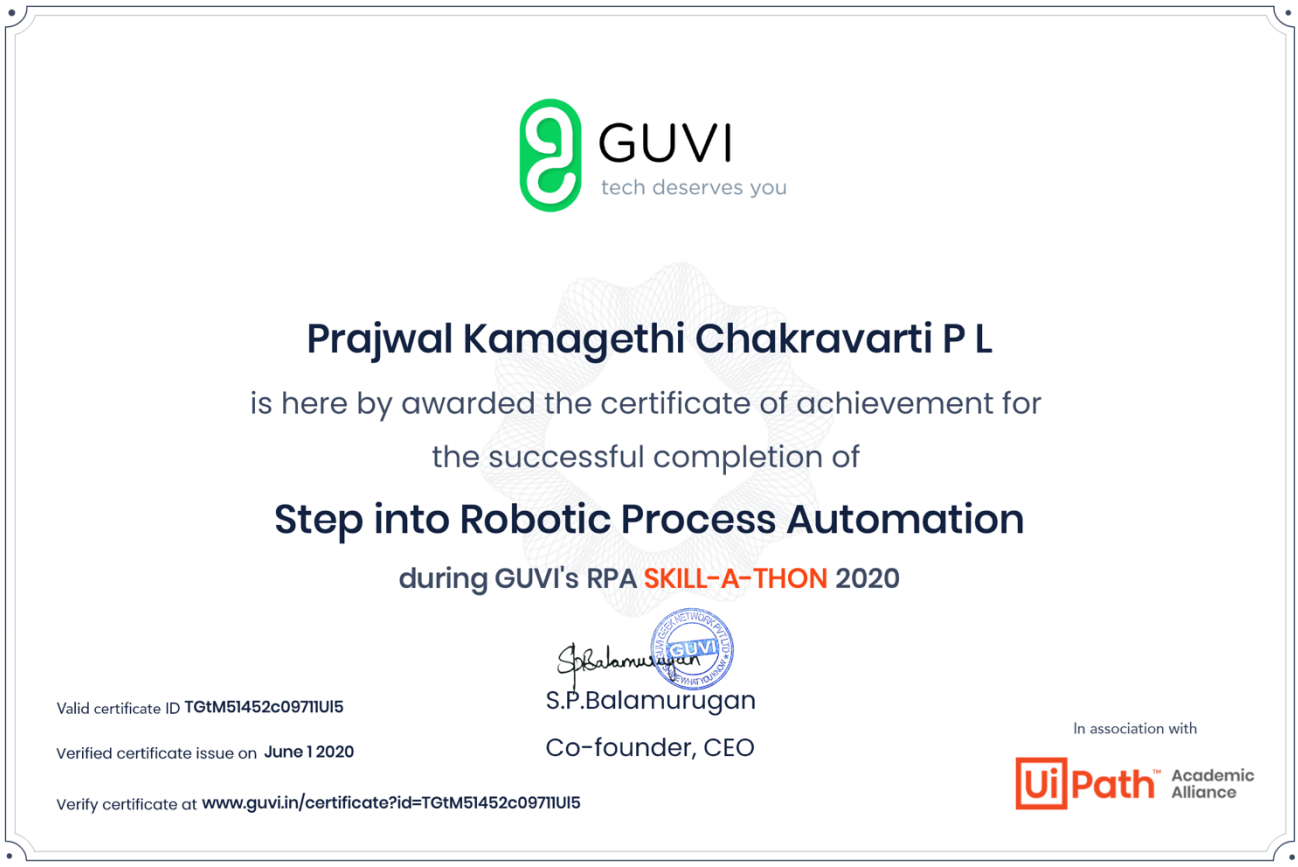
2. **Data Flow Code:**

```
module NAND_2_data_flow (output Y, input A, B);
    assign Y = ~(A & B);
endmodule
```

3. Behavioral Modelling code:

```
module NAND_2_behavioral (output reg Y, input A, B);
always @ (A or B) begin
    if (A == 1'b1 & B == 1'b1) begin
        Y = 1'b0;
    end
    else
        Y = 1'b1;
end
endmodule
```

- **RPA(Robotic Process Automation) Certificate:**



- **The above course was useful and interesting as it involved concepts of automation and roboti cs. Got to learn about UiPath tool for academic purpose. Also learnt to build basic automated bot to search movies in various websites.**