### **DAILY ASSESSMENT FORMAT**

Date:	04/06/2020	Name:	Prajwal Kamagethi Chakravarti P L
Course:	Python	USN:	4AL17EC073
Topic:	Application to Build a Web-based Financial Graph	Semester & Section:	6 & B
Github Repository:	https://github.com/alvas-		

# **FORENOON SESSION DETAILS** Image of the session: **▲ ● ▲ || ② |** | ♦ ♦ 68% **||** Thu 4:10 PM | Q | **②** || **=** Safari File Edit View History Bookmarks Develop Window Help ● ● ● 【 > □ PWM ESCs and Servos · PX4 User Guide ★ Leave a rating Your progress ★ Share 251. Candlestick Charts with Bokeh Rectangles 255. Note 256. Embedding the Bokeh Chart in a Webpage Section 32: Application 10: Build a Data Collector Web App with PostGreSQL and Flask Bookmarks About this course Section 34: Legacy Exercises A complete Python course for both beginners and intermediates! Master Python 3 by making 10 amazing Python apps. Section 35: Offers for my Other Python Courses 🔹 Safari File Edit View History Bookmarks Develop Window Help Jupyter Untitled Last Checkpoint: 10 minutes ago (autosaved) Logout File Edit View Insert Cell Kernel Widgets Help Trusted / Python 3 O P + 3< 2 15 ↑ ↓ HRun ■ C → Code + In [1]: from flask import Flask, render\_template app=Flask(\_\_name\_\_) plot(): from pandas\_datareader import data import datetime import fix\_yahoo\_finance as yf yf.pdr\_override() from bokeh\_forting import figure, show, output\_file from bokeh\_embed import components from bokeh\_embed import components start=datetime.datetime(2015,11,1) end=datetime.datetime(2016,3,10) df=data.get\_data\_yahoo(tickers="G00G", start=start, end=end) def inc\_dec(c, o): if c > o: value="Increase" elif c < o: value="Decrease"</pre> value="Decreaselse: value="Equal" return value df["Status"]=[inc\_dec(c,o) for c, o im zip(df.Close,df.Open)] df["Middle"]=(df.Open+df.Close)/2 df["Height"]=abs(df.Close-df.Open) p=figure(x\_axis\_type='datetime', width=1000, height=300) p.title.text="Candlestick Chart" p.grid.grid\_line\_alpha=0.3



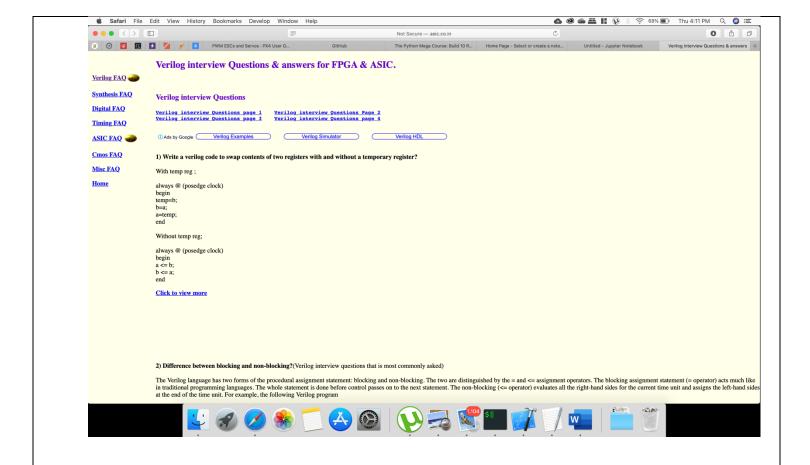
## Report – Report can be typed or hand written for up to two pages.

In this section we learnt analyzing Stock Market Data, Plotting Stock Market Data Candlestick Charts, Updating Candlestick Charts with Bokeh Quadrants, Learnt to plot Candlestick Charts with Bokeh Rectangles, Creating Candlestick Segments, Stylizing the obtained Chart, Learnt the Concept Behind Embedding Bokeh, Sharing the Charts in a Flask Webpage Learnt how to Embed the Bokeh Chart in a Webpage and also learnt to Deploy the Chart Website to a Live Server.

Date:	04-06-2020	Name:	Prajwal Kamagethi Chakravarti P L	
Course:	DIGITAL DESIGN USING HDL	USN:	4AL17EC073	
Topic:	Hardware modelling using     Varileg	Semester & Section:	6 <sup>TH</sup> & B	
	Verilog • FPGA and ASIC Interview questions	& Section.		
Github Repository:	https://github.com/alvas-education- foundation/Prajwal-Kamagethi.git			

## Image of the session:





Report: In this section, we learnt about the Verilog hardware description language.

- Understood the difference between behavioral and structural design styles.
- Learnt to write test benches and analyze simulation results.
- Learnt to model combinational and sequential circuits.
- Distinguish between good and bad coding practices.
- Case studies with some complex designs.

TASK: Implement a simple T Flipflop and test the module using a compiler.

```
Design:
```

```
module tff ( input clk,
       input rstn,
       input t,
      output reg q);
 always @ (posedge clk) begin
 if (!rstn)
  q <= 0;
  else
   if (t)
     q <= ~q;
   else
     q <= q;
end
endmodule
Testbench
module tb;
reg clk;
reg rstn;
reg t;
tff u0 ( .clk(clk),
      .rstn(rstn),
      .t(t),
     .q(q));
 always #5 clk = ~clk;
 initial begin
  {rstn, clk, t} <= 0;
  $monitor ("T=%0t rstn=%0b t=%0d q=%0d", $time, rstn, t, q);
  repeat(2) @(posedge clk);
  rstn <= 1;
  for (integer i = 0; i < 20; i = i+1) begin
   reg [4:0] dly = $random;
   #(dly) t <= $random;
  end
 #20 $finish;
 end
```

#### endmodule **▲** 🖎 💫 🔅 64% 🗈 Thu 4:28 PM 🔍 🔕 🖃 🐞 Safari File Edit View History Bookmarks Develop Window Help 0 6 0 m edaplayground.com O O E Favourites Edit code - EDA Playground EDA playground design.sv + Brought to you by A DOULOS ▼ Languages & Libraries module tff ( input clk, input rstn, input t, output reg q); Testbench + Design UVM / OVM 0 None Other Libraries () None OVL 2.8.1 SVUnit 2.11 SVAUnit 3.0 Smonitor ("T=W0t rstn=W0b t=W0d q=W0d", Stime, rstn, t, q); repect(2) @(posedge clk); rstn <= 1; for (integer i = 9; i < 20; i = i+1) begin reg [4:0] dly = Srondom; end(by) t <= Srondom; ☐ Enable TL-Verilog () Enable Easier UVM 1 Enable VUnit 1 ▼ Tools & Simulators 6 Cadence Xcelium 19.09 \$ Compile & Run Options -access +rw Use run.do Tcl file Open EPWave after run Download files after run Examples ▼ Community Collaborate Add a title to help you find your playground Public (anyone with the link can view) В І Н | 66 ⊨ ⊨ | % | ⊛ | ⊚ A short description will be helpful for you to remember your playground's details