Date:	04-06-2020	Name:	Rajeshwari Gadagi
Course:	HDL	USN:	4AL17EC076
Topic:	Hardwase modelling using Verilog,interview questions	Semester and section:	6 <sup>th</sup> sem and B sec

## Logic design

- Generate a netlist of gates/flip-flops or standard cells.
- A standard cell is a pre-designed circuit module (like gates, flip-flops, multiplexer, etc.) at the layout level.
- Various logic optimization techniques are used to obtain a cost effective design.
- There may be conflicting requirements during optimization:
  - · Minimize number of gates.
  - · Minimize number of gate levels (i.e. delay).

## **VLSI Design Flow**

- · Standardized design procedure
  - Starting from the design idea down to the actual implementation.
- Encompasses many steps:
  - Specification
  - Synthesis
  - Simulation
  - Layout
  - Testability analysis

## **Main Objectives of the Course**

## **Hardware Modeling Using Verilog**

- 1. Learn about the Verilog hardware description language.
- Understand the difference between behavioral and structural design styles.
- 3. Learn to write test benches and analyze simulation results.
- 4. Learn to model combinational and sequential circuits.
- 5. Distinguish between good and bad coding practices.
- 6. Case studies with some complex designs.

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Date:	04-06-2020	Name:	Rajeshwari Gadagi
Course:	Python programming	USN:	4AL17EC076
Topic:	Build a web based financial graph	Semester and section:	6 <sup>th</sup> sem and B sec

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