

Date:	04-06-2020	Name:	Rajeshwari Gadagi
Course:	HDL	USN:	4AL17EC076
Topic:	Hardwase modelling using Verilog,interview questions	Semester and section:	6 th sem and B sec

- **Logic design**

- Generate a netlist of gates/flip-flops or standard cells.
- A standard cell is a pre-designed circuit module (like gates, flip-flops, multiplexer, etc.) at the layout level.
- Various logic optimization techniques are used to obtain a cost effective design.
- There may be conflicting requirements during optimization:
 - Minimize number of gates.
 - Minimize number of gate levels (i.e. delay).

VLSI Design Flow

- Standardized design procedure
 - Starting from the design idea down to the actual implementation.
- Encompasses many steps:
 - Specification
 - Synthesis
 - Simulation
 - Layout
 - Testability analysis

Main Objectives of the Course

Hardware Modeling Using Verilog

1. Learn about the Verilog hardware description language.
2. Understand the difference between behavioral and structural design styles.
3. Learn to write test benches and analyze simulation results.
4. Learn to model combinational and sequential circuits.
5. Distinguish between good and bad coding practices.
6. Case studies with some complex designs.

Hardware Modeling Using Verilog

- Design Complexity increases Rapidly
- Increased size and complexity
- Fabrication technology improving
- CAD tools are essential
- conflicting requirements like area, speed and energy consumption

* Moore's law

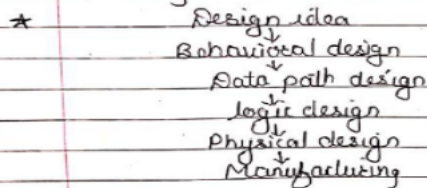
- Exponential growth
- Design complexity increases rapidly
- automated tools are essential
- Must follow well-defined design flow

* VLSI Design Flow

- Specification
- Synthesis
- Simulation
- Layout
- testability analysis and many more
- Need to use CAD tool

* Two competing HDLs -

1. Verilog
2. VHDL



Interview Questions for FPGA & ASIC

Verilog code to swap contents of two registers - with temp reg -	without temp reg -
always @ (posedge clock)	always @ (posedge clock)
begin	begin
temp = b;	a <= b;
b = a;	b <= a;
a = temp;	end
end	

Open a file -	Close a file -
integer file;	integer file, r;
file = \$fopen("filename");	r = \$fopen(file);
file = \$fopenw("filename");	r = \$fopenw(file);
file = \$fopena("filename");	

- * Sensitivity list :- indicates that when a change occurs to any one of elements in the list change, begin - end statement inside that always block will get executed

- * PLI (Programming language interface) of Verilog HNC is a mechanism to interface Verilog programs with programs written in C language

Date:	04-06-2020	Name:	Rajeshwari Gadagi
Course:	Python programming	USN:	4AL17EC076
Topic:	Build a web based financial graph	Semester and section:	6 th sem and B sec

```

## Build a web-based financial graph.
• candlestick chart is used for analysis in stock marketing data
• Downloading Datasets with Python -
  from pandas_datareader import data
  import datetime

• Stock Market Data Candlestick charts -
  start = datetime.datetime(2016, 3, 1)
  end = datetime.datetime(2016, 3, 10)
  df = data.DataReader(name="GOOG", data_source="yahoo",
                       start=start, end=end)
  df

• Embedding the Bokerh Chart in a webpage -
→ from flask import flask, render_template
  app = Flask(__name__)
  @app.route('/')
  def home():
      return render_template("home.html")
  @app.route('/about/')
  def about():
      return render_template("about.html")
  if __name__ == "__main__":
      app.run(debug=True)

• Code for script :-
  from flask import flask, render_template
  app = Flask(__name__)
  @app.route('/plot/')
  def plot():
      from pandas_datareader import data

```

```
.import datetime
from bkeh.plotting import figure, show, output_file,
from bkeh.embed import components
from bkeh.resources import ImportCon
start = datetime.datetime(2015, 11, 1)
end = datetime.datetime(2016, 3, 16)
df = data.DataReader(name="GOOG", data_source="yahoo",
                     start=start, end=end)
```

Plotting:-

```
{% extends "layout.html" %}
{% block contents %}
<div class="about">
  <h1> my about page </h1>
  <p> This is a test website again </p>
</div>
{% endblock %}
```