**DAILY ASSESSMENT FORMAT**

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| **Date:** | **04 june 2020** | **Name:** | **Roshni A B** |
| **Course:** | **HDL** | **USN:** | **4AL17EC080** |
| **Topic:** | **Hardware modelling using Verilog**  **FPGA and ASIC interview questions** | **Semester & Section:** | **6TH SEM B SEC** |
| **Github Repository:** | **Roshni\_online** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR26.828\CamScanner 06-04-2020 12.37.23_11.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR31.750\CamScanner 06-04-2020 12.37.23_12.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR36.734\CamScanner 06-04-2020 12.37.23_13.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR39.453\CamScanner 06-04-2020 12.37.23_14.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DI59.984\CamScanner 06-04-2020 12.37.23_10.jpg C:\Users\Admin\AppData\Local\Temp\Rar$DR12.3656\CamScanner 06-04-2020 12.37.23_9.jpg** |
| **C:\Users\Admin\AppData\Local\Temp\Rar$DI44.640\CamScanner 06-04-2020 12.37.23_1.jpg C:\Users\Admin\AppData\Local\Temp\Rar$DR51.125\CamScanner 06-04-2020 12.37.23_2.jpg** |

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| **Date:** | **04 june 2020** | **Name:** | **Roshni A B** | |
| **Course:** | **Python Programming** | **USN:** | **4AL17EC080** | |
| **Topic:** | **Application 9: Build a web-based financial graph** | **Semester & Section:** | **6th sem B sec** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR10.5359\CamScanner 06-04-2020 12.37.23_8.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR10.6844\CamScanner 06-04-2020 12.37.23_7.jpg** | | | |
| **C:\Users\Admin\AppData\Local\Temp\Rar$DR10.5437\CamScanner 06-04-2020 12.37.23_6.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR11.4640\CamScanner 06-04-2020 12.37.23_5.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR11.6469\CamScanner 06-04-2020 12.37.23_3.jpg**  **C:\Users\Admin\AppData\Local\Temp\Rar$DR12.2187\CamScanner 06-04-2020 12.37.23_4.jpg** | | | |