DAILY ASSESSMENT FORMAT

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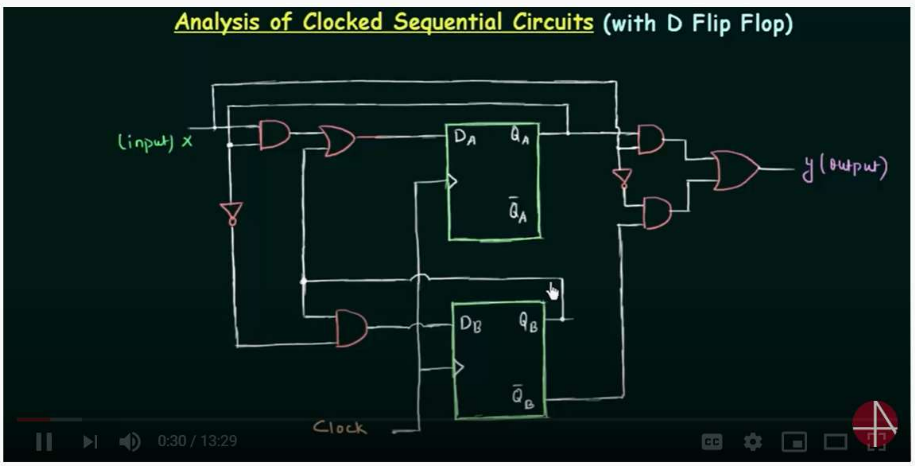
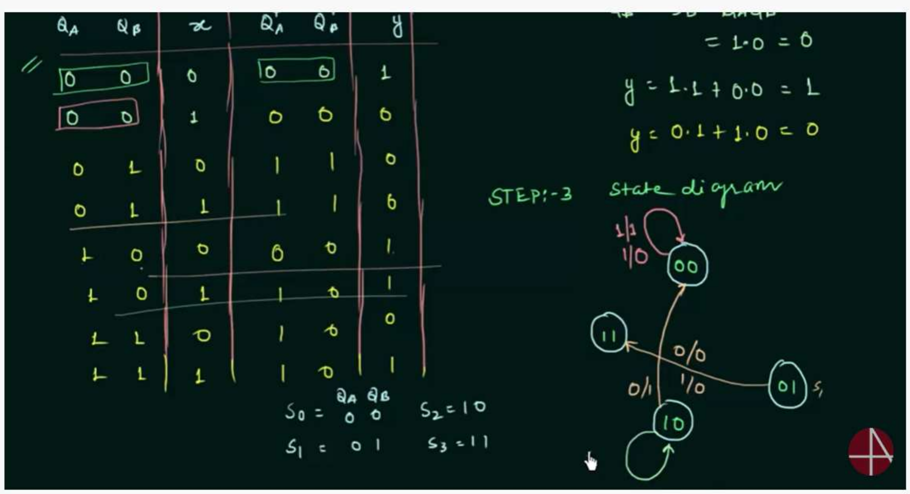
Course:	**Logic Design**	**USN:**	**4AL17EC103**
Topic:	1. **Analysis of clocked sequential circuits** 2. **Digital clock design**	**Semester & Section:**	**6-B**
Github Repository:	**Sachin-Courses**		

FORENOON SESSION DETAILS



Analysis of Clocked Sequential Circuits (with D Flip Flop)



Analysis of Clocked Sequential Circuits (with D Flip Flop)

NALYSIS OF CLOCKED SEQUENTIAL CIRCUITS

- Some flip-flops have asynchronous inputs that are used to force the flip-flop to a particular state independently of the clock

- The input that sets the **flip-flop to 1 is called preset or direct set.** The input that clears the flip-flop to 0 is called **clear or direct reset.**

- When power is turned on in a digital system, the state of the flip-flops is unknown. The direct inputs are useful for bringing all flip-flops in the system to a known starting state prior to the clocked operation.

- The knowledge of the type of flip-flops and a list of the Boolean expressions of the combinational circuit provide the information needed to draw the logic diagram of the sequential circuit. The part of the combinational circuit that gene rates external outputs is described algebraically by a set of Boolean functions called **output equations.** The part of the circuit that generates the inputs to flip-flops is described algebraically by a set of Boolean functions called flip-flop input equations **(or excitation equations).**

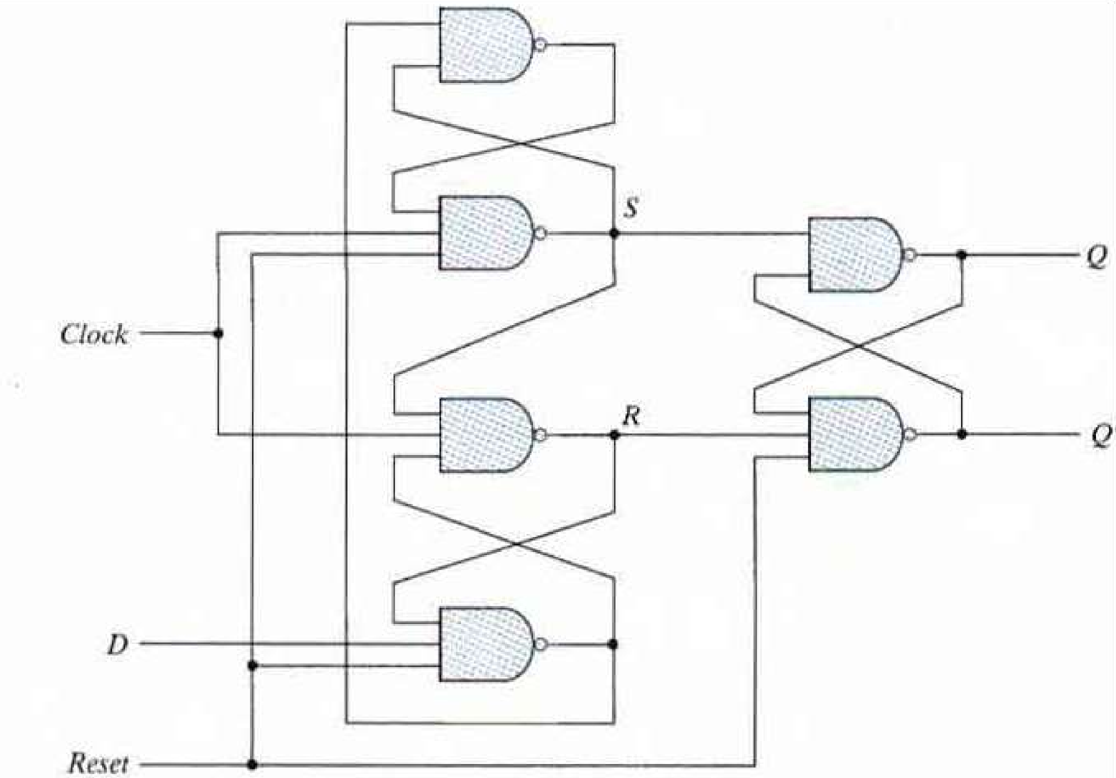
- The information available in a state table can be represented graphically in the form of a **state diagram.** In this type of diagram a state is represented by a circle and the (clock-triggered) transitions between states are indicated by directed lines connecting the circles.

- The time sequence of inputs, outputs, and flip-flop states can be enumerated in a state table (transition table). The table has four parts present state, next state, inputs and outputs.

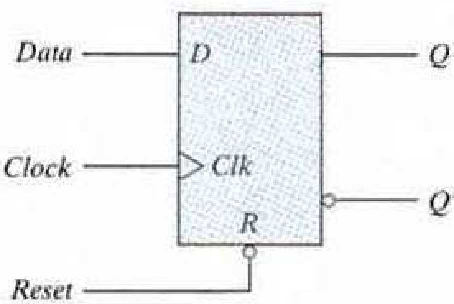
- In general a sequential circuit with **'m' flip-flops and 'n' inputs needs 2^{m+n}** rows in the state table.

Positive Edge Triggered D Flip-flop

- A circuit diagram of a Positive edge triggered D Flip-flop is shown as below. It has an **additional reset input** connected to the three NAND gates.



(a) Circuit diagram



(b) Graphic symbol

R	Clk	D	Q	Q'
0	X	X	0	1
0	↑	0	0	1
0	↑	1	1	0

(b) Function table

D flip-flop with asynchronous reset

- When the **reset input is 0 it forces output Q' to Stay at 1** which clears output Q to 0 thus resetting the flip-flop.

- Two other connections from the reset input ensure that the S input of the third **SR latch stays at logic 1** while the reset input is at 0 regardless of the values of D and Clk.

- Function table suggests that:

- **When R = 0, the output is set to 0 (independent of D and Clk).**

- The clock at Clk is shown with an upward arrow to indicate that the flip-flop triggers on the positive edge of the clock.

- The value in D is transferred to Q with every positive-edge clock signal provided that R = 1.

Analysis with D Flip-Flops

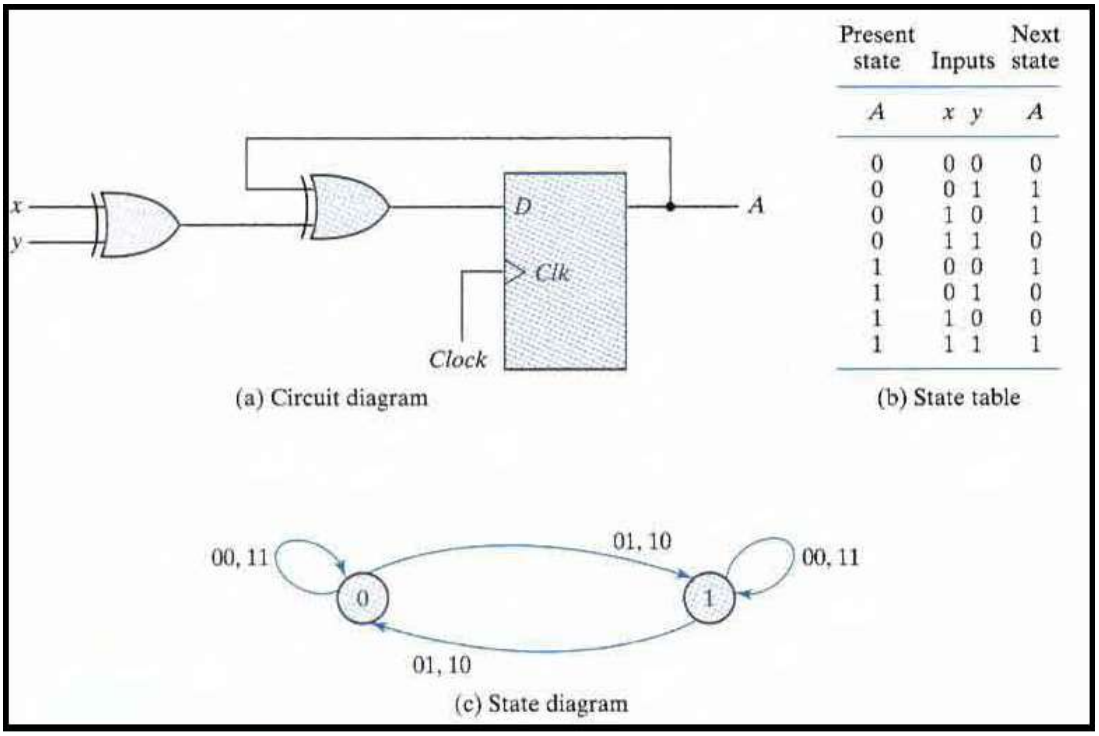
- The input equation of a D Flip-flop is given by $\mathbf{D_A = A \oplus x \oplus y}$. D_A means a D Flip-flop with output A.

- The x and y variables are the inputs to the circuit. No output equations are given, which implies that the output comes from the output of the flip-flop.

- The state table has one column for the present state of flip-flop 'A' two columns for the two inputs, and one column for the next state of A.

- The next-state values are obtained from the state equation $\mathbf{A(t + 1) = A \oplus x \oplus y}$.

- The expression specifies an odd function and is equal to 1 when only one variable is 1 or when all three variables are 1.



(a) Circuit diagram

(b) State table

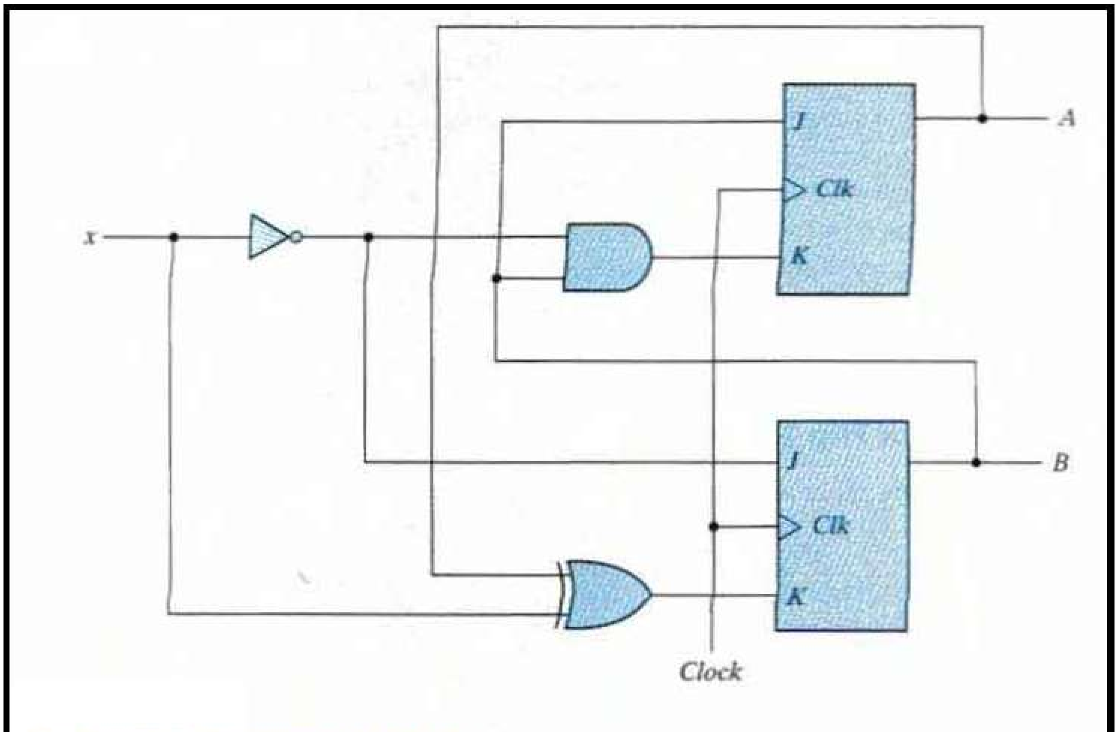
(c) State diagram

Analysis with JK Flip-Flops

- The circuit can be specified by the flip-flop input equations:
  - **$J_A = B$; $K_A = Bx'$**
  - **$J_B = x'$; $K_B = A'x + Ax' = A \oplus x$**
- The next state of each flip-flop is evaluated from the corresponding J and K inputs and the characteristic table of the JK flip-flop listed as:
  - **When J = 1 and K = 0 the next state is 1**
  - **When J = 0 and K = 1 the next state is 0**

- **When J = 0 and K = 0 there is no change of state and the next-state value is the same as that of the present state.**

- **When J = K = 1, the next-state bit is the complement of the present-state bit.**



Sequential circuit with *JK* flip-flop

- The characteristic equations for the flip-flops are

  - **A(t + 1) = JA' + K'A**

  - **B(t + 1) = JB' + K'B**

- This gives us the state equation of A by substituting the values of J_A, K_A

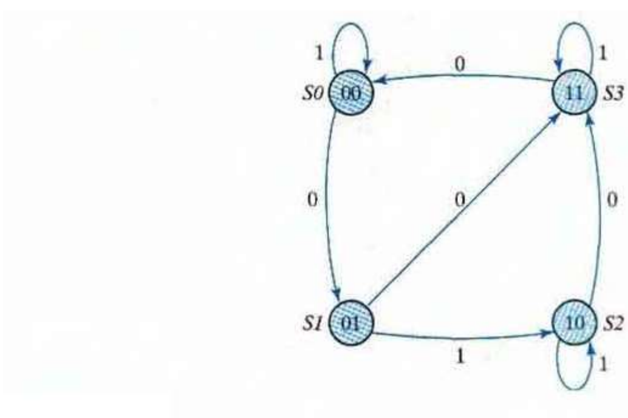
State Table for Sequential Circuit with JK Flip-Flops

Present State		Input	Next State		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

- **A(t + 1) = BA' + (Bx')'A = A'B + AB' + Ax**

- The state equation provides the bit values for the column headed "Next State" for A in the state table. Similarly, the state equation for flip-flop B can be derived from the characteristic equation by substituting the values of J_B and K_B.:

  - **B(t + 1) = x'B' + (A ⊕ x)'B = B'x' + ABx + A'Bx'**



State diagram of the circuit

Analysis with T Flip-Flops

- The circuit can be specified by the characteristic equations:

  - **Q(t+1) = T ⊕ Q = T'Q + TQ'**

- The sequential circuit has two flip-flops A and B, one input x, and one output y and can be described algebraically by two input equations and an output equation:

  - $T_A = Bx$

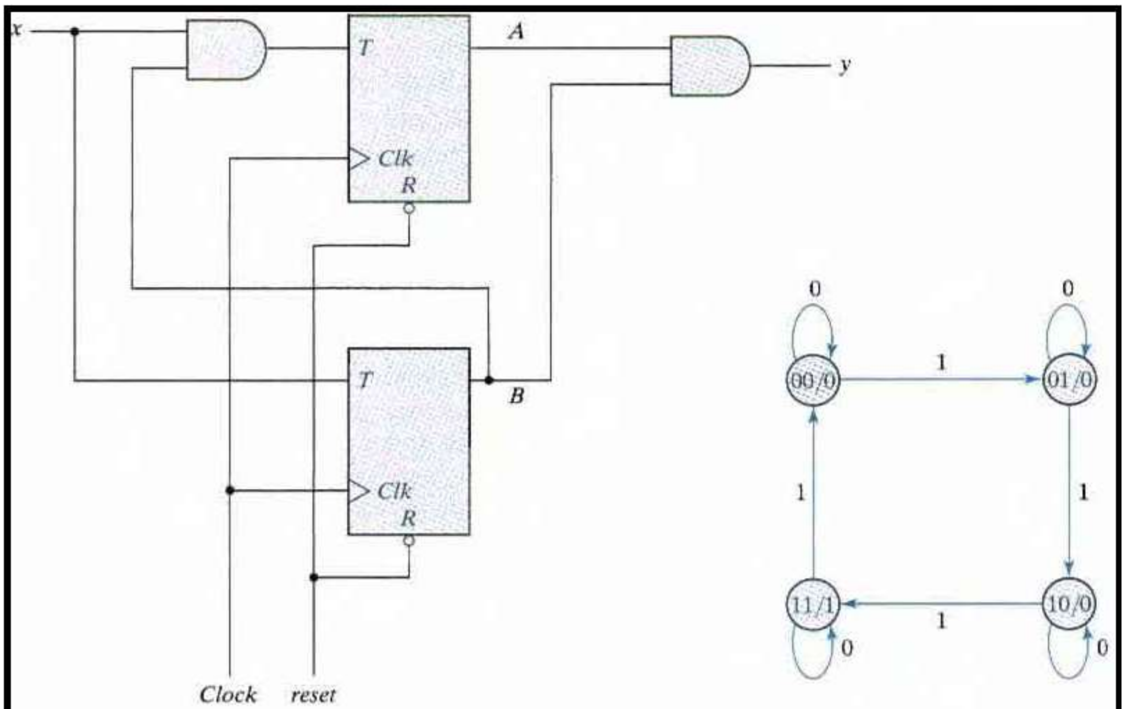
  - $T_B = x$

  - $y = AB$

- The state table for the circuit is listed below. The values for y are obtained from the output equation. The values for the next state can be derived from the state equations by substituting T_A and T_B in the characteristic equations yielding:

  - $A(t + 1) = (Bx)' A + (Bx)A' = AB' + Ax' + A'Bx$

  - $B(t + 1) = x \oplus B$



(a) Circuit diagram

(b) State diagram

Sequential circuit with *T* flip-flops