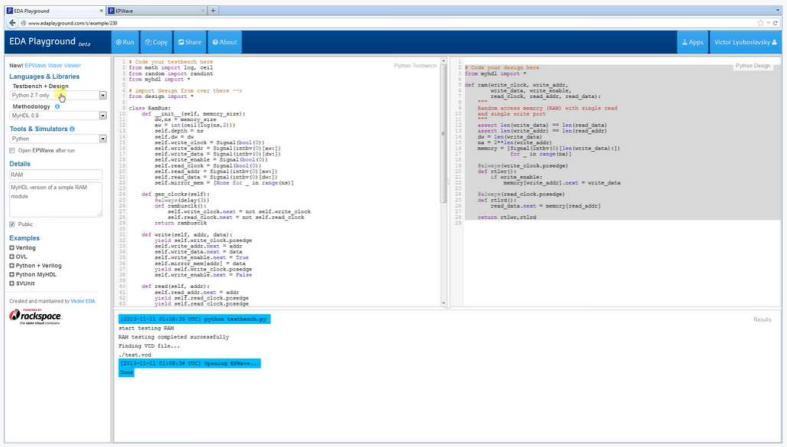
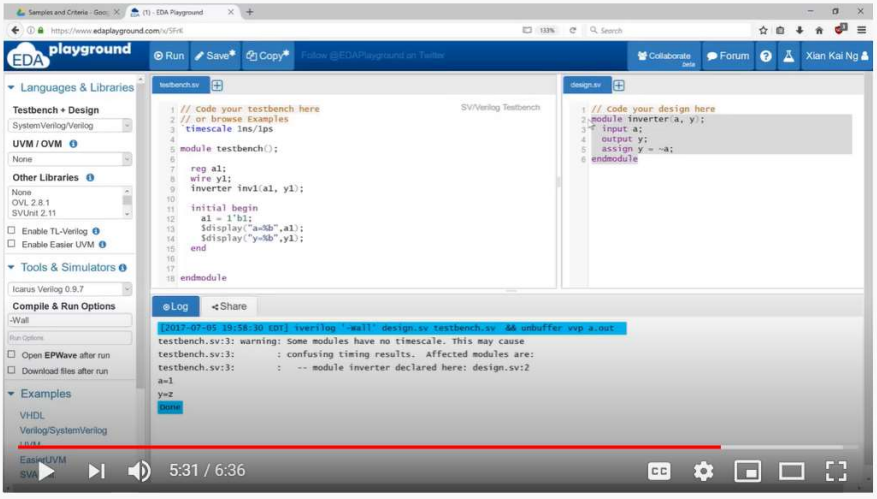
DAILY ASSESSMENT FORMAT

Date:	**03/06/2020**	**Name:**	**Sachin Krishna Moger**
Course:	**DIGITAL DESIGN USING HDL**	**USN:**	**4AL17EC103**
Topic:	***EDA Playground Tutorial Demo Video*** ***How to Download And Install Xilinx Vivado Design Suite*** ***Vivado Design Suite for implementation of HDL code***	**Semester & Section:**	**6-B**
Github Repository:	**Sachin-Courses**		

FORENOON SESSION DETAILS



EDA Playground Introduction -- Simulate Verilog from a Web Browser



Verilog on EDA Playground Starting Tutorial

What is EDA Playground?

EDA Playground gives engineers immediate hands-on exposure to simulating SystemVerilog, Verilog, VHDL, C++/SystemC, and other HDLs. All you need is a web browser. The goal is to accelerate learning of design/testbench development with easier code sharing and simpler access to EDA tools and libraries.

- *With a simple click, run your code and see console output in real time.*
- *View waves for your simulation using EPWave browser-based wave viewer.*
- *Save your code snippets ("Playgrounds").*
- *Share your code and simulation results with a web link. Perfect for web forum discussions or emails. Great for asking questions or sharing your knowledge.*
- *Quickly try something out*
    - *Try out a language feature with a small example.*
    - *Try out a library that you're thinking of using.*

Simulators

- Synopsys VCS
    - Commercial simulator for VHDL and SystemVerilog
- Cadence Incisive
    - Commercial simulator for VHDL and SystemVerilog (VHDL simulation not yet implemented on EDA Playground)
- Aldec Riviera-PRO
    - Commercial simulator for VHDL and SystemVerilog
    - Riviera-PRO Product Manual (registration required)
- Incisive Specman Elite
    - Commercial simulator that supports e Verification Language, IEEE 1647
    - Works with Cadence Incisive
    - Hello e World Video Tutorial
- GHDL
    - an open-source simulator for the VHDL language
    - fully supports the 1987, 1993, 2002 versions of the IEEE 1076 VHDL standard and partially the latest 2008 revision (well enough to support fixed_generic_pkg or float_generic_pkg)
- Icarus Verilog
    - Version 0.10.0 (devel) supports several SystemVerilog features.

Compilers and Interpreters

- C++
- Perl
- Python
- Csh (C Shell)

Libraries & Methodologies

For settings and options documentation, see Languages & Libraries Options

Available libraries and methodologies:

SystemVerilog and Verilog

- UVM - Universal Verification Methodology
  - UVM 1.2 Class Reference
    - What's New in UVM 1.2 on YouTube
  - UVM 1.1d Class Reference
- OVM - Open Verification Methodology
  - OVM 2.1.2 Class Reference
  - OVM 2.1.2 User Guide
- OVL - Open Verification Library
  - OVL Library Reference Manual
  - OVL Quick Reference
- ClueLib - A generic class library in SystemVerilog
  - ClueLib API Documentation
- svlib - A Programmer's Utility Library for SystemVerilog
  - svlib User Guide

VHDL

- OVL - Open Verification Library
  - OVL Library Reference Manual
  - OVL Quick Reference
- PSL - Property Specification Language
  - Natively supported by Riviera-PRO
- OSVVM - Open Source VHDL Verification Methodology
- UVVM - Universal VHDL Verification Methodology